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# **Reducing Development Time with the Embedded PC**

# Reducing Development Time with the Embedded PC

The embedded PC can help reduce the time to develop embedded systems by simplifying or eliminating steps in the development cycle

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## Summary

The embedded PC, leveraging off of the ubiquitous desktop and notebook PC's, allows embedded system developers to reduce the time it takes to get a product out the door. Though the embedded PC is not appropriate for all embedded systems applications, many systems can benefit from the reduction and possible elimination of development steps. The reduction or elimination directly impacts development time.

Claims of reducing the time to develop embedded systems have been around since the first microprocessor was programmed. Most of these claims are long on promise and short on reality. The embedded PC will not reduce all development times by some huge percentage, but it can significantly reduce the time to develop many embedded systems. In some cases, it can completely eliminate almost all of the traditional development steps.

This article investigates the impact of the embedded PC on development time. Many in the industry have been feeling the pressure to develop systems in ever shorter times. The 1995 Embedded Systems Survey Report found that the median time to develop an embedded system is 7.5 months. The same report revealed that this median is expected to shrink to 6 months within 2 years. Even more startling is that within 2 years, 20% of developers feel that they will have only 3 months to develop a product. The most direct way to reduce time to market is to cut as much out of the development process as possible. If you don't have to do something, you have saved time. One advantage of the embedded PC is that many of the steps normally associated with design can be skipped.

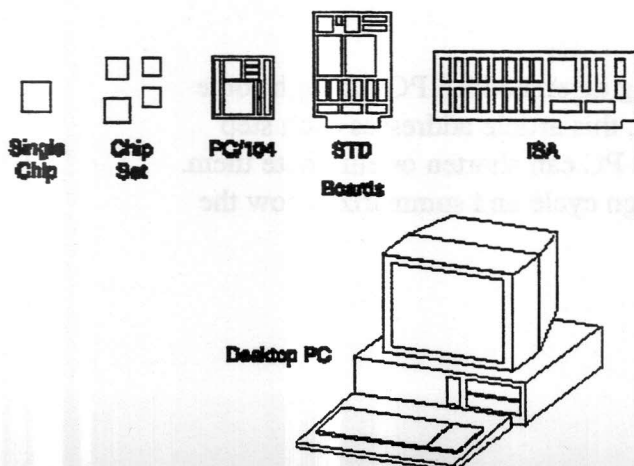


Figure 1 - The range of the embedded PC. An embedded system can be based on anything from a chip to a desktop PC and still maintain PC compatibility.



## Defining the Embedded PC

There is no single definition of the embedded PC. In general, an embedded system is regarded as an embedded PC if some of its architecture resembles the architecture of the IBM/PC. These computers are X86 based and use an interrupt, memory, and I/O map that is consistent with the IBM/PCs. On the desktop, the IBM/PC-based computers look very much the same. In the embedded world it is not as easy to identify the embedded PC. Figure 1 shows the range of what is considered an embedded PC.

An embedded PC can be a single chip (such as the Intel 80386EX) that has a subset of the entire PC architecture. It can also be a chipset surrounding the X86 microprocessor that is placed on a proprietary board. Or it can be a PC on a credit card sized board from S-MOS. Or a PC on an STD-bus card from Ziatech or a proprietary card like those from Radisys. An embedded PC can be based on the ISA bus but not look like an ISA card, like the PC/104 bus from Ampro.

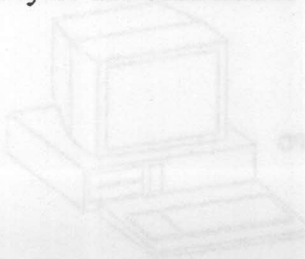
Many embedded PCs are based on ISA cards just like those used on the desktop. They just don't look like the desktop PC in that the enclosures they use are industrial strength and mount on a wall or in a rack.

## Benefits Available to all Forms of PC

Whatever the form of the embedded PC, they all can take advantage of the fact that they are, in varying degrees, PCs. They can all benefit from the reduction in development time brought about by the ubiquitous PC. Though the embedded PC is not perfect for everything, it has a number of advantages over other approaches. If the application can't take advantage of what the PC has to offer, the X86 is just another microprocessor option. But if the application can ride the coattails of the consumer PC products, you can reap significant savings in development time and cost (see sidebar, "The reasons to embed a PC").

Each embedded system follows a similar development cycle. After the requirement is defined, the steps are: system design, detailed design (hardware and software), prototype creation, system integration, debugging, and maintenance.

These same steps are carried out when using an embedded PC. Though some steps can be skipped with any development, this article addresses each step and discusses how the use of the embedded PC can shorten or eliminate them. Figure 2 depicts the embedded system design cycle and summarizes how the embedded PC can shorten the steps.





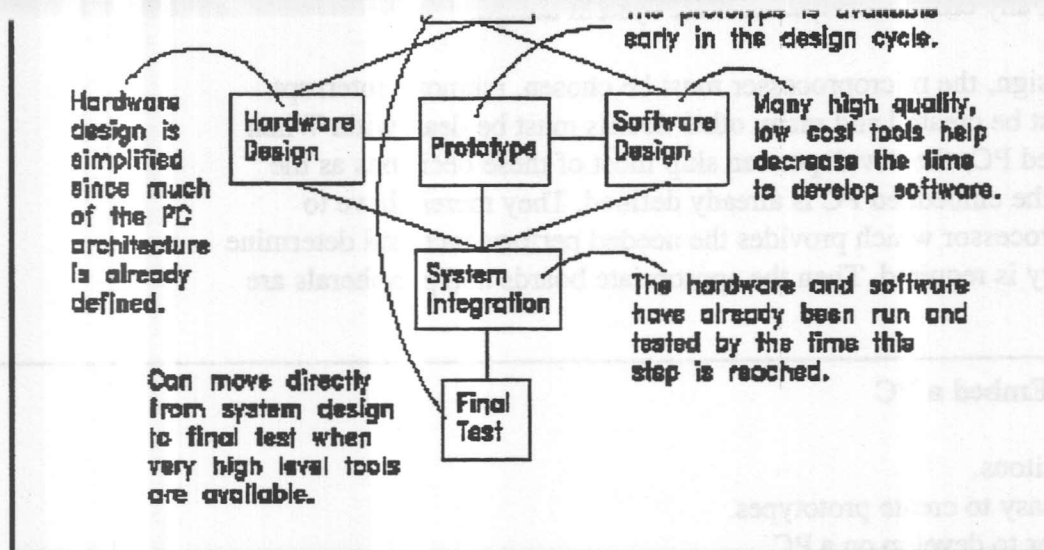


Figure 2 - The design cycle, and how the embedded PC can shorten steps.

An alternate approach uses Lotus 123, a spreadsheet program. Lotus 123 reads data from an RS-232 port and automatically inserts the data into a cell in the spreadsheet. The calculated results can also be taken from a cell and automatically sent to RS-232 ports. The entire development is reduced to connecting PC-based components together and configuring a spreadsheet.

### Automated Tools for Quick Development

Only certain embedded systems can take advantage of Lotus 123, but it is an example of the types of tools available in the PC world. Another example is LabView from National Instruments. This tool allows the developer to select needed functions as block diagrams and then connect them together graphically. Then the tool creates the program to perform the selected functions.

Other companies like Keithley Metrabyte and Data Translation have similar tools. As these tools become more powerful, they will significantly reduce development time.

Digital signal processing (DSP) can also benefit from the PC. Tools are now available that allow complex algorithms and instruments to be implemented by just connecting desired blocks on a PC's screen. An instrument that acquires data, presents the data on the screen, performs complex algorithms like an FFT, and displays frequency data in another window is easily created. Tools from Hyperception or Signalogic allow a complex DSP based instrument with a graphical interface to be created in a matter of hours.

### **Simplified System Design**

When the automated tools can't enable a jump from system design to final test, the standard development steps must be followed (Fig 2). The first step in developing any embedded system is the system design.

During system design, the microprocessor must be chosen, memory, interrupt and I/O maps must be created and many other details must be dealt with. When using the embedded PC, the developer can skip most of these decisions as the system design of the embedded PC is already defined. They merely have to choose the X86 processor which provides the needed performance and determine how much memory is required. Then the appropriate boards and peripherals are selected.

#### **The Reasons to Embed a PC**

- PCs are ubiquitous.
- PCs make it easy to create prototypes.
- It can be easier to develop on a PC
- PC expertise is available.
- PCs offer low cost hardware.
- Low cost, high quality development tools are available for the PC.
- A wide variety of PC-compatible products are available.
- Very high level automated tools are available.
- The PC architecture continues to offer increasing performance.
- PCs offer a huge range of display and input options.
- Many low level drivers are available.
- The shrinking PC for notebook computers results in technology that is ideal for embedded systems.

The time to create a system design from scratch can vary from a few hours for a simple system that doesn't require the approval of others, to weeks for more complex designs that must go through committee reviews. Once the embedded PC is selected, the time to go through the approval process is reduced since the number of options are reduced.

### **The Typically Split Detailed Design**

Once the system design is accomplished, the detailed hardware and software design begins. The design process is commonly split into hardware and software design. Then, once the hardware is ready, both parts are integrated and the debugging process begins.

The embedded PC provides a simplified hardware design since more options exist for the PC architecture than any other architecture. Fewer custom devices are required. The software design is also simplified with readily available off-the-shelf software modules.

## **It is Becoming a GUI World**

The world is moving towards graphical user interfaces (GUI) in a big way. In the not too distant future, most embedded systems will need a GUI. Cash registers, copy machines, industrial controls, and test equipment are examples of systems that have already moved to GUIs.

GUIs are not easy to create. They take a lot of time and are difficult to maintain. Normally a GUI is created by making complex calls to a graphical library or an operating system. Creating the code for these calls is very time consuming and tedious. Also, it is very difficult to make changes to the code.

### **“That GUI is nice, but what if we...”**

Once a GUI is finally created and seen on the screen, the layout is often less than optimum and a process of moving and modifying begins. To move something on the screen, it is necessary to modify the function call. Making the modification by changing the code with a text editor is very time consuming. The ideal approach is to just grab the object and move it or resize it. To change the operation of an active object on the screen, you want to just click on it and modify its definition.

To speed up this snail-like process and eliminate some of the tedium, GUI development tools are used. GUI development tools are moving quickly in the PC environment. They exist in other environments, but the high quality and low price of the PC-based tools makes them very attractive. Tools such as Visual C++, Visual Basic, and Delphi allow complete GUIs to be developed in a very short time. The savings can add up to weeks or even months compared to developing a GUI without these tools.

The desired result of the development process is a working product. At some stage in the development, the system must be integrated where the software is run on the hardware and the system is proven.

## **The Moment of Truth, Integration**

Integration is the high anxiety step in the development process. Here is where costly mistakes are found and must be fixed. Unfortunately, system integration usually happens near the end of the development cycle, when mistakes are most expensive to fix.

Depending upon the type of embedded system, the added cost to fix a mistake goes up by 2 to 10 times at each step. System integration is one of the most costly places to find and fix mistakes. This is also where schedules often



fall apart since this is the first time the design gets tested.

There are many ways to reduce the integration time. One of the best ways is to create a prototype early in the development process to prove the hardware and allow software testing. Development progresses without having to waste time creating test routines to make up for the lack of hardware.

### **Prototypes Reduce Integration Woes**

Prototyping is another area where the embedded PC really shines. Once the system design is accomplished, a functionally exact prototype can be made in a few days. Just about any interface imaginable is available for the PC. If the system must read voltages, run motors, read GPS position, synthesize waveforms, log data to a DAT drive, use a modem, control digital lines, send data on a network, or whatever, the card most likely exists. Moreover, the drivers for the board are also often available.

The time and expertise it takes to create a PC-based prototype is very low. Now, as the software is being created, a fully functioning prototype is available for testing. The hardware is also easily checked. The time and money needed to change the system at this stage, right after the system design is created, is much less than at the end of the project when system integration is normally attempted.

### **Native- vs. Cross-Development**

The code development step mostly fits into two categories, native-development and cross-development. When developing in a native environment, the code is developed and run on the same hardware. In a cross-development environment the application is developed on a host computer and must be loaded into target hardware to run. In many cases, the processor on the host and on the target are different so the application code can't run on the host at all.

Each approach has advantages and disadvantages. The native approach is often simpler since there is no need to connect and communicate between the host and the target. The cross-development approach allows more flexibility in the design of the target and allows the target to be monitored more easily.

A significant difference is cost. When developing in the native environment, the development hardware already exists, the computer on the desk. The cross development environment requires additional resources.

The PC thrives in both development approaches. As a native-development tool, the PC on the desk is used to develop and debug the application. Then the code is moved to the embedded PC-based product where it runs just like it did on the desktop.

The PC is also becoming the host of choice for cross-development. In this case the PC provides an easy to use and familiar environment. Most available



development tools that once used workstations are now available for Windows-based PCs.

When using the native environment there may be problems that can't be fixed with a native debugger. In these cases, an in-circuit emulator (ice) or logic analyzer can be used to monitor the system's operation.

### **An Ice that won't Freeze Accounting**

The PC affords another interesting option from the desktop world. A full function in-circuit emulator (costing from \$8,000 to \$30,000) can help find the really tough problems. Or Periscope's real-time hardware debugger can be used. This \$3,000 debugger provides trace and debugging functions that work with PC-based tools like Phar Lap Software's TNT Embedded Tool Suite.

As next generation X86s emerge, the on-chip debugging port becomes an interesting option. A very low cost board could sit in the desktop PC and interface to the internal registers in the microprocessor. Now the difference between native- and cross-development begins to blur.

### **Maintenance, Often Overlooked**

Embedded systems are usually difficult products to maintain. Once a product is shipped, the expertise within the company often drops quickly. The designers are assigned to new projects or leave the company. Eventually, maintenance is required and few remain who understand the design. When using the embedded PC, the hardware design is already well understood and the learning curve to get someone up to speed is reduced.

Documentation is a real problem in the embedded systems community. Many attempts have been made to address the problem. The common approach to documentation is to ignore the problem and hope it's never needed. When the PC is used, much of the hardware and lower level software is well documented. All that has to be documented is the higher level portions of the software.

The embedded PC can significantly reduce time to develop on projects where the application is able to take advantage of what the PC has to offer. The potential savings for each design step are summarized in Table 1. A comparison between a PC-based project and one without the advantages of the PC is made for each design step. The table provides insight into how much of a savings you could realize when using an embedded PC.

Whether the development cycle is reduced by just one week or by a year, it is still worth trying to achieve a reduction.

**Table 1 - Potential savings at each design step**

Design Step	Traditional	Embedded PC	Potential Savings
System Design	Start with blank paper and define the entire system.  (2 hours to 2 months)	Start with PC architecture and select from available options  (2 hours to 2 days)	No savings with very simple systems. Up to 6 weeks on complex designs.
Detailed Hardware Design	If using off-the-shelf products, select the appropriate boards. If designing from scratch, begin a long and tedious process of design.  (2 days to 2 years)	If using off-the-shelf products, select the appropriate boards. More options available to the PC than any other architecture. Less chance of requiring custom design. If designing custom board, many options from single chip to chip sets get you going quickly.  (2 days to 2 months)	If all needed boards are available to both options, no savings. If needed components exist in the PC world and not in other approaches, can save months.
Detailed Software Design	Write code, often from scratch.  (1 week to 2 years)	Use as much off-the-shelf software as possible. Use inexpensive but high quality tools. GUIs are much easier to create. Easier to find programmers familiar with the PC than some proprietary or lower volume approach. Can also use very high level tools like LabView or Lotus to quickly develop software without writing any code.  (2 days to 6 months)	If the application fits within the capabilities of the high level tools, the savings can be many months. If the application requires all code written from scratch, the savings is marginal. Still, many more low level drivers are available for PC products than any other architecture.

Design Step	Traditional	Embedded PC	Potential Savings
Prototype	<p>Must finish the detailed design before a prototype can be made. If using only available boards, the prototype is quickly assembled. If building from scratch, a prototype can be built only after the components are acquired and a board is laid out and fabricated.</p> <p>(1 week to 6 months)</p>	<p>Get any PC and select the boards that provide the functions needed. It doesn't have to look like the final product as long as it works like it.</p> <p>(2 days to 1 week)</p>	<p>Significant savings since the embedded versions of the PC work like the desktop versions. Almost any conceivable interface or peripheral is available for the PC. The prototype is assembled quickly and will work just like the final product. Savings from days to months.</p>
System Integration	<p>First time the entire system is tested. Very late in the design cycle. Hardware/software issues now must be worked out.</p> <p>(2 weeks to 6 months)</p>	<p>Final system integration consists of moving tested software from the desktop prototype to the final product. The software has already been tested with nearly identical hardware.</p> <p>(2 days to 2 weeks)</p>	<p>Savings from days to months. Serious problems already detected and fixed on the prototype.</p>
Maintenance	<p>If the system is properly documented, maintenance personnel must study the documentation and perform any required maintenance. Typically, the available documentation is very poor.</p> <p>(Doesn't affect product development time, costs later)</p>	<p>The PC is well known and documented. Easier to find knowledgeable maintenance personnel. When documentation is not adequately provided (as is typical) maintenance personnel can use other sources of PC documentation.</p>	<p>No savings to the development process. Cost comes later, if (when) problems surface. Also, the time to create new versions of older products is reduced if using a standard PC architecture.</p>







# **Design Considerations for the Embedded PC**

Third Party Vendor Reference, see P12



## INTRODUCTION

The acceptance of the PC Architecture into the business world has made it ideal for embedded PCs that are low cost and quick time-to-market. The vast availability of both PC hardware and software, development tools, and PC expertise provides engineers with a well defined platform. The design of an embedded PC requires understanding of all the hardware and software pieces. Depending on the application, the embedded PC may or may not require the complete functionality of a desktop PC. Some applications will require full PC compatibility while others may require only a subset. This paper describes the development tools, hardware and software design considerations for developing a cost-effective and quick time-to-market embedded PC.

### WHAT IS AN EMBEDDED PC?

The embedded PC can be very different from a traditional desktop PC. It can be completely hidden from the user with no display and no user input. Examples include single-line LCD screens with a keypad input. Even though these PCs appear to be no different than a microcontroller-based design they have the distinct advantage of being based on the PC platform. This allows the designer to use PC expertise, PC development tools, and desktop PC s for both software and hardware development.

### BASIC PC SYSTEM REQUIREMENTS AND COMPATIBILITY

The minimum configuration required for a DOS-based embedded PC is an Intel architecture processor, an 8254 timer, an 8259 interrupt controller and memory. A system based on only these components may not run MS-DOS\* but could run General Software Embedded DOS\* or Datalight ROM-DOS\*. This would still allow the software to be developed on a desktop PC.

There are several considerations that must be taken in determining if full PC compatibility is required in an embedded PC. For instance, in a portable design, it may not be necessary to support a floppy disk, thereby eliminating the requirement for the DMA channels typically used for floppy disk data transfers. Early understanding of the requirements of the design and possible PC compatibility tradeoffs can provide for a more cost-effective design.

It is important to determine if off-the-shelf software applications or software developed in-house will be used in the design. Software developed in-house provides more flexibility in the hardware design, whereas the ability to execute all off-the-shelf software requires full PC compatibility. Not all applications have the same hardware requirements as seen in Table 1 which allows hardware design flexibility in some off-the-shelf software applications.

Functionality	8254	8237	8259	RTC	8242	8250	PC Video
MSDOS*	X	X	X	X	X		X
Embedded DOS*	X		X				
ROM-DOS*	X		X				
MS Windows* 3.1	X		X	X	X		EGA,VGA
Smarterm/Procomm	X		X		X	X	X

\*Other Brands and Names are the property of their respective owners.

Table 1. Example of a Compatibility Table  
**EMBEDDED PC SOFTWARE CONSIDERATIONS**

The embedded PC architecture is composed of three layers. The bottom layer consists of the PC hardware, for example the CPU, Real Time Clock, DMA, Interrupt Controller, and various other devices depending on the compatibility required. One level up from the hardware is the BIOS which provides low-level drivers to interface to the hardware. Above the BIOS is the Disk Operating System (DOS) which provides a service of organizing files, disk functions, I/O functions, and launching applications. On top of these three layers resides the application. Due to the amount of time it takes to access the hardware through the BIOS or DOS, many software applications access the hardware directly. Figure 1 illustrates the three layer model and how the application software bypasses the other layers.

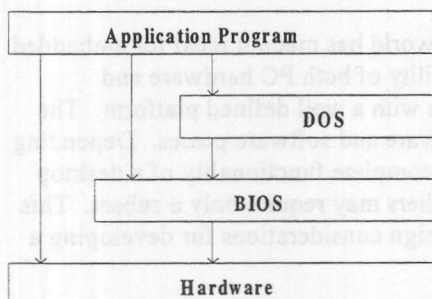


Figure 1. Three Layer Model

## BIOS

The BIOS is hardware dependent and typically requires some amount of changes for the embedded design. It is important to understand some of the basic components that make up a BIOS.

Typically a BIOS consists of seven main components; the Boot Vector, the Power On Self Test referred to as POST, the Boot-Strap, the BIOS compatibility address map, the BIOS Interrupt Service Routines (ISRs), the BIOS Device Service Routines (DSRs) and some configuration tables. The standard PC BIOS is 64K in size, located from F0000H to FFFFFH at the top 64K of the real mode address region(1MB). Many embedded PC BIOS vendors allow a range of sizes from 8K to 64K depending on the options required.

### Boot Vector

The Boot Vector is typically found at the top of the processor address space. After a reset due to either a software reset or a hardware reset, the processor jumps to the processor specific reset vector. The BIOS will contain a jump instruction (4 bytes) to pass control to the POST. The remaining bytes are used to indicate the BIOS manufacturer date and the PCs ID number.

### Power On Self Test

The POST contains tests and initialization routines for the hardware components. The POST can vary in size depending on the system hardware. For example, if the system does not require an 8042 keyboard controller, the keyboard/keyboard controller initialization code does not need to be compiled into the BIOS. Two POST tests that are worth mentioning are the CMOS Shutdown byte and the Optional ROM extension scan. The CMOS shutdown byte is a location in the CMOS RAM area of the Real Time Clock that provides information in determining the cause of a reset. The BIOS uses this shutdown byte to exit protected mode and skip the hardware tests. More information on this byte is discussed in the RTC section under EMBEDDED PC HARDWARE CONSIDERATIONS.

Another important feature in the POST is the ROM extension scan which allows easy software upgradability or additions to a BIOS without any knowledge of the current POST. These ROM extensions are typically used for ISA bus cards to install BIOS functions and initialize hardware on the card. During the POST, a search is conducted for ROM extensions located between C8000H to E0000H. The BIOS searches every 2K boundary for the word 55AAH which indicates a valid ROM extension. If a valid ROM extension is found, a ROM checksum is conducted to validate the contents,



and then the ROM extension code is executed. The ROM checksum requires byte 0 to the length minus one of the ROM extension to have a sum of zero. The last byte forces the checksum addition equal to zero.

Offset in the ROM Extension	Data
C8000-C8001	55AA
C8002	Length of extension. Number of 512 byte blocks, divisible by 4
C8003-End-1	Code
End	8 bit value to force the checksum value equal to zero.

Table 2. ROM Extension Example

These ROM extensions are used quite frequently for installing ROM-based DOS like Datalight's ROM-DOS\* or Microsoft's DOS\* in ROM. Microsoft's ROM Windows\* also uses this method for placing a 16K stub in real mode for installation. M-Systems has an option of installing their TFFS driver as a ROM extension. The ROM extension allows for a modular method of adding software to the embedded system.

After the POST, the BOOT strap loader or INT19 is executed and will search for a bootable disk in the system. The equipment list will indicate the number of floppy disks and hard disks available. If a flash disk is available for boot, it can install itself at the end of the list during its ROM extension installation. The first sector of the bootable disk is loaded into memory and the BIOS passes control to this data which in turn loads DOS.

#### BIOS Compatibility Table

The BIOS Compatibility table is a table of BIOS entry points that date back to the original PC/XT BIOS. This table needs to be installed to maintain compatibility with application software that calls on these entry points. The table resides from FE000H to FFFFFH and is optional with some BIOS manufacturers..

#### BIOS Interrupt Service Routines

BIOS Interrupt Service Routines (ISRs) are invoked by hardware interrupts from peripheral devices. They handle the low level software interface between peripheral requests and the BIOS.

#### BIOS Device Service Routines

BIOS Device Service Routines (DSRs) handle software generated interrupts. These interrupts can be generated either by the BIOS, DOS, MS Windows\*, or the application software. Each interrupt number provides a device service with many sub-functions below it. The function number desired for a particular interrupt is placed in the AH register and any other information required is placed in the remaining registers.

In an embedded PC BIOS, depending on the hardware, specific functions can be excluded to reduce the size of the BIOS if not needed. Obviously there would be a tradeoff with off-the-shelf software compatibility.

If power management is needed, there is an Advanced Power Management (APM) specification that defines functions for the BIOS. APM defines five modes of operation; Full On, APM Enabled, APM Standby, APM Suspend, and Off.

**Full On:** No system power management is being performed. All devices on.

**APM Enabled:** System is operating but power management is active. System clocks may be slowed or disabled and unused devices may not be powered.

**APM Standby:** After a short period with no activity, Standby is entered. Most power management features are active. The current operating parameters are retained, allowing rapid recovery to the APM Enabled state when activity resumes.

**APM Suspend:** After a long period with no activity, Suspend is entered. All power management functions are active for minimal power consumption (clocks stopped, etc.). The current operating state is saved, resulting in a slow recovery to the Enabled state.

**Off:** System power supply is off. Operational parameters are not stored. A full system reset is performed before reentering the Full On state.

Currently Microsoft DOS and Microsoft Windows\* have the ability to use these features.

The following table is a comparison of third party vendor BIOSs.

Features	Phoenix Technologies	Award Software	System Soft	AMI	General Software	Eurosoft	Annabooks	USA Teknik
PCMCIA	Yes	Yes	Yes	Yes	Planned	Planned	Planned	Yes
FFS/FTL	Yes	Yes	Yes	Yes	Q1 95	Yes	No	Yes
APM	Yes	Yes	Yes	Yes	No	Yes	No	Yes
Min Size	12KB ROM	64KB ROM	N/A	64KB ROM 1MB RAM	8KB ROM 4KB RAM	N/A	48KB ROM 4KB RAM	N/A
Free Source	Optional	Optional	No	Optional	Yes	Optional	Yes	Partial
Remote Floppy	No	No	No	No	Yes	Yes	Yes	Yes
Video/KBD to Serial	No	No	Yes	Yes	Yes	Yes	Yes	Yes
OEM Configurable	Yes	Yes	No	No	Yes	Yes	Yes	Yes
Debugger	Yes	Yes	No	Paradigm	Yes + SSI	Yes	Yes	No

Table 3. BIOS Comparison

#### Disk Operating Systems (DOS)

The DOS operating system offers functions for I/O communication, floppy/hard disk, video, keyboard, program handling, memory management, and network support. DOS consists of many functions that are available to the embedded user. These functions are out of the scope of this paper and are found in several books listed in the Reference section.

Two companies that have written their own version of DOS specifically for embedded designs are Datalight and General Software. Both are compatible with a version of Microsoft DOS. Microsoft offers both a ROM version and a disk version of DOS. The Microsoft DOS is distributed through Annabooks.

Generally no modifications need to be made to the DOS since it is not hardware dependent like the BIOS. Many vendors bundle a mini-command.com with an approximate size of 10K bytes if size is an issue. Below is a list of the DOS vendors:

	General Software Embedded DOS*	Microsoft MS DOS ROM	Datalight 6.0 ROM DOS*
MS DOS Compatible	MS6.22 Features	MS3.3, MS5.0, MS6.X	MS6.2
Support APM	No	Yes MS5.0, MS6.X	Yes
ROMable	Yes	Yes	Yes
Size Min	32KB ROM 8KB RAM	MS3.3 45K MS5.0 61K ROM 256K RAM	39KB ROM 8KB RAM
Source	Available	Parts Available	Parts Included
OEM Configurable	Yes	Yes	Yes
Remote Disk via Serial	Yes	No	Yes
Option Disk Compression	N/A	Double Space* (6.22)	Stacker*

\*Other Brands and Names are the property of their respective owners.

			Optional
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Table 4. DOS Comparison

Another feature for increased performance and memory savings is eXecute In Place (XIP). It allows code to be executed directly from where it is stored. MS DOS\* in ROM ROM Windows 3.1\*, and GEOWORKS supports XIP.

### Graphical User Interface (GUI)

MS ROM Windows\* and GEOWORKS exist today if a Graphical User Interface is a requirement.

### Microsoft ROM Windows

Microsoft ROM Windows\* is very similar to the disk based version found on many desktops. The Microsoft Windows\* 3.1 ROM Development Kit (RDK) is available from Annabooks. The ROM based Windows contains a small amount of XIP code in the real mode address space and a large amount of XIP code above the 1MB address region. The disk based Windows contains no XIP code since all code is loaded from disk. Two modes of operation exist for ROM Windows, standard mode and enhanced mode. In standard mode Windows, shell programs, applets, fonts and other Windows resources all execute from the XIP memory. In Enhanced mode, Windows executes both from RAM and XIP memory.

Windows Mode	Min RAM	Min XIP	Min Disk Space
Standard	1MB	2MB	0MB
Enhanced	2MB	3MB	2MB

Table 5. ROM Windows requirements

The XIP memory can be provided with Flash Memory like the 28F016 or 28F008. If this is the case, a software utility will be needed to load the ROM Windows files into the flash. Since disk space is a requirement for enhanced mode, a flash file system software is required. The appnote "Implementing Mobile Intel486™ SX CPU PC Designs Using FlashFile™ Components" (order number 292149-001) goes into great detail on the hardware and software specifics for a Microsoft ROM Windows\*/Microsoft DOS\* in ROM based design using the Microsoft Windows\* 3.1 RDK.

### GEOWORKS

The GEOS\* System Software by Geoworks is a windowed based OS that is targeted to consumer based products. It executes only in real mode and uses XIP windows to access programs. It is a very compact OS with many OEM configuration features. The GEOS OS requires a BIOS and a DOS to function.

### Flash File Systems

There are two methods of implementing a file system in flash, one is the Flash File System (FFS) developed by Microsoft and the other is the File Translation Layer (FTL) that is supported by several companies.

FFS uses linked lists to keep track of files. The system can be broken down into three parts. First is the File System Redirector (FSR) which intercepts DOS disk operations from an application and translates them before sending them on to the File System Driver (FSD). Second is the File System Driver, which accepts operations from the FSR. The FSD organizes the data according to the storage architecture and passes low level commands like Read, Write, Copy, and Erase to the Device Driver. Finally the Device Driver accepts low level commands from the FSD and interfaces to the hardware.

The FFS makes the flash drive appear like a network drive to the system. Network drives do not use the standard BIOS function call INT13 to talk to the disk. This causes some problems for applications that perform direct calls to the INT13 BIOS function as they will not be supported by FFS.



FFS also requires an ISA sliding window to access the flash. The window size can be 8KB, 16KB or 32KB and located in the C0000H to DFFFFH address range..

FTL is a sector based file system, like DOS, which allows the software to treat the flash as a normal sector based drive with a sector size of 512 bytes. When modifying a sector, the software remaps the sectors or block to a free area of flash while invalidating the old area. The location of the remapped block is also recorded. Typically an FTL implementation is approximately 20K in size. FTL is also defined in the PCMCIA specification. Depending on the hardware, three methods are available for implementing FTL.

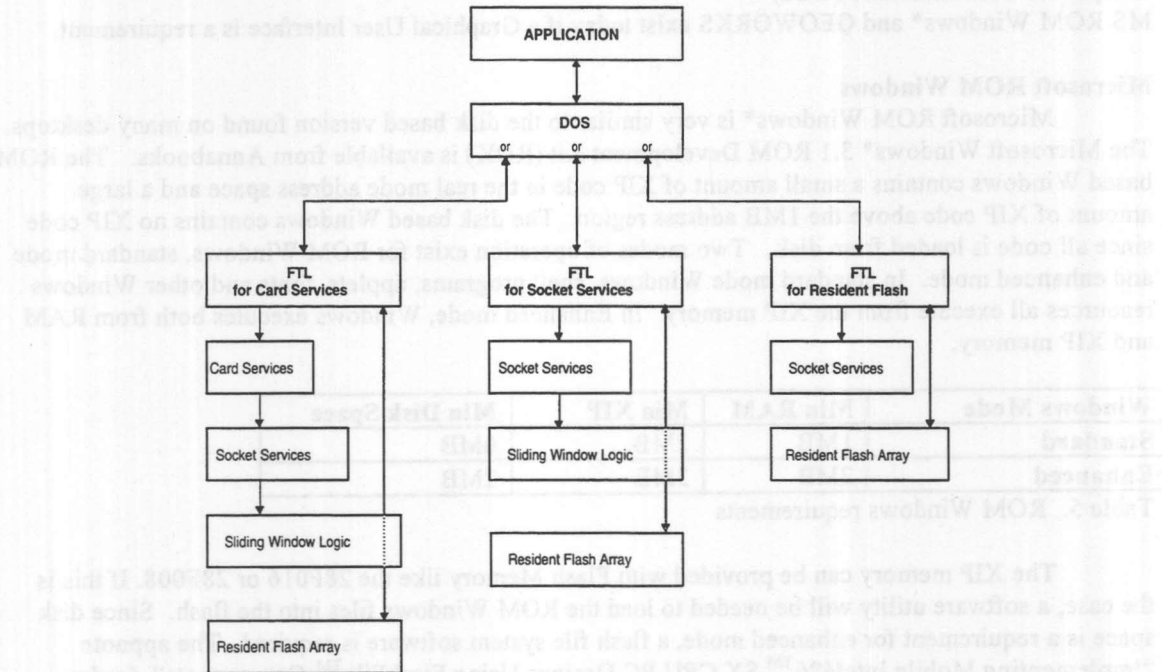


Figure 2. FTL Implementations

The first method uses PCMCIA and requires Card Services, Socket Services, and ISA Sliding Window logic (PCMCIA Controller). The second method requires Socket Services, and ISA Sliding Window logic (PLD) for the FTL to communicate to the flash array. The third method uses protected mode to access the flash and does not require an ISA sliding window. It is also able to communicate directly to the flash because of integrated flash drivers for the 28F008SA, 28F016SA, etc. FTL implementations intercept INT13 BIOS calls allowing for a higher level of compatibility with application software. Below is a list of various flash file system vendors:

	Microsoft FFS	SCM Microsystems	Datalight Cardtrick	M-Systems True FFS
Type	FFS	FTL	FTL/FFS	FTL
Device Driver	Yes	Yes	Yes	Yes
BIOS Extension	No	Yes	Yes	Yes

Table 6. FTL Comparison

## EMBEDDED PC HARDWARE CONSIDERATIONS

### Intel Architecture Processor

For full PC compatibility an i386™ processor with an 82C206 peripheral chipset provides basic PC compatibility. The 206 includes the 8259, 8237, 8254 and in some cases the RTC. The 206

is available from a number of vendors including Siemens SAB82C206, and PicoPower PT82C206F-LV. In addition, a chipset for DRAM, and ISA bus, is also required like the PicoPower PT86C378, or Opti 82C283. A one device solution with many of the above features (206 + DRAM + ISA) includes the Western Digital WD8110LV, the Chips and Technology F82C836, or the Samsung KS82C388A chipsets.

The Intel386™ EX processor embedded processor is a highly integrated 386 core with both PC and embedded peripherals. The Intel386 EX processor has a 26-bit address bus providing a 64MB address space. The interrupt controller, timers, DMA channels, and serial ports are all PC-AT compatible. The embedded functionality of the Intel386 EX processor consists of a synchronous serial port, DRAM refresh control, chip selects, power management, I/O ports, a watchdog timer, and a JTAG interface. The Intel386 EX processor alone can run a variety of BIOSs and DOSs. Implementing MS Windows\* on the EX will require a keyboard controller, real time clock, video controller, and a DRAM controller.

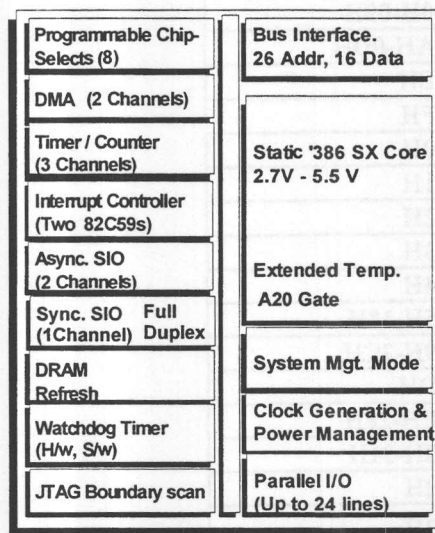


Figure 3. Intel386™ EX Block Diagram

The Intel386 EX Processor Point of Sale reference design is a good example of an embedded design that supports MS Windows\*.

### Display

If system display is required, several possibilities exist with varying degrees of PC support. The standard PC displays consist of Monochrome, CGA, EGA, and VGA. The VGA controller is the most widely available due to the PC market. VGA controllers exist for CRTs or LCDs or both simultaneously.

If a CRT display is required, a VGA controller is the most widely available with resolutions ranging from 640x480 to 1024x768. VGA controllers are backwards compatible thereby providing all of the PC display standards. A VGA BIOS is required for controller initialization and video functions. The size of the VGA BIOS is typically 32K. Possible tradeoffs include, leaving a video controller out of a design if no display is required. If only a text display is required, the display can be rerouted through the serial port or a small LCD single line character display can be added. A full LCD controller can also provide VGA resolution. Below are the PC compatible video modes that have PC software support:

Display	ROM	Colors	Resolution	RAM	Mem Address
MDA	Integrated in Sys BIOS	None	Char only	4K	B0000-B0FFF
HGC	Integrated in Sys BIOS	None	720x348	64K	B0000-BFFFF

\*Other Brands and Names are the property of their respective owners.

CGA	Integrated in Sys BIOS	16	640x200	16K	B8000-BFFFF
EGA	16K C0000H-C3FFF	64	640x350	64K-256K	A0000-BFFFF
VGA	32K C0000H-C7FFF	256K	720x480	256K	A0000-BFFFF
Super VGA	32K C0000H-C7FFF	256K	1024x768	512K-1MB	A0000-BFFFF

Table 7. PC Video Modes

## RTC

In the PC architecture the Real Time Clock contains a battery clock and CMOS RAM. The clock keeps time after power has been removed and also stores the system configuration in CMOS RAM. If the system is never to be powered off, then an RTC may not be required. If the system is not expandable, then the configuration information can be stored in ROM.

CMOS RAM Function	RAM Locations
Time/Date	00H-09H
RTC Control Regs	0AH-0DH
Diagnostic Byte	0EH
Reset Code Byte	0FH
Diskette Type	10H
Reserved	11H
Hard Disk Type	12H
Reserved	13H
Equipment Installed Byte	14H
Base & Extended Memory	15H-18H
Reserved	19H-2CH
Additional Flags	2DH
Checksum Value	2EH-2FH
Memory above 1MB	30H-31H
Century	32H
System Information	33H
Reserved	34H-3FH

The original RTC used in the PC AT was a Motorola MC146818. Now several manufacturers supply equivalent products like Dallas Semiconductors DS1287 and BenchMarq. The RTC contains 64 bytes of CMOS RAM that are accessed using two I/O locations port 70 and 71. Port 70 is the address register and port 71 is the data register. Valid address values are 0 to 3FH for 64 CMOS locations. The first 10 locations are used by the RTC to update the time and date, the next four locations are control registers for the RTC, and the remaining 50 locations are used to store system configuration.

The Reset Code Byte(0FH) was originally used in the PC-AT to allow the 80286 processor to return from protected mode to real mode by using the processor reset. This byte would indicate why the processor was reset and has several possible values:

- 00H Normal power up reset or <CTRL> <ALT> <DEL> reset.
- 04H Skip POST
- 05H Skip POST, preserve memory, send an EOI to the Interrupt controller, and then jump to reset vector 0040:0067. .
- 09H Block move return
- 0AH Jump to reset vector 0040:0067 without issuing EOI.

The location 0040:0067 contains the address where Real Mode execution should resume. On a Intel386™ processor or Intel486™ processor based system the switch from protected to real mode can



be made without resetting the processor, instead the Protected Enable(PE) bit in the Processors MSW register can be disabled. Some BIOSs allow this selection.

If the design does not require a real time clock then it is possible to use the PE bit to switch from protected mode to real mode. To maintain compatibility the BIOS can be hard coded with the hardware configuration. If the design requires MS-DOS\* or MS Windows\* than an RTC is a requirement.

#### Keyboard or Keypad

If data or user entry is not required a keyboard controller like the Intel8242PC/WA/WB is not required. For development purposes the data or user entry can be temporarily rerouted through the serial port for debug. MS DOS\* and MS Windows\* both require a PC standard keyboard controller and keyboard, although for limited data entry a keypad may suffice. This requires both non-standard hardware(keyboard scanner) and software (scanner driver).

#### Memory

Memory size is dependent on the application. Typically the BIOS and DOS will require 10K of RAM with 2K for the interrupt vectors. MS DOS\* requires a minimum of 256K while MS Windows\* requires 2MB.

FFFFFH	64KB BIOS
F0000H	64KB DOS
E0000H	16KB Windows Stub
DC000H	24KB FTL
D6000H	ROM Extensions
CA000H	8KB ISA Window
C8000H	32KB VGA BIOS
C0000H	128K VGA Mem
A0000H	640KB DRAM
005FFH	BIOS/DOS Data
002FFH	Interrupt Vectors
00000H	

#### Storage

There are several types of media for data storage and include Hard disk, floppy, PCMCIA, Flash, or ROM. It should be determined if the media need read, or read/write capability. Storage requirements depend on the amount of data to be stored, size constraints, power, reliability, removability, and other factors. Below is a partial table of storage possibilities:

Media	R/W	Storage	Removable
Hard Disk	R/W	5MB-1GB	No

PCMCIA	R/W	10MB-40MB	Yes
Flash Array	R/W		No
Floppy	R/W	360K-2.88MB	Yes
ROM	R		No
CD-ROM	R	Huge	Yes

### Boot Block Flash/ROM

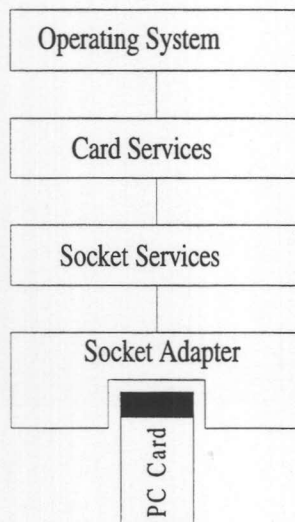
Boot block Flash or ROM is used for storing the BIOS. The boot block flash has the advantage of programming the BIOS after the board has been manufactured, thus allowing longer software development time and field upgrades. To control the BIOS programming on the flash, a flash utility is typically placed in the boot block of the flash prior to placement on the board. An example of this is the EV386EX evaluation board which comes with a flash utility call iBOOTLDR. Source code for this program is available on the Intel BBS (916-356-3600).

### Flash Array

A Flash array allows for data storage and is located above the 1MB real mode address region or can be paged with ISA Sliding Window logic. Access to the flash can be accomplished in either protected mode or virtual mode. This memory can be used to store ROM Windows or a flash file system.

### PCMCIA

The Personal Computer Memory Card International Association (PCMCIA) specification defines both memory and I/O cards. The cards, referred to as PC cards, are approximately 3.5" by 2" with a thickness that can vary from 3.3mm to 10.5mm depending on the type. These PC cards are ideal for portable embedded devices or embedded instruments. They allow users to upgrade software, increase data storage, and add I/O devices. To interface these PC cards to an embedded design, a PCMCIA controller is required as well as a software interface. Below is the software model.

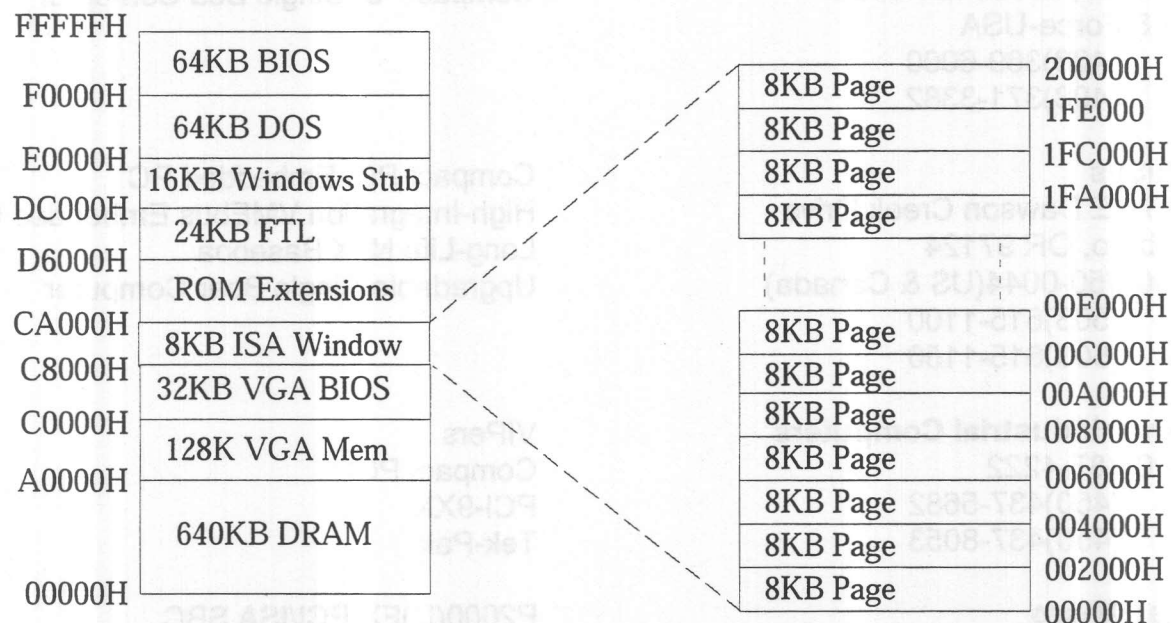


A variety of controllers exist from companies like Cirrus, Databook, and Vadem. Most interface to either the ISA, EISA, or PCI bus. Most controllers are based on the Intel 82365SL which is also compliant with the Exchangeable Card Architecture (ExCA™) or QuickSwap™ specifications. QuickSwap has replaced ExCA as the standard for Intel Architecture. QuickSwap guarantees that a minimum hardware and software interface exists in the system. This allows the PC architecture to have the ability to communicate with a wide variety of cards. Software drivers like Socket Services and Card Services are required for the interface to operate correctly.

The Socket Services provides a standardized interface to the socket hardware, but is independent of the hardware implementation. This software resides in the ROM BIOS and provides a variety of functions. The Card Services provides a higher level of functions that applications or operating systems can call on for interfacing to the card. To be fully compatible with most cards, the system software must support PCMCIA version 2.1 and QuickSwap. If the system is using flash memory, the drivers may also want to support the Memory Technology Drivers interface. This provides future support for updates when new types of Flash memory cards appear on the market. It is also possible to use a flash file system with a flash card.

### ISA Sliding Window

The ISA sliding window allows real mode programs access to memory above the 1MB address space. Typically this window is built around the LIM (Lotus-Intel-Microsoft) Expanded Memory Specification (EMS). Special hardware and software is required to support EMS. The ISA sliding window can range from 4KB to 64KB in size and there can also be multiple windows in real mode.



Flash file systems can use a window like this to access a flash array.

### CONCLUSION

There are a variety of options available for the embedded PC designer today. Selecting and understanding the correct configuration is very important to a successful design. Issues like PC compatibility, storage, memory map, hardware requirements are just some of the factors involved. The subjects covered in this paper were designed to provide you with the basic building blocks to design an embedded PC.



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#### **Ampro Computers**

4757 Hellyer Avenue  
San Jose, CA  
USA 95138  
1-800-966-5200(USA)  
Tel: (408)360-0200  
Fax: (408)360-0222

#### **Force Computers**

2001 Logic Drive  
San Jose, CA 95124-3468  
1-888-Force-USA  
Tel: (408)369-6000  
Fax: (408)371-3382

#### **RadiSys**

5445 NE Dawson Creek Drive  
Hillsboro, OR 97124  
1-800-950-0044(US & Canada)  
Tel: (503)615-1100  
Fax: (503)615-1150

#### **Teknor Industrial Computers**

1-800-387-4222  
Tel: (450)437-5682  
Fax: (450)437-8053

#### **Texas Micro**

5959 Corporate Drive  
Houston, TX 77036  
1-800-627-8700  
Fax: (713)541-8226

#### **VMIC**

12090 S. Memorial Parkway  
Huntsville, AL 35803  
1-800-322-3616  
Tel: (256)880-0444  
Fax: (256)882-0859

#### **Ziatech**

1050 Southwood Drive  
San Luis Obispo, CA 93401  
Tel: (805)541-0488  
Fax: (805)541-5088

### **Product**

CoreModule/P5i  
Little Board/P5i  
Little Board/P5e

CompactPCI Systems  
Rackmount Workstations  
CompactPCI Single Board Computer

Compact PCI Embedded PC  
High-Integration VMEbus Embedded Computer  
Long-Life NLX Baseboard  
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VIPers  
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**VenturCom**

Five Cambridge Center  
Cambridge, MA 02142  
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1010 Atlantic Avenue  
Alameda, CA 94501 USA  
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Tel: (214) 231-2216

**Pentium<sup>®</sup> II Processor Mobile Module:  
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# Embedded Module Connector 2 at 266 MHz (EMC-2) Design Guide

Application Note

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*November 1998*

Order Number: 273212-001

# Pentium® II Processor Mobile Module: Embedded Module Connector 2 at 266 MHz (EMC-2) Design Guide

Application Note

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### **Revision History**

Revision	Date	Notes
001	October 1998	First release of this document.





**EMC-2** refers to the Embedded Module Connector-2. This module is identical to the Intel® Pentium® II Processor Mobile Module Connector (MMC-2). A complete description of this module is located in the *Intel® Pentium® II Processor Mobile Module: Mobile Module Connector 2 (MMC-2)* datasheet (<http://developer.intel.com/design/mobile/datashts>).

**Intel 440BX AGPset** refers to both the 82443 BX Host Bridge Controller and the 82371EB PCI ISA IDE Xcelerator.

**82443BX** refers to the Intel 82443BX Host Bridge Controller.

**PIIX4E** refers to the Intel 82371EB PCI ISA IDE Xcelerator.

**Design Features** are items that allow the designer to fully use the capabilities of the mobile Pentium® II processor and the Intel 440BX AGPset.

**Design Checklists** are items which provide recommendations for designing an EMC-2-based platform.

**Design Considerations** are items that should be considered but may not be applicable to your design.

## 1.2

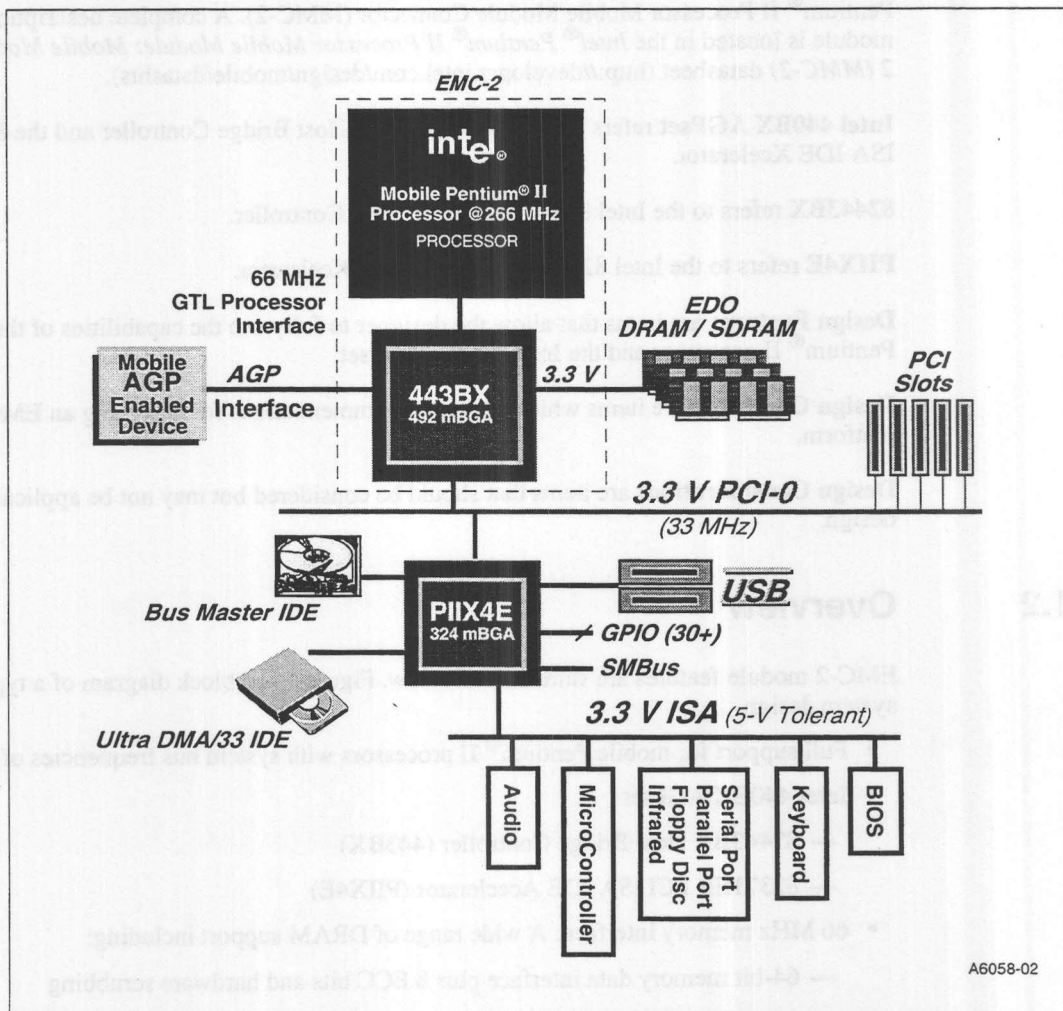
### Overview

EMC-2 module features are summarized below. Figure 1 is a block diagram of a typical EMC-2 system design.

- Full support for mobile Pentium® II processors with system bus frequencies of 66 MHz
- Intel 440BX AGPset
  - 82443BX Host Bridge Controller (443BX)
  - 82371EB PCI ISA IDE Accelerator (PIIX4E)
- 66 MHz memory interface: A wide range of DRAM support including:
  - 64-bit memory data interface plus 8 ECC bits and hardware scrubbing
  - 60 ns EDO DRAM and 66 MHz SDRAM support
  - 16 Mbit and 64 Mbit DRAM technologies
- 5 PCI masters
  - PCI Specification Rev 2.1 Compliant

- Accelerated Graphics Port (AGP) Slot:
  - AGP Interface Specification Revision 1.0 compliant
  - AGP - 66/133 MHz, 3.3-V device support
- Integrated IDE controller with Ultra DMA/33 support
  - PIO Mode 4 transfers
  - PCI IDE bus master support
- Integrated Universal Serial Bus (USB) controller with two USB ports
- Integrated System Power Management support

Figure 1. EMC-2/440BX AGPset System Block Diagram



## 1.3 Related Documents

Table 1. Related Intel Documents

Document	Order Number
Intel® Pentium® II Processor Mobile Module (MMC-2) datasheet	243668
Mobile Pentium® II Processor Specification Update	243887
Intel® Pentium® II Processor Mobile Module: Mobile Module Connector 2 (MMC-2) datasheet	243668
Intel® 440BX AGPset: 82443BX Host Bridge/Controller datasheet	290633
PIIX4 Universal Serial Bus Design Guide	NDA†
CK97 Clock Synthesizer Design Guidelines application note	243867
Intel® 82371EB PCI-to-ISA/IDE Xcelerator (PIIX4E) Specification Update	290635
Intel® 82371AB PCI-to-ISA/IDE Xcelerator (PIIX4) datasheet	290562
Intel® Architecture Software Developer's Manual, Volume 1; Basic Architecture	243190
Intel® Architecture Software Developer's Manual, Volume 2; Instruction Set Reference	243191
Intel® Architecture Software Developer's Manual, Volume 3; System Programming Guide	243192
Intel® Architecture MMX™ Technology Developer's Guide	243006
AP-485 Intel Processor Identification and the CPUID Instruction application note	241618
AP-585 Pentium® II Processor GTL + Guidelines application note	243330
AP-586 Pentium® II Processor Thermal Design Guidelines application note	243331
AP-587 Slot 1 Processor Power Distribution Guidelines application note	243332
AP-589 Slot 1 Processor EMI Overview application note	243334

† NDA documents are only available through an Intel Field Sales Representative.

Table 2. Related Specifications

Document	URL/Contact
PCI Local Bus Specification, Revision 2.1	<a href="http://www.pcisig.com/specs.html">http://www.pcisig.com/specs.html</a>
Universal Serial Bus Specification, Revision 1.0	<a href="http://www.usb.org/usb/developers/index.html">http://www.usb.org/usb/developers/index.html</a>
AGP Interface Specification, Revision 1.0	<a href="http://www.agpforum.org/index.htm">http://www.agpforum.org/index.htm</a>
AGP Platform Design Guide, Revision 1.1A	<a href="http://www.agpforum.org/index.htm">http://www.agpforum.org/index.htm</a>
Information Technology – AT Attachment with Packet Interface Extension (ATA/ATAPI-4)	<a href="ftp://fission.dt.wdc.com/pub/standards/">ftp://fission.dt.wdc.com/pub/standards/</a>
System Management Bus Specification	<a href="http://www.sbs-forum.org/">http://www.sbs-forum.org/</a>
66MHz Unbuffered SDRAM 64-bit (Non-ECC/Parity) 144-pin SO-DIMM Specification, Revision 1.0	Contact an Intel Field Sales Representative



## 2.0 Design Features

### 2.1 Mobile Pentium® II Processor

The mobile Pentium II processor is the first of the Pentium II processor family to be offered for the embedded platform. It is offered at 266 MHz with a PSB speed of 66 MHz. It consists of a mobile Pentium II processor core with an integrated second-level cache controller and a 64-bit high-performance host bus. The mobile Pentium II processor has a private second-level cache bus that allows a high-performance 64-bit wide cache subsystem to be gluelessly implemented using a Tag RAM and two BSRAM devices. The mobile Pentium II processor can cache up to 512 Mbytes of memory using 512 Kbytes of BSRAM. The private second level cache bus complements the host bus by providing critical data faster, improving performance, and reducing total system power consumption. The mobile Pentium II processor's 64-bit wide Low Power GTL+ host bus is compatible with the 440BX AGPset and provides a glueless, point-to-point interface for an I/O bridge and memory controller.

### 2.2 Intel® 440BX AGPset

The Intel® 440BX AGPset is based on the Pentium II processor architecture. It interfaces with the mobile Pentium II processor's system bus at 66 MHz. Along with its Host-to-PCI bridge interface, the 82443BX host bridge controller has been optimized with a 66 MHz SDRAM memory controller and data path unit. The 82443BX also features the Accelerated Graphics Port (AGP) interface. The 82443BX component includes the following functions and capabilities:

- 64-bit Low Power GTL+ based system data bus interface
- 32-bit system address bus support
- 64/72-bit main memory interface with optimized support for SDRAM
- 32-bit PCI bus interface with integrated PCI arbiter
- AGP interface with up to 133 MHz data transfer capability
- Extensive data buffering between all interfaces for high throughput and concurrent operations

Figure 1 shows a block diagram of a typical platform based on the 440BX AGPset. The 82443BX system bus interface supports a mobile Pentium II processor at a bus frequency of 66 MHz. The physical interface design is based on the Low Power GTL+ specification and is compatible with the Intel 440BX AGPset. The 440BX provides an optimized 72-bit DRAM interface (64-bit Data plus ECC). This interface supports 3.3-V DRAM technologies.

The 82443BX is designed to support the PIIX4E I/O bridge. The PIIX4E is a highly-integrated multifunctional component that supports the following functions and capabilities:

- PCI Revision 2.1 compliant PCI-to-ISA bridge with support for 33 MHz PCI operations
- ACPI Power Management support
- Enhanced DMA controller, interrupt controller and timer functions
- Integrated IDE controller with Ultra DMA/33 support
- USB host interface with support for two USB ports
- System Management Bus (SMB) with support for DIMM Serial Presence Detect

### 2.2.1 System Bus Interface

The 82443BX supports a maximum of 4 Gbytes of memory address space from the processor perspective. The largest address size is 32 bits. The 82443BX provides bus control signals and address paths for transfers between the processor bus, PCI bus, Accelerated Graphics Port and main memory. The 82443BX supports a 4-deep-in-order queue, which provides support for pipelining of up to four outstanding transaction requests on the system bus. The mobile Pentium® II processor supports a second-level cache size of 512 Kbytes with ECC. All cache-control logic is provided on the processor.

For system bus-to-PCI transfers, the addresses are either translated or directly forwarded on the PCI bus, depending on the PCI address space being accessed. When the access is to a PCI configuration space, the processor I/O cycle is mapped to a PCI configuration space cycle. When the access is to a PCI I/O or memory space, the processor address is passed without modification to the PCI bus. Certain memory address ranges are dedicated for a graphics memory address space. When this space or a portion of it is mapped to main DRAM, the address is translated by the AGP address remapping mechanism and the request is forwarded to the DRAM subsystem. A portion of the graphics aperture can be mapped on the AGP, and the corresponding system bus cycles accessing that range are forwarded to the AGP without any translation. The AGP address map defines other system bus cycles that are forwarded to the AGP.

### 2.2.2 DRAM Interface

The 82443BX integrates a main memory controller that supports a 64/72-bit DRAM interface which operates at 66 MHz. The integrated DRAM controller features include:

- 3.3-V interface
- Support for up to three double-sided SODIMMs
  - 8 Mbytes to 48 Mbytes using 16-Mbit technology
  - 192 Mbytes using 64-Mbit technology
- Support for ECC with hardware scrubbing

### 2.2.3 Accelerated Graphics Port Interface

The 82443BX supports an AGP interface. The AGP interface has a maximum theoretical transfer rate of ~532 Mbytes/s.

### 2.2.4 PCI Interface

The 82443BX PCI interface operates at 33 MHz, is Revision 2.1 compliant, and supports up to five external PCI bus masters in addition to the PIIX4E I/O bridge. The PCI interface is only 3.3-V. If the developer requires a 5-V interface, a level shifter implementation is recommended.

### 2.2.5 System Clocking

The 82443BX operates the system bus interface at 66 MHz, the PCI bus at 33 MHz and the AGP at a transfer rate of 66/133 MHz. The 82443BX clocking scheme uses an external clock synthesizer that produces reference clocks for the system bus and PCI interfaces. The 82443BX generates the AGP and DRAM clock signals. Please refer to the *CK97 Clock Synthesizer/Driver Specification* (order number 243867).

## 2.3 PCI ISA IDE Xcelerator (PIIX4E)

The PCI ISA IDE Xcelerator (PIIX4E) is a multi-function PCI device that implements a PCI-to-ISA bridge function, a PCI IDE function, a Universal Serial Bus host/hub function, and an Enhanced Power Management function. Because it is a PCI-to-ISA bridge, the PIIX4E integrates many common I/O functions found in ISA-based PC systems; a seven channel DMA Controller, two 82C59 Interrupt Controllers, an 8254 Timer/Counter, and a Real Time Clock. In addition to DMA Compatible transfers, each DMA channel also supports Type F transfers.

The PIIX4E contains full support for PC/PCI and Distributed DMA protocols that implement PCI-based DMA. The Interrupt Controller has edge or level sensitive programmable inputs. Chip select decoding is provided for a BIOS, Real Time Clock, Keyboard Controller, second external microcontroller, and two Programmable Chip Selects. The PIIX4E provides full Plug-and-Play compatibility. The PIIX4E can be configured as a subtractive decode bridge or as a positive decode bridge.

The PIIX4E supports two IDE connectors. This provides an interface for IDE/EIDE hard disks and CD-ROMs. Up to four IDE devices can be supported in Bus Master mode. The PIIX4E contains support for Ultra DMA/33 compatible synchronous DMA devices.

The PIIX4E contains a Universal Serial Bus (USB) host controller that is Universal Host Controller Interface (UHCI) compatible. The host controller's root hub has two programmable USB ports.

The PIIX4E supports Enhanced Power Management, including full clock control, device management for up to 14 devices, and suspend and resume logic with Power On Suspend, Suspend to RAM, or Suspend to Disk. The PIIX4E fully supports operating-system-directed power management according to the Advanced Configuration and Power Interface (ACPI) specification. The PIIX4E integrates both a System Management bus (SMBus) host and slave interface for serial communication with other devices.

For more information on the PIIX4E, please refer to the 82371AB *PCI-to-ISA/IDE Xcelerator (PIIX4)* datasheet (order number 290562) and the 82371EB *PCI-to-ISA/IDE Xcelerator (PIIX4E)* Specification Update (order number 290635).

## 3.0 Memory Guidelines

This section lists guidelines to be followed when routing the signal traces for the board design. The order in which signals are routed first and last will vary from designer to designer. Some designers prefer routing the clock signals first, while others prefer routing the high-speed bus signals first. Either order can be used, as long as the guidelines listed here are followed. When the guidelines listed here are not followed, it is very important to simulate the design. Even when the guidelines are followed, it is recommended that you simulate these signals for proper signal integrity, flight time and cross talk.

### 3.1 DRAM Interface Overview

The 82443BX integrates a main memory DRAM controller that supports a 64-bit DRAM array for embedded environments. The DRAM types supported are Synchronous (SDRAM) and Extended Data Out (EDO). The 82443BX does not support a mixture of SDRAM and EDO memory. The



82443BX DRAM interface runs at 66 MHz. The DRAM controller interface is fully configurable through a set of control registers. Complete descriptions of these registers are given in the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet.

The 443BX supports industry standard 64-bit wide 144-pin SODIMM modules with SDRAM or EDO DRAM devices. Both symmetric and asymmetric addressing is supported. For write operations of less than a Qword in size, the 443BX will either perform a byte-wide write cycle (non-ECC protected configuration) or a read-modify-write cycle by merging the write data on a byte basis with the previously read data (ECC or error correction configurations). The 82443BX requires 60 ns EDO DRAMs or SDRAM with CAS latency of 2 (CL2), and supports 1-and 2-row SODIMMs. The 82443BX provides refresh functionality with programmable rates (normal DRAM rate is 1 refresh/15.6  $\mu$ s). When using SDRAM the 82443BX can be configured via the paging policy register to keep multiple pages open within the memory array. Pages can be kept open in all rows of memory. When using two bank SDRAM devices in a particular row, up to two pages can be kept open within that row.

The DRAM interface of the 82443BX is configured by the DRAM control registers, DRAM timing register, SDRAM control register, bits in the NBXCFG register and the eight DRAM row boundary (DRB) registers. The DRAM configuration registers control the DRAM interface to select EDO or SDRAM, RAS timing, and CAS rates. The eight DRB registers define the size of each row in the memory array, enabling the 82443BX to assert the proper CSA[7:0]#, CSB[7:0]# pair for accesses to the array.

### 3.1.1 Pin Groups

The 82443BX has multiple copies of many of the signals interfacing to memory. However, the EMC-2/440BX AGPset only supports a single copy of the memory signals. See "Single Set DRAM Interface" on page 16 for more information. The interface consists of the following pins:

Multiple copies:

MAA[13:0], MAB[12:11,9:0]# and MAB[13, 10]  
CSA[7:0]#, CSB[7:0]#  
SRASA#, SRASB#  
SCASA#, SCASB#  
WEA#, WEB#  
DQMA[7:0], DQMB[5:1]

Single copies:

CKE[5:0] (for three SODIMM configuration)  
MD[63:0]  
MECC[7:0]  
GCKE (for four DIMM configuration)  
FENA (FET switch control for four DIMM configuration)

The CSA[7:0]#, CSB[7:0]# pins function as RAS# pins in the case of EDO DRAMs. The DQM pins function as CAS# pins in the case of EDO DRAMs. Two CS# lines are provided per row. These are functionally equivalent. The extra copy is provided for loading reasons. The two SRAS#, SCAS# and WE# pins are also functionally equivalent and each copy drives two rows of DRAM. Most pins use programmable strength output buffers. When a row contains 16-Mbit SDRAMs, MAA11 and MAB11# function as Bank Select lines. When a row contains 64-Mbit SDRAMs, MAA[12:0], MAB[12:11] function as Bank Addresses (BA[1:0], or Bank Selects). If the design



does not support ECC, you may leave MECC[7:0] unconnected. When the design supports ECC, perform simulations to determine which buffer strength is needed for loading requirements. This may require a BIOS change.

### 3.1.2 Single Set DRAM Interface

The following two sections explain which signals are used in embedded platforms. Note that MAB[13,10] are not active low because these address bits are used to define various SDRAM commands.

#### 3.1.2.1 EDO DRAM

Single copies used:

MAB[12:11,9:0]# and MAB[13,10]  
MD[63:0]  
MECC[7:0]  
RASA[5:0]#  
CASA[7:0]#  
WEA#

#### 3.1.2.2 SDRAM

Single copies used:

MAB[12:11,9:0]# and MAB[13,10]  
MD[63:0]  
MECC[7:0]  
CSA[5:0]#  
DQMA[7:0]  
CKE[5:0]  
SRASA#  
SCASA#  
WEA#

## 3.2 DRAM Layout Guidelines

**Note:** The following DRAM layout guidelines are intended for use with the 266 MHz EMC-2 platforms that will use *only* 66 MHz Host/SDRAM clock frequencies.

- The DRAM expansion socket for embedded applications is the 144-pin SODIMM.
- MAB[11]# should be connected to pin 106 of the SODIMM connector.
- MAB[12]# should be connected to pin 70 and pin 110 of the SODIMM connector.
- MAB[13] should be connected to pin 72 and pin 112 of the SODIMM connector.
- For onboard 64-Mbit SDRAM devices on the motherboard, MAB[11]# should be connected to A13/BA0 on the SDRAM device, and MAB[13] should be connected to A11 on the SDRAM device.

- The memory data bit traces may be byte-swapped to simplify board routing and minimize trace lengths. This should also be done for the data bits within the byte channel.
- Board impedance should be  $55 \Omega \pm 15\%$ .
- All resistors should be within 5% tolerance.
- Trace widths for memory signals should be 5 mil.
- Populate the furthest SODIMM first to avoid stub reflections.
- Any onboard memory should be put further away from the EMC-2 module than the SODIMM connectors.
- Place the on board DRAM connector, SODIMM connector, and EMC-2 connector as near to each other as possible.

### 3.2.1 SODIMM Connection - EDO DRAMS

Figures 2 and 3 show how to route the EMC-2/440BX DRAM interface to EDO DRAM.

Figure 2. EDO DRAM - One On-board Bank, Two SODIMMs

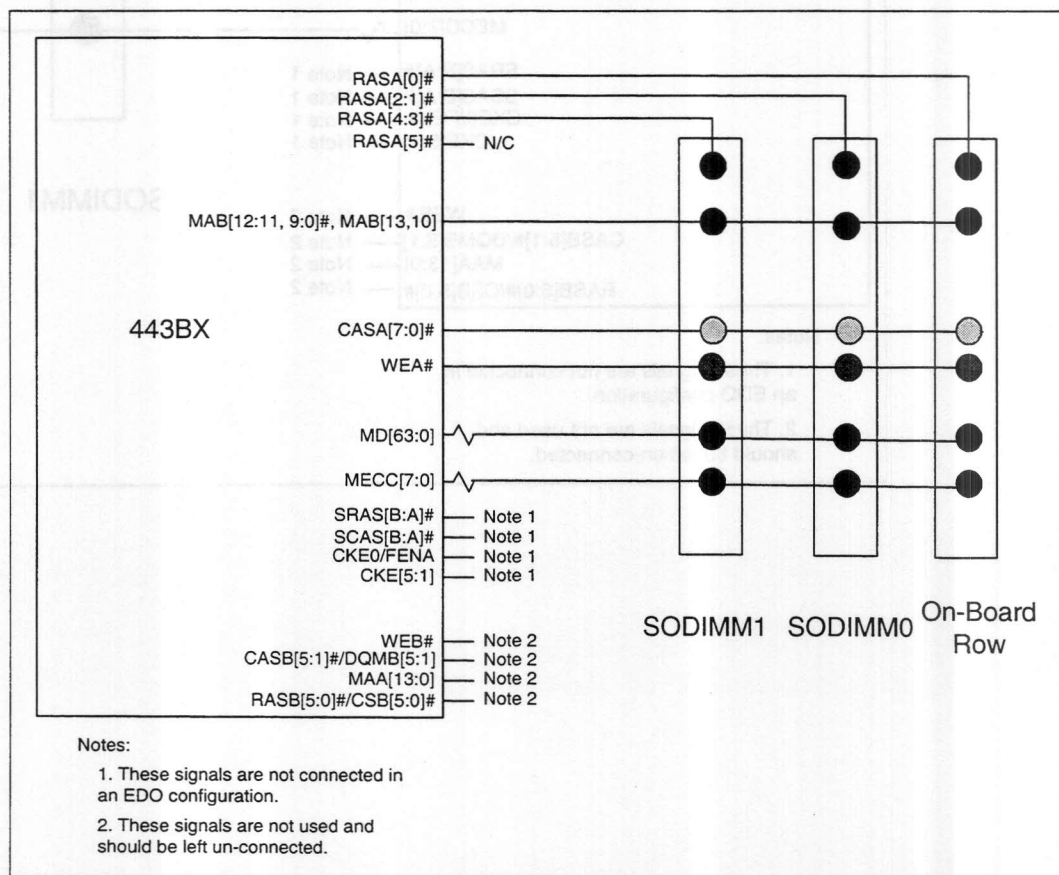


Figure 3. EDO DRAM - Two SODIMMs

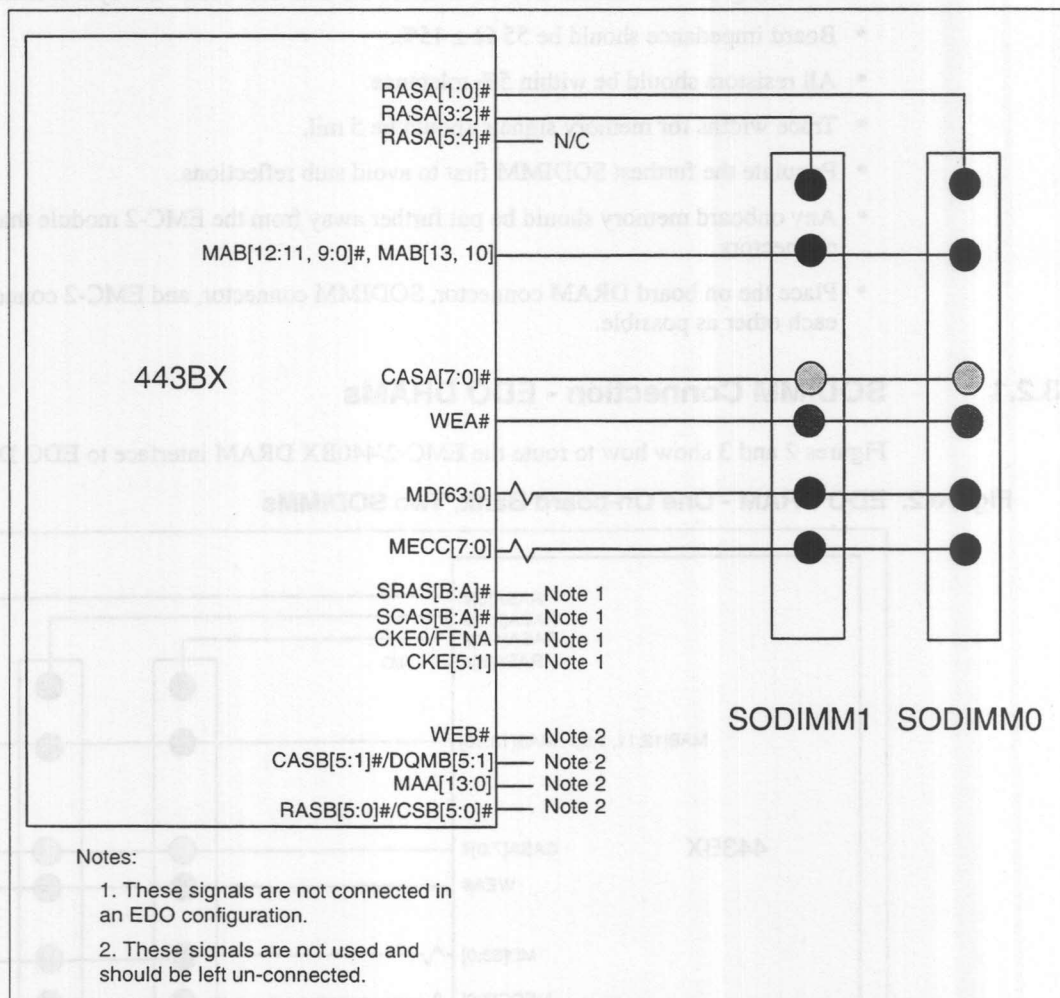
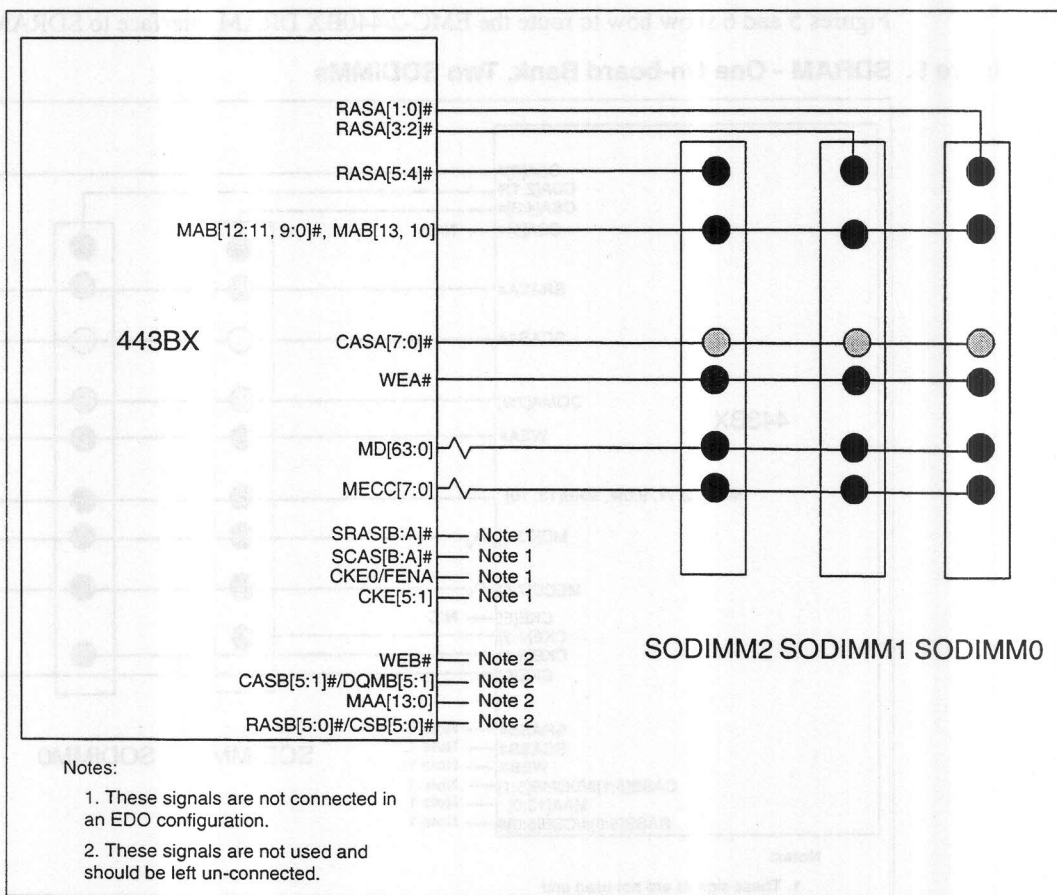


Figure 4. EDO DRAM - Three SODIMMs





### 3.2.2 SODIMM Connection - SDRAM

Figures 5 and 6 show how to route the EMC-2/440BX DRAM interface to SDRAM.

Figure 5. SDRAM - One On-board Bank, Two SODIMMs

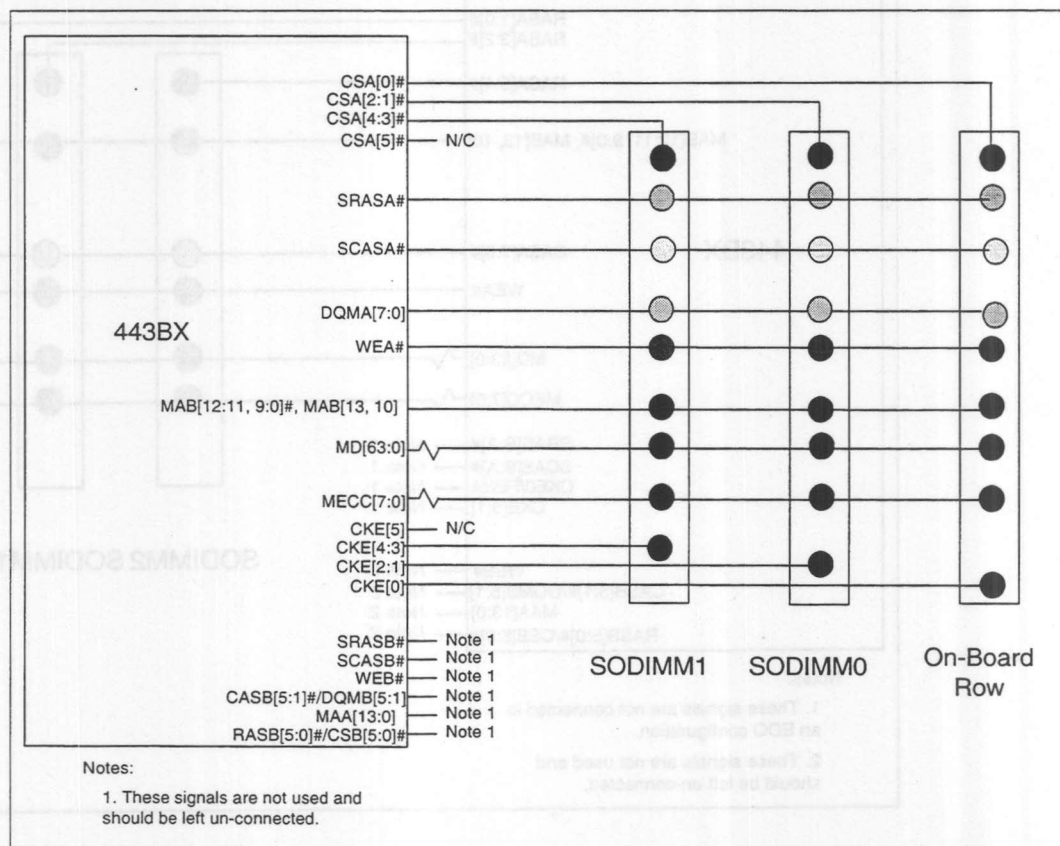


Figure 6. SDRAM - Two SODIMMs

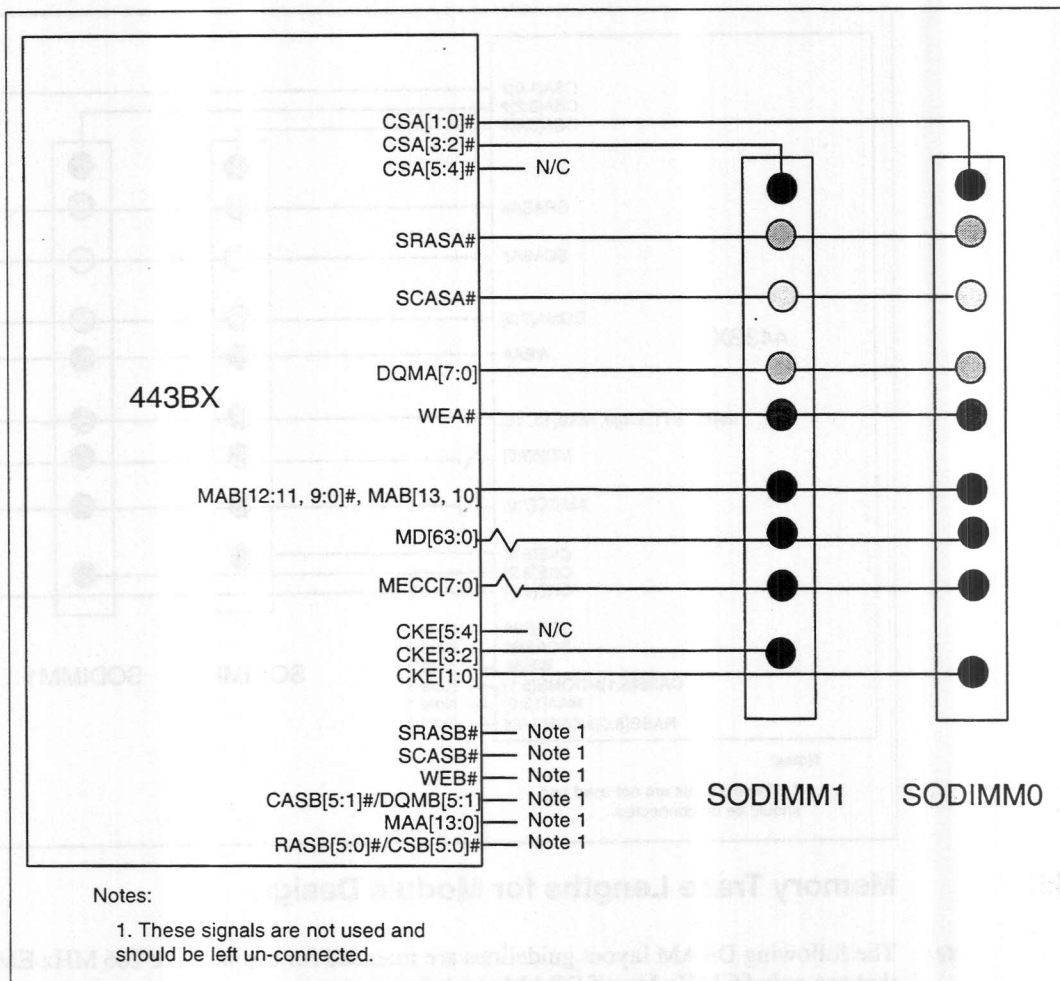
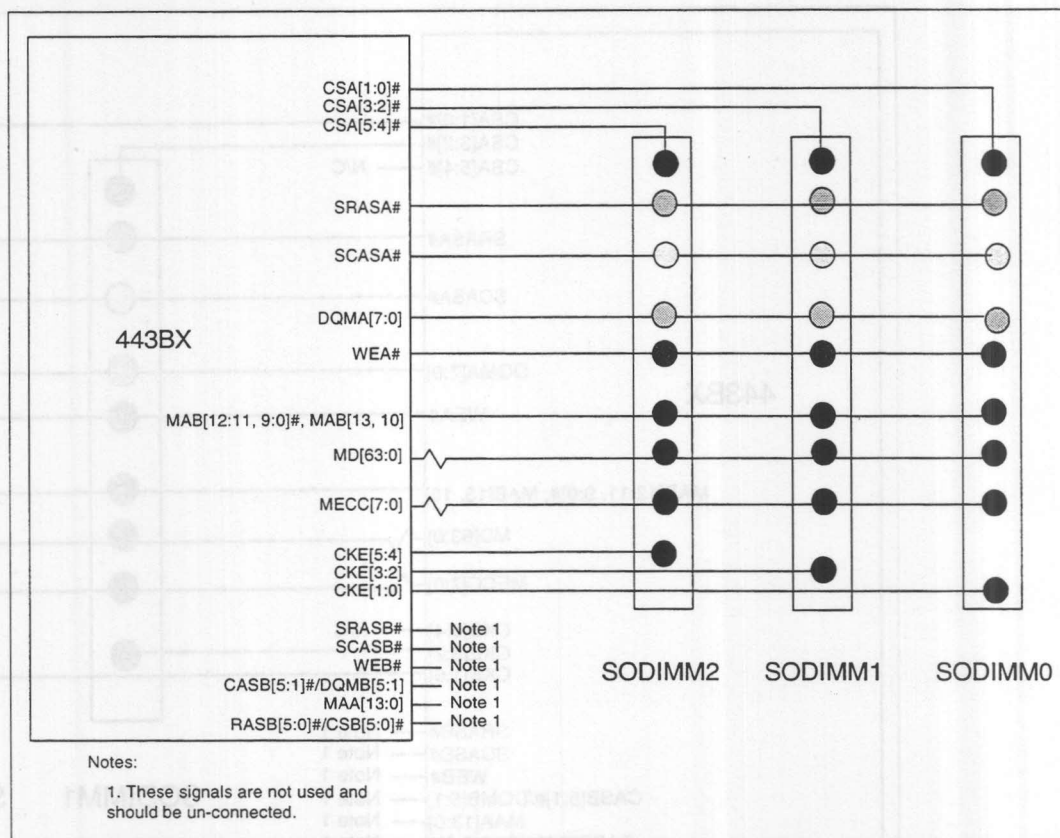


Figure 7. SDRAM - Three SODIMMs



### 3.2.3 Memory Trace Lengths for Module Design

**Note:** The following DRAM layout guidelines are intended for use with the 266 MHz EMC-2 platforms that use *only* 66 MHz Host/SDRAM clock frequencies.

Table 3 provides the minimum and maximum trace lengths to the SODIMM connector for each signal group (excluding clock) for each design. For the trace lengths of clocks, see "Clocking Guidelines" on page 25.

For memory configurations with on-board memory devices, signal traces should be routed as if there were a "phantom" connector on the board. The designer should follow the routing guidelines from the *66MHz Unbuffered SDRAM 64-bit (Non-ECC/Parity) 144-pin SO-DIMM Specification*, Revision 1.0, for the memory signals from the "phantom" connector to the on-board memory devices (refer to Table 2 on page 11). In other words, route the memory channel from the 82443BX to the position that SODIMM0 would occupy in your design following the given constraints, and route from that point onward according to the *66MHz Unbuffered SDRAM 64-bit (Non-ECC/Parity) 144-pin SO-DIMM Specification*.

Table 3. Trace Lengths for the DRAM Interface

Signal	Min. Length	Max. Length		Resistor (on System Electronics Board)
MAB[13:0]x, WEA#, SRASA#, SCASA#	0 inch	8.0 inch	203.2 mm	NONE
CKE[5:0]	0 inch	9.0 inch	228.6 mm	NONE
CSA/RASA[5:0]#	0 inch	9.0 inch	228.6 mm	NONE
CASA[7:0]#/DQMA[7:0]#	0 inch	9.0 inch	228.6 mm	NONE
MD[63:0], MECC[7:0]	0 inch	8.0 inch	203.2 mm	18 $\Omega$ $\pm$ 5%

### 3.3 SODIMM DRAM Organization

The 144-pin SODIMM (1" height) has a maximum capacity of eight devices and provides the following configuration possibilities (see Table 4) for SDRAM or EDO.

Table 4. SODIMM DRAM Organization

Technology	SODIMM Organization	Component Organization	Devices per Row	Mbyte per SODIMM
16 Mbit	1 M x 64 / S	1 M x 16	4	8 Mbyte
	2 M x 64 / D	1 M x 16	4	16 Mbyte
	2 M x 64 / S	2 M x 8	8	16 Mbyte
64 Mbit	2 M x 64 / S	2 M x 32	2	16 Mbyte
	4 M x 64 / D	2 M x 32	2	32 Mbyte
	4 M x 64 / S	4 M x 16	4	32 Mbyte
	8 M x 64 / D	4 M x 16	4	64 Mbyte
	8 M x 64 / S	8 M x 8	8	64 Mbyte

NOTE: "S" denotes single-sided SODIMMs. "D" denotes double-sided SODIMMs.

#### 3.3.1 64-Mbit SDRAM System Examples

Table 9 lists five system examples. Each example is based on using three SODIMM sockets or one on-board DRAM and two SODIMM sockets. The terms used in Table 9 are defined below:

144 SODIMM: Number of SODIMM sockets plus on-board DRAM  
Row: RAS[5:0]# or CS[5:0]# connection.  
Technology: DRAM technology 16 Mbit, 64 Mbit  
Density/Width: DRAM configuration 16 Mbit: 2 M x 8, or 1 M x 16  
64 Mbit: 8 M x 8, 4 M x 16, or 2 M x 32  
# Devices/Row: Number of DRAM components per row.



Table 5. System Examples for Supporting 64-Mbit SDRAM

144 SODIMM	Row	Technology	Density x Width	# Devices/Row	Mbytes per SODIMM
<b>Example #1</b>					
#1 or on-board	0	16 Mbit	2 M x 8	8	16 Mbytes
#2	1	16 Mbit	1 M x 16	4	8 Mbytes
	2	16 Mbit	1 M x 16	4	8 Mbytes
#3	3	16 Mbit	2 M x 8	8	16 Mbytes
Total	4			24	48 Mbytes
<b>Example #2</b>					
#1 or on-board	0	16 Mbit	2 M x 8	8	16 Mbytes
#2	1	16 Mbit	2 M x 8	8	16 Mbytes
#3	2	16 Mbit	2 M x 8	8	16 Mbytes
Total	3			24	48 Mbytes
<b>Example #3</b>					
#1 or on-board	0	16 Mbit	2 M x 8	8	16 Mbytes
#2	1	64 Mbit	8 M x 8	8	64 Mbytes
#3	2	64 Mbit	4 M x 16	4	32 Mbytes
Total	3			20	112 Mbytes
<b>Example #4</b>					
#1 or on-board	0	64 Mbit	8 M x 8	8	64 Mbytes
#2	1	64 Mbit	8 M x 8	8	64 Mbytes
#3	2	64 Mbit	8 M x 8	8	64 Mbytes
Total	3			24	192 Mbytes

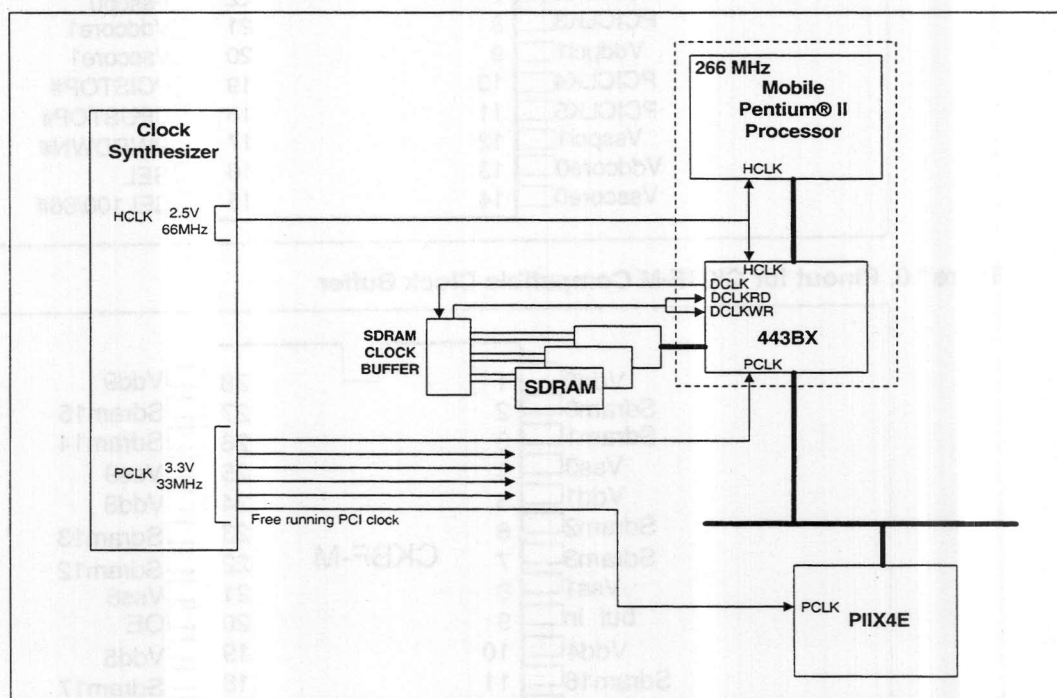
## 4.0 Clocking Guidelines

This section lists guidelines to be followed when routing the signal traces for the board design. The order in which signals are routed will vary from designer to designer. Some designers prefer routing all of the clock signals first, while others prefer routing the high-speed bus signals first. Either order can be used, as long as the guidelines listed here are followed. When the guidelines listed here are not followed, it is very important to simulate the design. Even when the guidelines are followed, it is recommended that you simulate signals for proper signal integrity, flight time and cross talk.

### 4.1 Clocking System Overview

This section provides guidelines and application information for clock layout in an EMC-2/440BX AGPset system. These guidelines are based on the HCLK, PCICLK and SDRAMCLK requirements and should be implemented along with the application instructions supplied by your clock chip vendor. Figure 8 shows the clock synthesizer connection to the processor, 443BX, and SDRAM when using an EMC-2 module.

Figure 8. Clock Connections to the EMC-2 Module



## 4.2 Clock Synthesizer Pinout and Specifications

A clock synthesizer that meets the *CK97 Clock Synthesizer Design Guidelines* (order number 243867) will meet the requirement for an EMC-2/440BX AGPset-based system. Table 8 on page 30 lists clock vendors that provide clock synthesizers which meet the *CK97 Clock Synthesizer Design Guidelines*.

**Note:** The CK100-M compatible clock synthesizer operates in multi-voltage mode. The processor clocks operate at 66 MHz at 2.5 V, and the PCI clocks operate at 33 MHz at 3.3 V. The CKBF-M compatible clock buffer provides clocks for SDRAM operating at 66 MHz at 3.3 V.

Figure 9. Pinout for CK100-M Compatible Clock Synthesizer

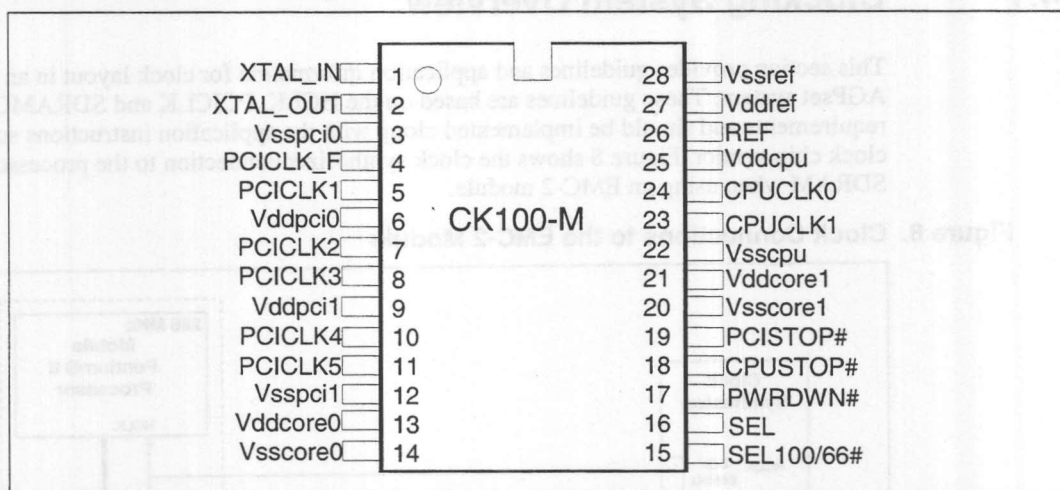
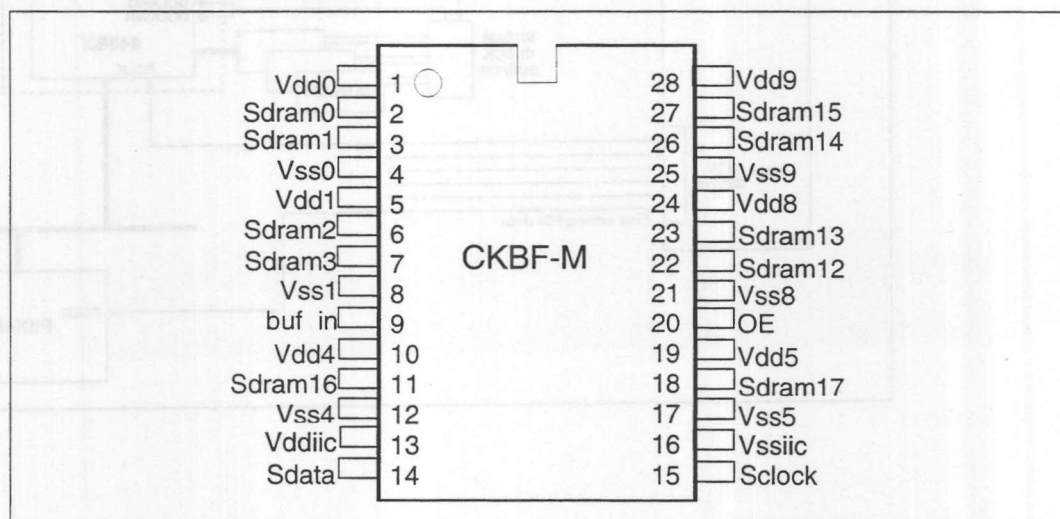


Figure 10. Pinout for CKBF-M Compatible Clock Buffer



### 4.3 Timing Guidelines

Trace lengths should be matched within clock signal groups to minimize skew between copies of the clocks. This applies to the HCLK-to-HCLK and the PCICLK-to-PCICLK clock trace lengths.

**Figure 11. Timing Specifications Layout**

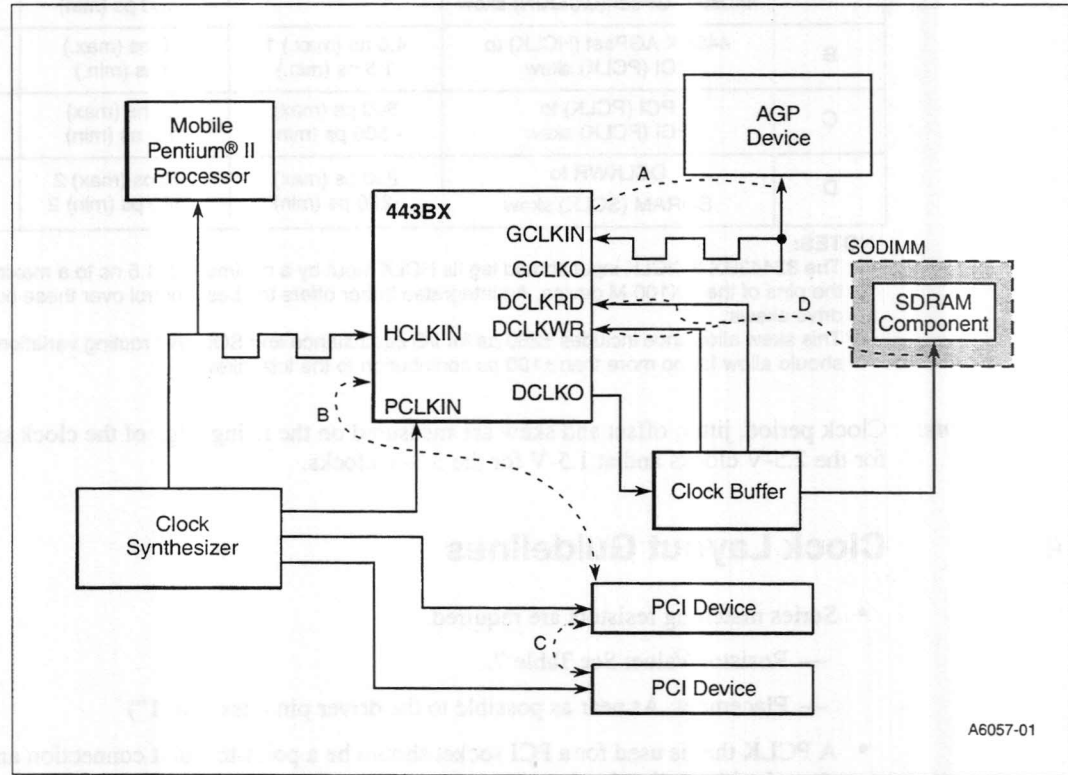


Figure 11 shows a simplified clocking layout for the timing specifications. The recommended trace lengths are given in the Note on page 28. See Table 6 for the clock skews.



Table 6. Timing Specifications for Maximum and Minimum Clock Skews

Symbol	Description	CK100-M Pin-to-Pin	Boards	Total
A	AGP device (GCLK) to 440BX AGPset (GCLKIN) skew	N/A	100 ps (max) - 100 ps (min)	100 ps (max) - 100 ps (min)
B	440BX AGPset (HCLK) to PCI (PCLK) skew	4.0 ns (max.) 1 1.5 ns (min.)	1.0 ns (max.) 0 ns (min.)	5.0 ns (max.) 1.5 ns (min.)
C	PCI (PCLK) to PCI (PCLK) skew	500 ps (max) - 500 ps (min)	1.5 ns (max) - 1.5 ns (min)	2.0 ns (max) - 2.0 ns (min)
D	DCLKWR to SDRAM (SCLK) skew	250 ps (max) - 250 ps (min)	380 ps (max) 2 - 380 ps (min) 2	630 ps (max) - 630 ps (min)

**NOTES:**

1. The 82443BX PCICLK input should lag its HCLK input by a minimum of 1.5 ns to a maximum of 4.0 ns at the pins of the CK100-M device. An integrated buffer offers the best control over these output-to-output drive skews.
2. This skew allowance includes  $\pm 280$  ps for I/O capacitance and SODIMM routing variation. Motherboards should allow for no more than  $\pm 100$  ps contribution to the total skew.

**Note:** Clock period, jitter, offset and skew are measured on the rising edge of the clock signals at 1.25-V for the 2.5-V clocks and at 1.5-V for the 3.3-V clocks.

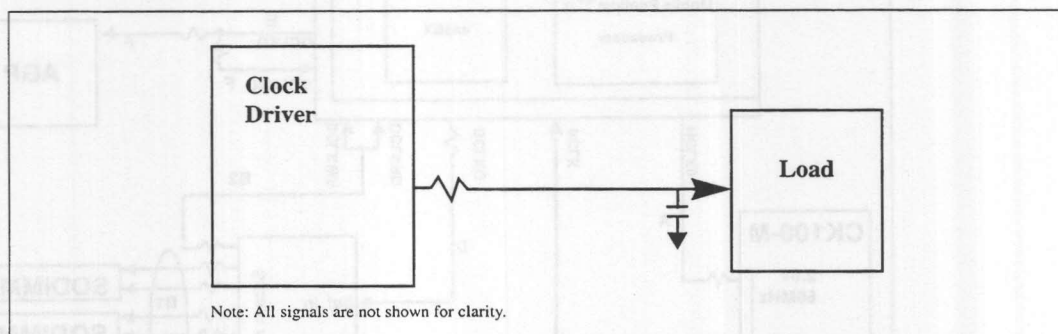
## 4.4 Clock Layout Guidelines

- Series matching resistors are required.
  - Resistor Value: See Table 7.
  - Placement: As near as possible to the driver pin (less than 1")
- A PCLK that is used for a PCI socket should be a point-to-point connection and should not be shared with another load.
- When designing with an expansion connector, remember to account for the PCICLK trace length in the docking station.
- Route all clocks on internal layers to provide better trace delay consistency and EMI containment.
- Board impedance should be  $55 \Omega \pm 15\%$ .
- Use discrete resistors on HCLK signals coming from CK100-M.
- Minimize the use of vias in clock signals.
- All clocks should have 1:2 width-to-spacing ratio.
- CKBF-M should be on the V<sub>3</sub> rail and CK100-M should be on the V<sub>3S</sub> rail (see "Power and Ground Pins" on page 34 for a description of these rails).



## 4.5 Optional Clock Layout

Figure 13. General Clock Layout



This optional layout implementation is suggested to accommodate clock tuning, HCLK & PCICLK from CK100-M and SCLK from CKBF-M. This will allow the designer to tune the individual clock signals to minimize EMI and allow for variations in impedance, skew and loading.

The variables to be considered include:

- Variation in actual device load
- Line and load impedance variation
- Driver output impedance
- Vendor variation

The stub to the capacitor must be minimized. The maximum stub length on a clock trace is < 0.5 inch. The capacitor should be placed as close as possible to the load. Refer to the specific clock vendors for layout and termination guidelines.

## 4.6 Clock Vendors

Table 8. Clock Vendors

Vendor Name	Address
IC Works, Inc.	3725 North First Street San Jose, CA 95134 (408) 922-0202
International Microcircuits, Inc.	525 Los Coches Street Milpitas, CA 95035 (408) 263-6300
Integrated Circuit Systems, Inc.	1271 Parkmoor Avenue San Jose, CA 95126-3448 (408) 925-9493
Cypress Semiconductor	12020 113th Ave. Northeast Kirkland, WA 98034 (425) 398-3400



## 5.0 82443BX AGP Interface for EMC-2 Design

This section lists guidelines to be followed when routing the signal traces for the board design. Even when the guidelines are followed, it is recommended that you simulate as many signals as possible for proper signal integrity and cross talk. See Section 6.2.10, “AGP Signals” on page 38 for AGP pull-up requirements. See Section 4.0, “Clocking Guidelines” on page 25 for AGP clocking information.

### 5.1 Layout and Routing Guidelines

For the definition of AGP interface functionality (protocols, rules and signaling mechanisms, and the platform level aspects of AGP functionality), refer to the latest *AGP Interface Specification* and *AGP Platform Design Guide*. This document focuses only on specific 440BX platform recommendations for the AGP interface.

Throughout this section the term “data” refers to G\_AD[31:0], G\_C/BE[3:0]# and SBA[7:0]. The term “strobe” refers to AD\_STB[B:A] and SB\_STB. When the term “data” is used, it is referring to one of three groups of data as seen in Table 9. When the term “strobe” is used it is referring to one of the three strobes as it relates to the data in its associated group.

**Table 9. Data and Associated Strobe**

Data	Associated Strobe
G_AD[15:0] and G_C/BE[1:0]#	AD_STBA
G_AD[31:16] and G_C/BE[3:2]#	AD_STBB
SBA[7:0]	SB_STB

#### 5.1.1 On-board AGP Compliant Device Layout Guidelines

Longer trace lengths require a greater amount of spacing between traces in order to reduce crosstalk. When using 1:2 spacing, maximum trace length of data lines is 9.5 inches. The line length mismatch is 0.5 inches. The strobe is the longest trace of the group. This restricts the maximum trace length of data lines to less than 4.5 inches for a 1:1 trace spacing. The strobe requires a 1:2 trace spacing. Trace length guidelines given in this section do not reflect signal integrity and EMI. It is recommended that you simulate the routes to ensure that signal quality requirements are met.

**Figure 14. On-board AGP Compliant Device Layout Guidelines**

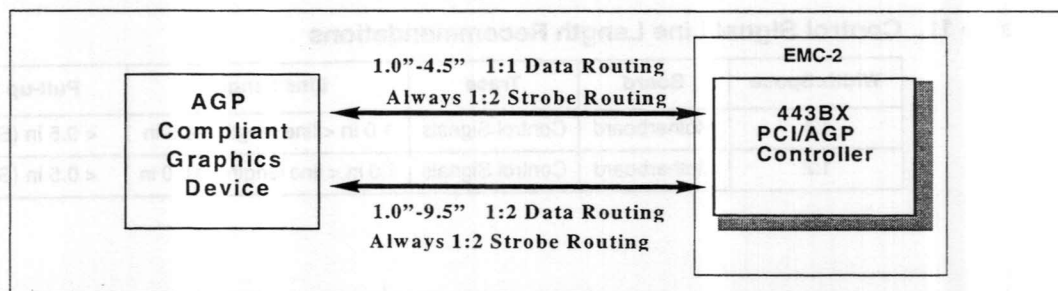
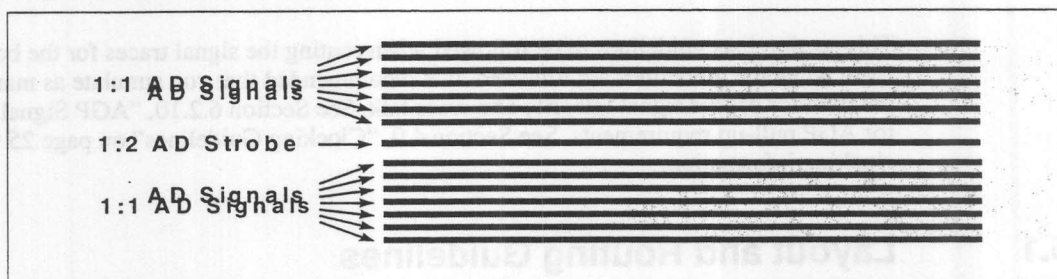




Figure 15. Signal Layout Recommendations



### 5.1.1.1 Data and Strobe Signal Routing Recommendations

Table 10. Motherboard Recommendations

Width:Space	Trace	Line Length	Line Length Matching
1:1(Data)/1:2(Strobe)	Data /Strobe	1.0 in < line length < 4.5 in	0.5 in, strobe longest trace
1:2	Data/Strobe	1.0 in < line length < 9.5 in	0.5 in, strobe longest trace

The line length mismatch must be less than 0.5" and the strobe must be the longest signal of the group. For example, if the strobe is at 4.0 inches, the data line can be from 3.5 to 4.0 inches in length. It is best to reduce the line length mismatch wherever possible to insure added margin. The strobe is always required to have 1:2 trace spacing. It is also best to separate the traces by as much as possible in order to reduce the amount of trace-to-trace coupling.

**Note:** Under certain layouts, crosstalk and ground bounce can be observed on the AD\_STB signals of the AGP interface. Although Intel has not observed system failures due to this issue, noise margin has been improved by enhancing the AGP buffers on the 82443BX. For new designs, additional margin can be obtained by following AGP layout guidelines.

### 5.1.1.2 Control Signal Routing Recommendations

Some of the control signals require pull-up resistors to be installed on the motherboard. Pull-up resistors should be discrete resistors, since resistor packs will need longer stub lengths and may violate timing requirements. The stub length to these pull-up resistors must be controlled. The maximum stub length on a strobe trace is < 0.1 inch. The maximum stub trace length on all other traces is < 0.5 inch. For Pull-up recommendations, see "AGP Signals" on page 38..

Table 11. Control Signal Line Length Recommendations

Width:Space	Board	Trace	Line Length	Pull-up Stub Length
1:1	Motherboard	Control Signals	1.0 in < line length < 8.5 in	< 0.5 in (Strobes < 0.1in)
1:2	Motherboard	Control Signals	1.0 in < line length < 10.0 in	< 0.5 in (Strobes < 0.1in)

## 5.2 ACPI Compliance Requirements

Based on the Advanced Configuration and Power Interface (ACPI) specification, the AGP graphics device must be ACPI compliant and must implement its own self power management circuitry, such as self clock-gating and an idle bus detection mechanism to reduce power. However, in an embedded Pentium® II processor-based platform the AGP device clock is a derivative of the host clock.

When the host clock stops (C3 state - Deep Sleep), the AGP clock also stops. An AGP\_BUSY# protocol solves this instantaneous AGP stop clock problem. The AGP graphics device must signal the operating system or the south bridge that it is currently busy and the AGP clock should not be stopped.

The AGP device internally protects its core logic to ensure that an illegal clock will not corrupt the AGP device state. This protection gates the internal clock nets used for the device's logic from the time STP\_AGP# is asserted until it is deasserted. The STP\_AGP# signal is an indication that the AGP clock will not be valid for much longer and should be gated off for protection. STP\_AGP# should be connected to the PIIX4E's SUS\_STAT1# signal.

The AGP\_BUSY# signal indicates that the graphics controller requires the GCLK to be running. This signal should be connected to one of the PIIX4E's PCIREQ# pins. When the PCIREQ# pin must be shared, it can be logically ORed with one of the PIIX4E's PCIREQ# inputs. AGP\_BUSY# is an open-drain signal from the graphics device and requires a 10 K $\Omega$  Pull-up resistor.

AGP\_SUSPEND# is for AGP devices that support Suspend mode. The AGP\_SUSPEND# signal can be connected to the PIIX4E's SUSB# signal.

## 5.3 AGP IDSEL Routing

An AGP compliant master is composed of a PCI compliant target interface and an AGP compliant master interface. (Optionally the device can also include a PCI compliant master interface when required.) When used in a PCI mode of operation, the AGP device must provide an external IDSEL that is connected to AD16. When the AGP device is designed for exclusive operation on the AGP interface the device does not have an external IDSEL pin, therefore IDSEL does not need to be routed.

## 6.0 Design Guideline Checklists

Design checklists provided in this section are intended to be used for schematic reviews of the 266 MHz EMC-2 based platform designs. The checklists do not represent the only way to design a system, but do provide recommendations. The system designer should examine the checklist items for correctness. Additional design considerations are also provided.

### 6.1 Resistor Values

Pull-up and pull-down register values are system dependent. The appropriate value for your system can be determined from an AC/DC analysis of the pull-up voltage used, the current drive capability of the output driver, input leakage currents of all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the input high/low voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be done to determine the minimum

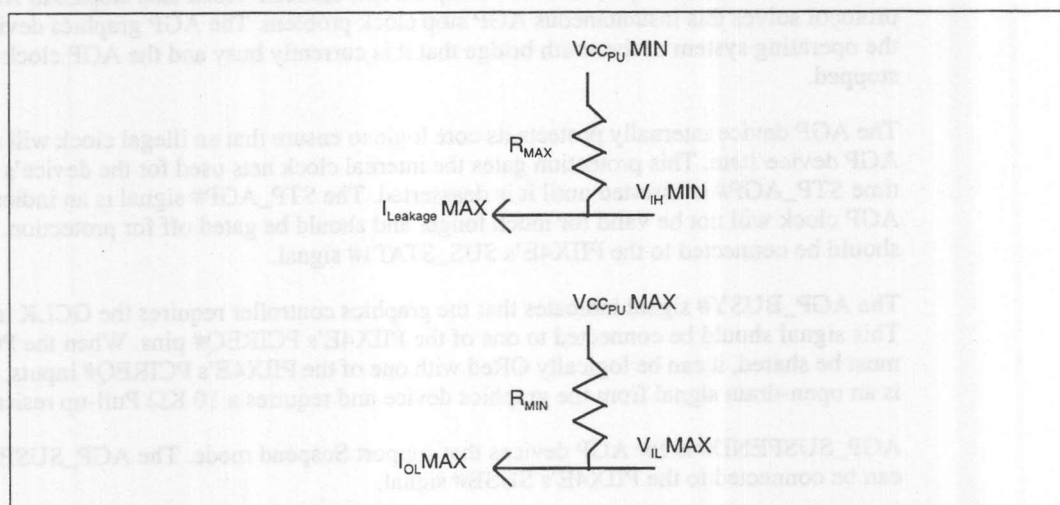
and maximum values that may be used on an individual signal. Engineering judgment should be used to determine the optimal value. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications and other considerations.

A simplistic DC calculation for a pull-up value is:

$$R_{MAX} = (V_{CCPU} MIN - V_{IH} MIN) / I_{Leakage} MAX$$

$$R_{MIN} = (V_{CCPU} MAX - V_{IL} MAX) / I_{OL} MAX$$

Figure 16. Pull-up Resistor Example



## 6.2 EMC-2 Design Checklist [ ]Pass, [ ]Fail

For PIIX4E recommendations on the I/O system electronics board, please see “82371EB (PIIX4E) Design Checklist [ ]Pass, [ ]Fail” on page 40.

### 6.2.1 EMC-2 Errata

Please see the *Mobile Pentium® II Processor Specification Update* (order number 243887) for workarounds for any errata that may be present on the stepping used.

### 6.2.2 Power and Ground Pins

- V\_DC is the DC voltage driven from the power supply and is required to be between 5-V and 21-V DC  $\pm$  5%. The module cannot be inserted or removed while V\_DC is powered on.
- V\_3S is a SUSB#-controlled 3.3-V voltage supply which is an output of the voltage regulator on the system electronics. This rail should be off during Suspend-to-RAM (STR), Suspend-to-Disk (STD), and Soft-Off (SOff) modes.
- V\_5 is a SUSC# controlled 5-V voltage supply which is an output of the voltage regulator on the system electronics. This rail should be off during Suspend-to-Disk (STD), and Soft-Off (SOff) modes.
- V\_3 is a SUSC# controlled 3-V voltage supply which is an output of the voltage regulator on the system electronics. This rail should be off during Suspend-to-Disk (STD), and Soft-Off (SOff) modes.



- V\_CPUPU is driven by the EMC-2 to power processor interface signals such as the PIIX4E open-drain pull-ups for the processor/PIIX4E sideband signals.
- V\_CLK is driven by the EMC-2 to power the HCLK drivers from the CK100-M clock source.
- VCCAGP is the VDDQ AGP voltage, and should be connected to V\_3.
- V<sub>TT</sub> is an output of the DC-DC regulator on the EMC-2, and is driven to the core voltage (VCC\_CORE) of the processor. V<sub>TT</sub> is used for ITP implementations.
- All unused active low 3.3-V tolerant inputs should be connected to V\_3S with a 10-K $\Omega$  resistor unless otherwise stated.
- All unused active high inputs should be connected to ground (V<sub>SS</sub>) through a 10-K $\Omega$  resistor unless otherwise stated.

### 6.2.3 Decoupling Requirements

In order to provide adequate filtering and in-rush current protection for any system design, bulk capacitance is required. A small amount of bulk capacitance is supplied on the EMC-2. To achieve proper filtering, additional capacitance should be placed on the system electronics. Table 12 details the bulk capacitance requirements for the system electronics when using the EMC-2.

**Table 12. Module Capacitive Decoupling Requirements**

Voltage Plane	Capacitance	ESR	Ripple Current	Rating (V)
V_DC	100 $\mu$ F, 0.1 $\mu$ F, 0.01 $\mu$ F <sup>1</sup>	20 m $\Omega$	1- 3.5 A <sup>3</sup>	20% tolerance @ 35-V
V_5	100 $\mu$ F, 0.1 $\mu$ F, 0.01 $\mu$ F <sup>1</sup>	100 m $\Omega$	1 A	20% tolerance @ 10-V
V_3	470 $\mu$ F, 0.1 $\mu$ F, 0.01 $\mu$ F <sup>1</sup>	100 m $\Omega$	1 A	20% tolerance @ 6-V
V_3S	100 $\mu$ F, 0.1 $\mu$ F, 0.01 $\mu$ F <sup>1</sup>	100 m $\Omega$	1 A	20% tolerance @ 6-V
VCC_AGP	22 $\mu$ F, 0.1 $\mu$ F, 0.01 $\mu$ F <sup>1</sup>	100 m $\Omega$	1 A	20% tolerance @ 6-V
V_CPUPU	2.2 $\mu$ F, 8200 pF <sup>2</sup>	n/a	n/a	20% tolerance @ 6-V
V_CLK	10 $\mu$ F, 8200 pF <sup>2</sup>	n/a	n/a	20% tolerance @ 6-V

**NOTES:**

1. This capacitance should be located near the processor module connector.
2. V\_CPUPU and V\_CLK filtering should be located next to the system clock synthesizer.
3. Ripple current specification depends on V\_DC input. For 5-V V\_DC, a 3.5 A device is required. For V\_DC at 18-V or higher, 1 A is sufficient.

### 6.2.4 Clock and Test Signals

- See “Clocking Guidelines” on page 25 for clocking guidelines.
- Use discrete resistors for the HCLK signals from the CK100-M. Do not mix HCLK, and PCLK signals coming from the CK100-M in resistor packs.
- FQS should be connected to the SEL pin of the CK100-M to provide the host clock frequency. CKBF-M should be on the V\_3 rail and the CK100-M should be on the V\_3S rail.
- The clock signal from the CKBF-M to the SODIMM should have 18  $\Omega$  series termination resistors.
- CONFIG[1] should be pulled to V\_3ALWAYS with a 100-K $\Omega$  resistor on the system I/O.
- CONFIG[2] should be pulled to GND in all 440BX AGPset based designs. A weak 100-K $\Omega$  resistor may be used.



Table 13. Clock and Test Signal Resistor Values

Name	Termination Resistor ( $\Omega$ )	Pull-up (Pull-down) Resistor ( $\Omega$ )
HCLK	22 (see above)	None
PCLK	33 (see above)	None
DCLKO	18	None
DCLKRD	†	None
DCLKWR	†	None
GCKO	18†	None
GCKIN	18†	None
SDRAM_CLK	18†	None
FQS	None	None

† See “Clock period, jitter, offset and skew are measured on the rising edge of the clock signals at 1.25-V for the 2.5-V clocks and at 1.5-V for the 3.3-V clocks.” on page 28.

## 6.2.5 SDRAM and EDO Signals

- See “Memory Guidelines” on page 14 for memory guidelines.
- MD[63:0] should have 18  $\Omega$  series termination resistors.

Table 14. SDRAM and EDO Signal Resistor Values

Name	Termination Resistor ( $\Omega$ )	Pull-up (Pull-down) Resistor ( $\Omega$ )
MD[63:0]	18	None

## 6.2.6 Module Strapping Options

- MAB9# is the AGP Disable strapping option on the EMC-2. This pin should be pulled up to V<sub>3</sub> with a 10-K $\Omega$  resistor when the AGP is disabled.

Table 15. EMC-2 Strapping Options

Pin Name	Function	Low	High	Internal Resistor	Status Register
MAB9#	AGP Disable	AGP Enabled	AGP Disabled	Pull-down	PMCR[1]

## 6.2.7 PCI Bus Signals

- See “PCI Bus Signals” on page 41.
- The EMC-2 supports only 3.3-V PCI.
- An 8.2 K $\Omega$  – 10 K $\Omega$  pull-up to V<sub>3S</sub> should be placed on the CLKRUN# signal.
- The 82443BX does not implement the PERR# pin. Data parity errors are still detected and reported on SERR# (when enabled by SERRE and PERRE).

### 6.2.7.1 Design Considerations

The 82443BX supports up to five PCI masters with its REQ[4:0]#/GNT[4:0]# pairs. The PCI bus supports up to 10 PCI loads. The 82443BX and the PIIX4E each represent one load; other PCI components soldered on the motherboard add one load each; and each PCI connector adds approximately two loads. A design with four PCI slots and no motherboard devices uses all available PCI loads. When all five REQ[4:0]#/GNT[4:0]# pairs are used, simulation is required to ensure that the PCI Bus Specification Rev. 2.1 timings are met. It is recommended, per the PCI specification, that the design have series resistors (~100  $\Omega$ ) on each of the PCI connector IDSEL lines.

**Table 16. PCI Bus Signals Resistor Values**

Name	Termination Resistor ( $\Omega$ )	Pull-up (Pull-down) Resistor ( $\Omega$ )
AD[31:0]	None	None
C/BE[3:0]#	None	None
FRAME#	None	10 K pull-up to V <sub>3S</sub>
DEVSEL#	None	10 K pull-up to V <sub>3S</sub>
IRDY#	None	10 K pull-up to V <sub>3S</sub>
TRDY#	None	10 K pull-up to V <sub>3S</sub>
STOP#	None	10 K pull-up to V <sub>3S</sub>
REQ[4:0]#	None	10 K pull-up to V <sub>3S</sub> if unused
GNT[4:0]#	None	10 K pull-up to V <sub>3S</sub> if used
PHOLD#	None	10 K pull-up to V <sub>3S</sub>
PHLDA#	None	10 K pull-up to V <sub>3S</sub>
PAR	None	None
SERR#	None	10 K pull-up to V <sub>3S</sub>
CLKRUN#	None	8.2 ~ 10 K pull-up to V <sub>3S</sub>
PCIRST#	33 (see "PCI Bus Signals" on page 41)	None
PLOCK#	None	10 K pull-up to V <sub>3S</sub>

### 6.2.8 Processor/PIIX4E ISA Bridge Sideband Signals

- Pull-ups to V<sub>CPUPU</sub>: INIT# - 1 K $\Omega$ , STPCLK# - 680  $\Omega$ ; LINT1#/NMI, LINT0#/INTR, IGNNE#, A20M#, SMI# - 4.7 K $\Omega$ . These are open collector outputs from the PIIX4E component.
- CPURST can be left unconnected for EMC-2 designs.
- Refer to the *System Management Bus Specification* (see Table 2) for descriptions and specifications of the three SMBus signals: SMBALERT#, SMBCLK, and SMBDATA. A pull-up resistor is required. Values will vary depending on V<sub>DD</sub> and the actual capacitance of the bus.

Table 17. Sideband Signal Resistor Values

Name	Termination Resistor ( $\Omega$ )	Pull-up (Pull-down) Resistor ( $\Omega$ )
FERR#	None	None
CPURST	None	None
IGNNE#	None	4.7 K pull-up to V_CPUPU
INIT#	None	1 K pull-up to V_CPUPU
INTR	None	4.7 K pull-up to V_CPUPU
NMI	None	4.7 K pull-up to V_CPUPU
A20M#	None	4.7 K pull-up to V_CPUPU
SMI#	None	4.7 K pull-up to V_CPUPU
STPCLK#	None	680 pull-up to V_CPUPU

### 6.2.9 Power Management Signals

- MID[3:0] should have a 100 K $\Omega$  pull-up to V\_3S.
- BXPWROK must transition from inactive (low) to active (high) a minimum of 1 ms after BX\_VCC is within the specified Functional Operating Range. See “82443BX Host Bridge Controller Power Sequencing” on page 69 for more information.

Table 18. Power Management Signals Resistor Values

Name	Termination Resistor ( $\Omega$ )	Pull-up (Pull-down) Resistor ( $\Omega$ )
SUS_STAT#	None	None
VR_ON	None	None
VR_PWRGD	None	None
SM_CLK	None	Refer to the <i>System Management Bus Specification</i>
SM_DATA	None	Refer to the <i>System Management Bus Specification</i>
ATF_INT#	None	Refer to the <i>System Management Bus Specification</i>
MID[3:0]	None	100 K pull-up to V_3S

### 6.2.10 AGP Signals

- See “82443BX AGP Interface for EMC-2 Design” on page 31
- The MAB9# strapping option for the 443BX is on the I/O system electronic board. This allows the designers to enable or disable the AGP.
- When the AGP is disabled all AGP signals are three-stated and isolated. They do not need external pull-up resistors.
- Unconnected pins on a disabled AGP interface: PIPE#, SBA[7:0], RBF#, ST[2:0], AD\_STBA, AD\_STBB, SB\_STB, G\_FRAME#, G\_IRDY#, G\_TRDY#, G\_STOP#, G\_DEVSEL#, G\_REQ#, G\_GNT#, G\_AD[31:0], G\_C/BE[3:0]#, G\_PAR.
- The AGP graphic card must be able to signal the operating system, or the south bridge, that it is currently busy and the AGP clock should not be stopped. See “ACPI Compliance Requirements” on page 33.



- The LOCK# signal is not supported on the AGP interface, even for PCI operations.
- AGP signals that require pull-ups should use discrete resistors not resistor packs.
- When the AGP is enabled the following AGP signals must have pull-up resistors of approximately 8.2 K $\Omega$  to VCCAGP to ensure they contain stable values when no agent is actively driving the bus: G\_FRAME#, G\_TRDY#, G\_IRDY#, G\_DEVSEL#, G\_STOP#, SERR#, PERR#, RBF#, INTA#, INTB#, PIPE#, G\_REQ#, G\_GNT#, SB\_STB, AD\_STBA, AD\_STBB.
- GPAR requires a 100 K $\Omega$  pull-down resistor when the design is interfacing to an AGP connector, or when the AGP compliant device uses PIPE# or side band addressing. When the AGP compliant device uses GFRAME# only, the pull-down resistor is not needed.
- When side band addressing is disabled, SBA[7:0] are isolated and no external pull-ups are required.
- When PIPE# is used to queue addresses the master is not allowed to queue addresses using the side band addressing bus.
- No external termination (for signal quality) is required by the specification. Termination can be added to improve signal integrity, provided that performance (timing) constraints are still satisfied.
- AGP interrupts may be shared with PCI interrupts similar to the recommendations in the PCI Revision 2.1 specification. For example, in a system with three PCI slots and one AGP, interrupts should be connected such that each of the four INTA# lines connects to a unique input on the PIIX4E. It is recommended that the interrupts be staggered. It is also recommended that each PIRQ be programmed to a different IRQ, if possible.
- The system electronics (S.E.) board designer must properly interface the AGP interrupts to the PCI bus.
- In order to minimize the impact of any impedance mismatch between the S.E. board and the add-in card, an impedance of 55  $\Omega \pm 15\%$  is strongly recommended.
- The AGP strobe signals must be grouped with their associated data signals. AD\_STBA with G\_AD[15:0], AD\_STBB with G\_AD[31:16], SB\_STB with SBA[7:0]. See Section 5.1, "Layout and Routing Guidelines" on page 31.
- Some onboard AGP devices may require their own VREF. This should be generated locally from the AGP interface VCCAGP rail. You should use a separate voltage divider from the AGP\_REF for 82443BX. Do not connect the two. The VCCAGP rail is the AGP controller I/O ring voltage supply.

Table 19. AGP Signals Resistor Values (Sheet 1 of 2)

Name	Termination Resistor ( $\Omega$ )	Pull-up (Pull-down) Resistor ( $\Omega$ )
GAD[31:0]	None	None
GC/BE[3:0]#	None	None
GFRAME#	None	8.2 K pull-up to VCCAGP
GDEVSEL#	None	8.2 K pull-up to VCCAGP
GIRDY#	None	8.2 K pull-up to VCCAGP
GTRDY#	None	8.2 K pull-up to VCCAGP
GSTOP#	None	8.2 K pull-up to VCCAGP
GREQ#	None	8.2 K pull-up to VCCAGP



Table 19. AGP Signals Resistor Values (Sheet 2 of 2)

Name	Termination Resistor ( $\Omega$ )	Pull-up (Pull-down) Resistor ( $\Omega$ )
GGNT#	None	8.2 K pull-up to VCCAGP
GPAR	None	100 K pull-down (If AGP device does NOT use GFRAME# ONLY)
PIPE#	None	8.2 K pull-up to VCCAGP
SBA[7:0]	None	None
RBF#	None	8.2 K pull-up to VCCAGP
ST[2:0]	None	None
ADSTB[B:A]	None	8.2 K pull-up to VCCAGP
SBSTB	None	8.2 K pull-up to VCCAGP

### 6.3 82371EB (PIIX4E) Design Checklist [ ]Pass, [ ]Fail

#### 6.3.1 82371EB (PIIX4E) Errata

- Please see the *82371EB (PIIX4E) PCI ISA IDE Xcelerator Specification Update* for workarounds or any errata that may be applicable to the stepping used.

#### 6.3.2 Power and Ground Pins

- V\_3ALWAYS is a 3.3-V rail that is connected to V<sub>CC</sub>(SUS) of the PIIX4E. V\_3ALWAYS should power off only when the system is mechanically off.
- V<sub>CC</sub> and V<sub>CC</sub>(USB) must be tied to V\_3S. V<sub>CC</sub>(USB) should be tied to the same voltage rail as the PIIX4E core.
- V<sub>CC</sub>(RTC) should be tied to the 3.3-V supply voltage for the RTC logic.
- V<sub>REF</sub> must be tied to 5-V in a 5-V tolerant system. This signal must power up before or simultaneous to V\_3S, and it must power down after or simultaneous to V\_3S. Note that most IDE devices operate at 5-V, so even when running a 3.3-V PCI bus, the PIIX4E IDE interface must be 5-V tolerant.
- V<sub>REF</sub> can be tied to V\_3S in a non-5-V tolerant system. IDE devices are generally 5-V devices.
- Tie V<sub>SS</sub> and V<sub>SS</sub>(USB) to ground.
- All unused active low 3.3-V tolerant inputs should be connected to V\_3S with a 10-K $\Omega$  resistor unless otherwise stated.
- All unused active high inputs should be connected to ground (V<sub>SS</sub>) through a 10-K $\Omega$  resistor unless otherwise stated.

Table 20. PIIX4E Power Signal Pin Assignments

Power Pins	Ball Number
VCC	E9, E11, E12, E16, F5, F6, F14, F15, G6, P15, R6, R7, R15, T6
VCC(RTC)	L16
VCC(SUS)	N16,R16
VCC(USB)	K5
VSS(USB)	J5
VSS	D10, E7, E13, J9-J12, K9-K12, L9-L12, M9-M12

### 6.3.3 Clock and Test Signals

- USB Clock - A 48 MHz clock with a duty cycle of better than 40/60% should be fed into the PIIX4E's USB clock input, pin L3.
- Place a 10-K $\Omega$  pull-up resistor on TEST# to V\_3ALWAYS. Test signals reside in the Suspend/Resume well.
- In a Pentium II processor-based system, CONFIG[1] should be pulled to V\_3ALWAYS with a 100-K $\Omega$  resistor.
- CONFIG[2] should be pulled to GND with a 100-K $\Omega$  resistor in all 440BX AGPset-based designs.

Table 21. Clock and Test Signal Resistor Values

Name	Termination Resistor ( $\Omega$ )	Pull-up (Pull-down) Resistor ( $\Omega$ )
TEST#	None	10 K Pull-up to V_3ALWAYS
CONFIG[1]	None	100 K Pull-up to V_3ALWAYS
CONFIG[2]	None	100 K Pull-down

### 6.3.4 PCI Bus Signals

- All unused general purpose inputs (GPIs) should be pulled to a valid logic level with a 10-K $\Omega$  resistor. When pulled high, they should be pulled to V\_3S except for the GPIs that are in the VCC(SUS) well.
- All unused outputs can be left as no-connects.
- All IDSEL signals should have a 100-W series resistor at each device.
- In a 5-V PCI environment, place 2.7 K $\Omega$  pull-up resistors to 5-V on PIRQ[A:D]#, SDONE, SBO#, FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, PERR#, SERR#, REQ64# and ACK64# on the PCI bus.
- Place the 10-K $\Omega$  pull-up resistors to V\_3S on PCIREQ[D:A]# and REQ[A:C]# when these signals are unused or when using a PCI add-in slot to insure that these signals do not float.
- In a 3.3-V PCI environment, place 10-K $\Omega$  pull-up resistors to V\_3S on PIRQ[A:D]#, SDONE, SBO#, FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, PERR#, SERR#, REQ64# and ACK64# on the PCI bus.

- For all new designs, make sure that the PIIX4E does not connect IDSEL to AD12, becoming device 1. On 82443BX, AGP is known as device 1 whether disabled or not. Connect IDSEL from PIIX4E to AD18.
- For systems in which the PCIRST# signal is lightly loaded (<50 pF), place a 33-W series termination resistor on this signal. This resistor should be placed as close as possible to the PIIX4E.

Table 22. PCI Bus Signal Resistor Values

Name	Termination Resistor ( $\Omega$ )	Pull-up (pull-down) Resistor ( $\Omega$ )
Unused GPIs	None	10 K to a valid level
IDSEL signals	100	None
PIRQ[A:D]#	None	10 K Pull-up to V <sub>3S</sub>
SDONE	None	10 K Pull-up to V <sub>3S</sub>
SBO#	None	10 K Pull-up to V <sub>3S</sub>
FRAME#	None	10 K Pull-up to V <sub>3S</sub>
TRDY#	None	10 K Pull-up to V <sub>3S</sub>
STOP#	None	10 K Pull-up to V <sub>3S</sub>
IRDY#	None	10 K Pull-up to V <sub>3S</sub>
DEVSEL#	None	10 K Pull-up to V <sub>3S</sub>
PLOCK#	None	10 K Pull-up to V <sub>3S</sub>
PERR#	None	10 K Pull-up to V <sub>3S</sub>
SERR#	None	10 K Pull-up to V <sub>3S</sub>
REQ64#	None	10 K Pull-up to V <sub>3S</sub>
ACK64#	None	10 K Pull-up to V <sub>3S</sub>
PCIREQ[D:A]#	None	10 K Pull-up to V <sub>3S</sub>
REQ[A:C]#	None	10 K Pull-up to V <sub>3S</sub>

### 6.3.5 ISA/EIO Signals

- When implementing Power On Suspend (POS) mode, ISA signals should be pulled up to V<sub>3S</sub>. Otherwise use V<sub>5S</sub>.
- Use 4.7 K $\Omega$  pull-up resistors on SD[15:0], MEMR#, MEMW#, IOR#, IOW#, IOCS16#.
- Use 1 K $\Omega$  pull-up resistors on IOCHRDY, MEMCS16#, REFRESH#, ZEROWS#.
- Use 10 K $\Omega$  pull-up resistors on IRQx. IRQ8# resides in the V<sub>CC</sub>(SUS) well, it must be pulled to V<sub>3ALWAYS</sub>. When IRQ8# is not used, its default is GPI[6] and it requires a 10 K $\Omega$  external pull-up resistor.
- Use a 4.7 K $\Omega$  pull-down resistor on DRQx.
- When using the EIO bus, IOCHK# becomes a general-purpose input and in ISA, IOCHK# requires a 4.7 K $\Omega$  pull-up resistor.



Table 23. ISA/EIO Signal Resistor Values

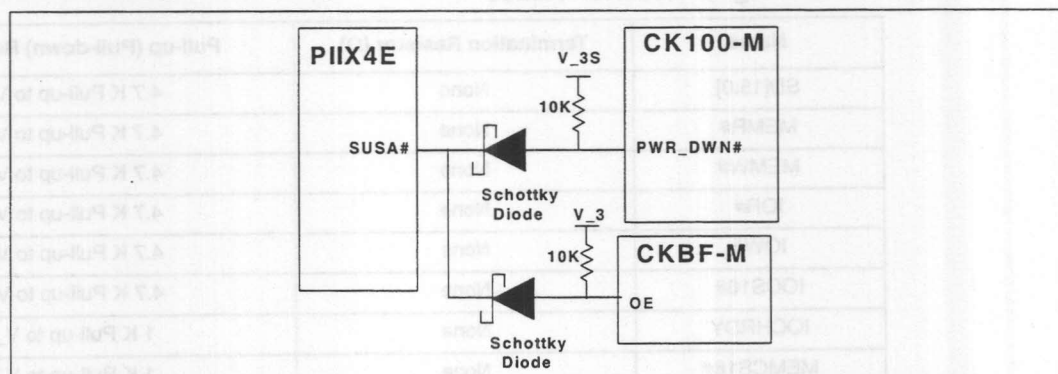
Name	Termination Resistor ( $\Omega$ )	Pull-up (Pull-down) Resistor ( $\Omega$ )
SD[15:0]	None	4.7 K Pull-up to V <sub>3S</sub>
MEMR#	None	4.7 K Pull-up to V <sub>3S</sub>
MEMW#	None	4.7 K Pull-up to V <sub>3S</sub>
IOR#	None	4.7 K Pull-up to V <sub>3S</sub>
IOW#	None	4.7 K Pull-up to V <sub>3S</sub>
IOCS16#	None	4.7 K Pull-up to V <sub>3S</sub>
IOCHRDY	None	1 K Pull-up to V <sub>3S</sub>
MEMCS16#	None	1 K Pull-up to V <sub>3S</sub>
REFRESH#	None	1 K Pull-up to V <sub>3S</sub>
ZEROWS#	None	1 K Pull-up to V <sub>3S</sub>
IRQx	None	10 K Pull-up to V <sub>3S</sub> (see above)
DRQx	None	4.7 K (Pull-down)
SIRQ	None	10 K Pull-up to V <sub>3S</sub>
IOCHK#	None	4.7 K Pull-up (if using ISA bus)

### 6.3.6 Power Management Signals

- Power management signals that reside in the V<sub>CC</sub>(SUS) well may require pull-ups, the pull-ups must be connected to V<sub>3ALWAYS</sub>. These signals do not support 5-V input levels.
- EXTSMI# is an input at reset and an open drain output when activating an SMI# within the Serial IRQ function. Designers may need an 8.2 K $\Omega$  pull-up to V<sub>3ALWAYS</sub> when it is not always being driven to a valid state.
- When CLKRUN# is not connected between the PIIX4E and the 82443BX, it should be tied low through a 100  $\Omega$  resistor at the 82443BX. When CLKRUN# is connected between the PIIX4E and the 82443BX, an 8.2 K $\Omega$  – 10 K $\Omega$  pull-up to V<sub>3S</sub> should be placed on the CLKRUN# signal.
- SUS\_STAT1# is connected between the 82443BX and the PIIX4E.
- SUS\_STAT2# is connected from the PIIX4E to the devices that must be informed of the stopping of the clocks.
- PCI\_STP# is connected to the clock synthesizer to stop the PCI clocks.
- CPU\_STP# is connected to the clock synthesizer to stop the processor clock.
- SUSA# is connected to the clock synthesizer's PWR\_DWN# pin through a Schottky diode with a 10 K $\Omega$  pull-up resistor. Alternatively, SUSA# may be used to control the clock synthesizer's power plane.



Figure 17. Clock Design Block Diagram



- SUSA# and SUSC# are used to control the power planes.
- THRM# is connected to the thermal protection logic.
- PCIREQ[D:A]# is connected between the PIIX4E and the PCI bus. Bus master requests are considered to be power management events.
- Connect RI# to the modem when this feature is used.
- Connect BATLOW# to the battery monitoring logic when this feature is implemented.
- Connect LID to the lid monitoring logic of the system.
- PWRBTN# is connected to logic that allows the user to switch from and to suspend.
- RSMRST# is connected to a switch to allow a complete system reset. This signal resides in the  $V_{CC}(RTC)$  well. Its potential must not exceed that of  $V_{CC}(RTC)$ .

Table 24. Power Management Signal Resistor Values

Name	Damping Resistor ( $\Omega$ )	Pull-up (Pull-down) Resistor ( $\Omega$ )
EXTSMI#	None	See above
CLKRUN#	None	8.2 K $\Omega$ ~10 K $\Omega$ Pull-up to $V_{3S}$ (if connected from PIIX4E to 82443BX) 100 K $\Omega$ (Pull-down) otherwise

### 6.3.7 USB Interface

- Refer to the *PIIX4 USB Design Guide* (see Table 2) for the layout recommendations for USB, clock, over-current detection circuit and general board layout recommendations.

### 6.3.8 IDE Interface

- 5.6 K $\Omega$  pull-down resistors on PDDREQ and SDDREQ.
- 1 K $\Omega$  pull-up resistors on PIORDY and SIORDY.
- 470  $\Omega$  pull-down resistor on pin 28 of the IDE connector (CSEL). Support Cable Select (CSEL) is a PC97 requirement. The state of the cable select pin determines the master/slave configuration of the hard drive at the end of the cable.
- The primary IDE connector uses IRQ14, and the secondary IDE connector uses IRQ15.

- The ATA-4 specification requires 33  $\Omega$  series terminating resistors on P/SDIOR, P/SDIOW#, P/SDCS[1,3]#, P/SDA[2:0], P/SDDACK# and P/SDD[15:0]. These series termination resistors should be placed as close as possible to the PIIX4E.
- For Ultra-DMA enabled systems, the ATA-4 specification also requires 82  $\Omega$  series terminating resistors on P/SDDREQ, INTRQx and P/SIORDY. These series terminating resistors should be placed as close as possible to the PIIX4E.
- When the distance between the PIIX4E and connector is greater than 4", the terminating resistor should be placed within 1" of the PIIX4E.
- When using the ISA reset signal RSTDRV from the PIIX4E, it should be routed through a Schmitt trigger for RESET# signals.
- Ground pins 19, 2, 22, 24, 26, 30, 40 of both ATA connectors
- Pins 20 and 34 of both ATA connectors should be left unconnected.
- According to ATA-4 specification, a 10 K $\Omega$  pull-down resistor is required on DD7 to allow a host to recognize the absence of a device at power-up.
- Exceptions: When the PIIX4E's IDE interface is configured as Primary 0/Primary 1, and two IDE devices are connected, it should appear to the devices as if they are on the same cable. See *Intel® 82371AB PCI-to-ISA/IDE Xcelerator (PIIX4) datasheet* (order number 290562).
  - Both IDE devices should connect to IRQ14.
  - CSEL connected (pin28) together between the two ATA connectors and be pulled down with a 470  $\Omega$  resistor to meet PC97 requirement.
  - DIAG (pin 34) connected together between the two ATA connectors.

Table 25. IDE Interface Signal Resistor Values

Name	Termination Resistor ( $\Omega$ )	Pull-up (pull-down) Resistor ( $\Omega$ )
PDDREQ	33 (82 for Ultra DMA)	5.6 K (pull-down)
SDDREQ	33 (82 for Ultra DMA)	5.6 K (pull-down)
PIORDY	82 (Ultra DMA only)	1 K Pull-up
SIORDY	82 (Ultra DMA only)	1 K Pull-up
CSEL (Pin 28)	None	470 (pull-down)
All signals to the two IDE connectors	33	None
DD7	33	10 K (pull-down)

### 6.3.9 BIOS to Flash Memory Interface

2 Mbits of flash is usually all that is required to support the 82443BX in all configurations. These are the recommendations for an Intel 28F200BV flash part.

- Use 0.01  $\mu$ F - 0.1  $\mu$ F capacitors for power supply ( $V_{CC}$  and  $V_{PP}$ ) decoupling.
- Connect BYTE# to GND when a x16 flash device is used to configure it for x8.
- Use GPOx to control the WP# signal.
- Connect  $V_{PP}$  to 5-V.
- Use GPOx to control the RP# signal.

## 7.0 Power Sequencing

This section provides a summary of the power sequencing requirements and options of the 440BX AGPset. It provides a detailed description of the PIIX4E Suspend/Resume sequence, signaling protocols, and timings. The recommended usage model for power plane control in a 440BX platform using PIIX4E power management signals is described.

This section does not represent the only way to design a system, but it does provide recommendations for using the 440BX AGPset.

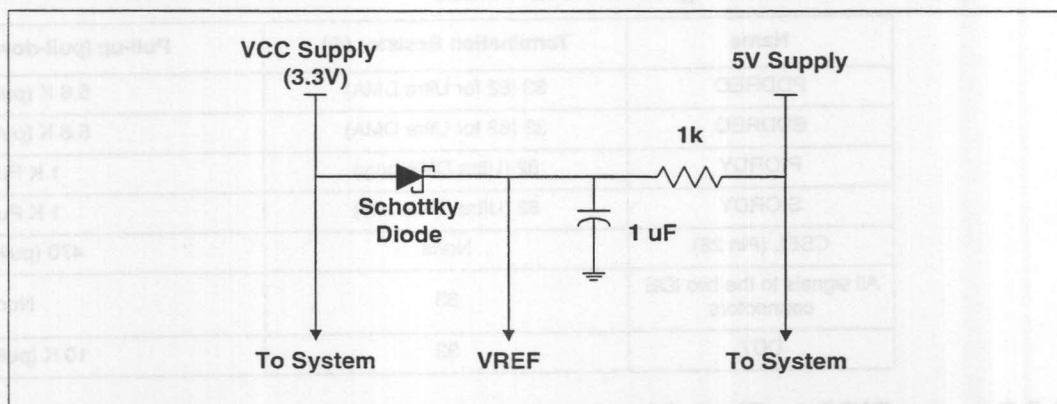
## 7.1 PIIX4E Power Sequencing

### 7.1.1 Power Sequencing Requirements

In systems requiring 5-V tolerance, the VREF signal must be tied to 5-V. This signal must power up before or simultaneous to  $V_{CC}$ . It must power down after or simultaneous to  $V_{CC}$ . In a non-5-V tolerant system (3.3-V only), this signal can be tied directly to  $V_{CC}$ . There are then no sequencing requirements. Refer to Figure 18 for an example circuit schematic, which may be used to ensure the proper VREF sequencing.

The PIIX4E  $V_{CC}$  and  $V_{CC}(USB)$  supplies are separated internally in order to reduce noise on USB signals. They should not be powered up or down independently of one another. They should be connected to the same power plane on the motherboard. There are no other power sequencing requirements for the various  $V_{CC}$  power supplies to the PIIX4E.

Figure 18. VREF Supply Schematic



### 7.1.2 Suspend/Resume and Power Plane Control

The PIIX4E supports three different Suspend modes. The common system usage model for these modes is described here and includes Power On Suspend (POS), Suspend to RAM (STR), and Suspend to Disk (STD). This mode definition allows for other system usage models that use the PIIX4E suspend/resume control signals in other ways. The common system mode names are used throughout this document.



The PIIX4E power management architecture is designed to allow systems to support multiple suspend modes, and to switch between those modes as required. A suspended system can be resumed by a number of different events. The system returns to full operation, and can then continue processing or be placed into another suspend mode. The new mode can be at a lower power mode than from what it resumed.

### 7.1.2.1 Power On Suspend (POS) System Model

All devices are powered up except for the clock synthesizer. The Host and PCI clocks are inactive, and the PIIX4E provides control signals and the 32 KHz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer. The only power consumed in the system while it is in POS mode is due to DRAM refresh and leakage current of the powered devices.

When the system resumes from POS mode, the PIIX4E can resume without resetting the system, can reset the processor only, or can reset the entire system. When no reset is performed, the PIIX4E only needs to wait for the clock synthesizer and processor PLLs to lock before the system is resumed. This takes typically 20 ms.

### 7.1.2.2 Suspend to RAM (STR)

Power is removed from most of the system components during STR, except the DRAM. Power is supplied to the host bridge (for DRAM Suspend Refresh) and the PIIX4E's RTC and Suspend Well logic. The PIIX4E provides control signals and a 32 KHz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer and other power planes.

The PIIX4E resets the system on resume from STR.

### 7.1.2.3 Suspend to Disk (STD) and Soft Off (SOff)

Power is removed from most of the system components during STD. Power is maintained to the RTC and Suspend Well logic in the PIIX4E.

The PIIX4E resets the system on resume from STD.

The STD state is also called the Soft Off (SOff) state. The difference depends on whether the system state is restored by software to a pre-suspend condition or if the system is rebooted.

### 7.1.2.4 Mechanical Off (MOff)

This is not a suspend state. This is a condition where all power except the RTC battery has been removed from the system. It is typically controlled by a mechanical switch that turns off AC power to a power supply. It could be used as a condition in which an embedded system's main battery has been removed.

The PIIX4E controls the system entering the various suspend states through the suspend control signals listed in Table 26. Upon initiation of suspend, the PIIX4E asserts the SUS\_STAT[1-2]#, SUSA#, SUSB#, and SUSC# signals in a well defined sequence to switch the system into the desired power state. The SUSA#, SUSB#, and SUSC# signals can be used to control various power planes in the system. The SUS\_STAT1# signal is a status signal that indicates to the host bridge when to enter or exit a suspend state, or when to enter or exit a stop clock state (when the system is still running). This is typically used to place the DRAM controller into a Suspend Refresh mode of operation. The SUS\_STAT2# signal is a status signal that can be used to indicate to other system devices when to enter or exit a suspend state (like the graphics and Cardbus controllers). See



“System Suspend and Resume Control Signaling” on page 50 for sequencing details. Note that these signals are associated with a particular type of suspend mode and power plane for descriptive purposes here. The system designer is free to use these signals to control any type of function desired.

The system is placed into a suspend mode by programming the Power Management Control register. The Suspend Type is first programmed and then the Suspend Enable bit is set. This causes the PIIX4E to automatically sequence into the programmed suspend mode.

**Table 26. Power State Decode**

Power State	RSMRST#	SUS_STAT1#	SUS_STAT2#	SUSA#	SUSB#	SUSC#
On	1	x <sup>†</sup>	1	1	1	1
POS	1	0	0	0	1	1
STR	1	0	0	0	0	1
STD/SOFF	1	0	0	0	0	0
Mechanical Off	0	0	0	0	0	0

<sup>†</sup> SUS\_STAT1# is also used when the system is running. It indicates to the Host-to-PCI bridge when to switch between the normal and suspend refresh mode for DRAM Stop Clock support. In the Stop Clock condition, HCLK is stopped and the Host-to-PCI bridge must run DRAM refresh from the internal oscillator.

### 7.1.3 System Resume

The PIIX4E can be resumed from either a Suspend or Soft Off state. Depending on the suspend state that the system is in, different features can be enabled to resume the system. There are two classes of resume events, those whose logic resides in the PIIX4E main power well and those whose logic resides in the PIIX4E suspend well. Those in the suspend well can resume the system from any Suspend or Soft Off state. Those in the main power well can only resume the system from a Power On Suspend state. Table 27 lists the suspend states for which a particular resume event can be enabled.

Upon detection of an enabled resume event, the PIIX4E sets appropriate status signals and automatically transitions its suspend control signals to bring the system into a “full on” condition. The sequencing is shown in “System Suspend and Resume Control Signaling” on page 50.

**Table 27. Resume Events Supported In Different Power States (Sheet 1 of 2)**

Resume Event	Suspend States			
	POS	STR	STD/SOff	MOff
RTC Alarm (IRQ8) <sup>†</sup>	x	x	x	
SMBus Resume Event (Slave Port Match)	x	x	x	
Serial A Ring (RI)	x	x	x	
Power Button (PWRBTN#)	x	x	x	
EXTSMI (EXTSMI#)	x	x	x	
LID (LID)	x	x	x	
GPI 1	x	x	x	
GSTBY Timer Expiration	x	x	x	

Table 27. Resume Events Supported In Different Power States (Sheet 2 of 2)

Resume Event	Suspend States			
	POS	STR	STD/Soff	Moff
Interrupt (IRQ 1,3-15)	x			
USB	x			

† RTC Alarm only supports internal RTC. For external RTC implementations, the IRQ8 must be tied to one of the other resume input signals (GPI[1], LID, EXTSMI#,RI#) for the resume functionality.

### 7.1.3.1 System Resume Events

The various resume events and their programming model are shown here.

Table 28. Resume Event Programming Model

System Resume Event	Programming Model
PWRBTN# Asserted	[PWRBTN_EN]
LID Asserted	[LID_EN]
- Polarity Select	[LID_POL]
GPI[1] Asserted	[GPI_EN]
EXTSMI# Asserted	[EXTSMI_EN]
SMBus Events:	[ALERT_EN] [SLV_EN] [SHDW1_EN] [SHDW2_EN]
Global Standby Timer Expiration:	[GSTBY_EN]
Ring Indicate Assertion (RI#)	[RI_EN]
RTC Alarm (IRQ8) <sup>†</sup>	[RTC_EN]
USB Resume Signaling: (POS Only)	[USB_EN]
IRQ[1,3-7,9-15]: (POS Only)	[IRQ_RSM_EN]

† RTC Alarm only supports internal RTC. For external RTC implementations, the IRQ8 must be tied to one of the other resume input signals (GPI[1], LID, EXTSMI#,RI#) for the resume functionality.

### 7.1.3.2 Global Standby Timer Resume

The Global Standby Timer is used to monitor system activity during normal operation and can be reloaded by system activity events. Upon expiration, it generates an SMI#. When the system is placed in a Suspend Mode, the Global Standby Timer can be used to generate a resume event. The Global Standby Timer can enable two different timer resolutions for wake-up times from approximately 30 seconds to 8.5 hours. This can allow the system to transition into a lower power suspend state.

See the System Management Section of the 82371AB PCI-to-ISA/IDE Xcelerator (PIIX4) datasheet for additional information about the Global Standby Timer.

## 7.1.4 System Suspend and Resume Control Signaling

The PIIX4E automatically controls the signals required to transition the system between the various power states. It provides control for Host and PCI clocks, main memory and video memory refresh, system power plane control, and system reset. Table 29 and Table 30 illustrate the common usage model for power plane control using the SUS[C:A]# signals. The PIIX4E Resume well should always be powered by a trickle supply (main battery or backup battery in an embedded system).

**Table 29. Power Plane Control**

SUSA# (POS)	SUSB# (STR)	SUSC# (STD)
Clock synthesizer Video display <sup>1</sup>	Processor (Low Power GTL+ supplies) PIIX4E Core Other system devices <sup>2</sup>	82443BX Host Bridge Controller DRAM Graphics Controller

**NOTES:**

1. The video display (flat panel or CRT) may optionally be powered off in POS. This could be accomplished by using the PIIX4E's SUSA# or SUS\_STAT2# signals to assert the video controller's STANDBY signal.
2. Devices may include mass storage, audio, or other devices that will not generate system resume events.

**Table 30. Power Plane Control Using SUS[C:A]# Signals**

Power Plane	Suspend Mode (Suspend Mode Signals Asserted by the PIIX4E)			
	Full On (None)	POS (SUSA#, SUS_STAT[2:1]#)	STR (SUS[B:A]# SUS_STAT[2:1]#)	STD (SUS[C:A]# SUS_STAT[2:1]#)
Clock Synthesizer	On	Off	Off	Off
Video Display	On	On/Off <sup>1</sup>	Off	Off
CPU	On	On	Off	Off
PIIX4E Core	On	On	Off	Off
Other Devices <sup>2</sup>	On	On	Off	Off
82443BX	On	On	On	Off
DRAM	On	On	On	Off
Graphics Controller	On	On	On	Off
PIIX4E Resume	On	On	On	On
PIIX4E RTC	On	On	On	On

**NOTES:**

1. The video display (flat panel or CRT) may optionally be powered off in POS. This could be accomplished by using the PIIX4E's SUSA# or SUS\_STAT2# signals to assert the video controller's STANDBY signal.
2. Devices may include mass storage, audio, or other devices that will not generate system resume events.

### 7.1.4.1 Power Well and Reset Signal Timings

Figure 19 shows the system timings for changing the power states of a system using the POS/STR/STD models.



### 7.1.4.2 PIIX4E Power Well Timings

Figure 19 describes the relative transitions for PIIX4E power supplies.

Figure 19. PIIX4E Power Well Timings

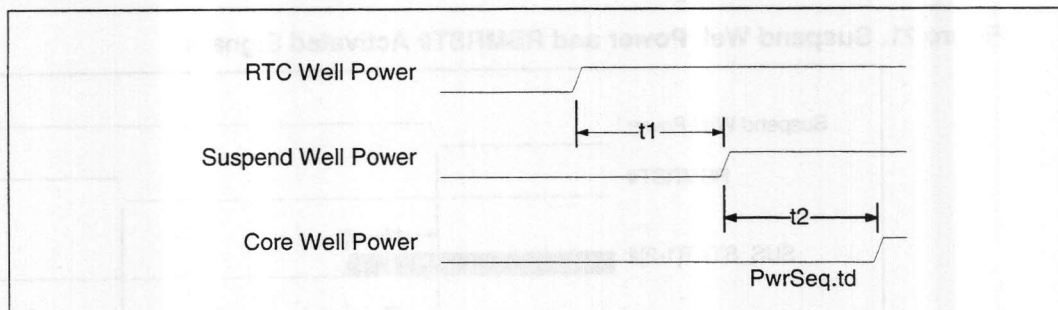


Table 31. PIIX4E Power Well Timings

Sym	Parameter	Min	Max	Unit	Notes
t1	RTC Well Power to Suspend Well Power	0		ns	
t2	Suspend Well Power to Core Well Power	0		ns	

### 7.1.4.3 RSMRST# and PWROK Timing

Figure 20 describes the required timings for PIIX4E power level active status signals.

Figure 20. RSMRST# and PWROK Timings

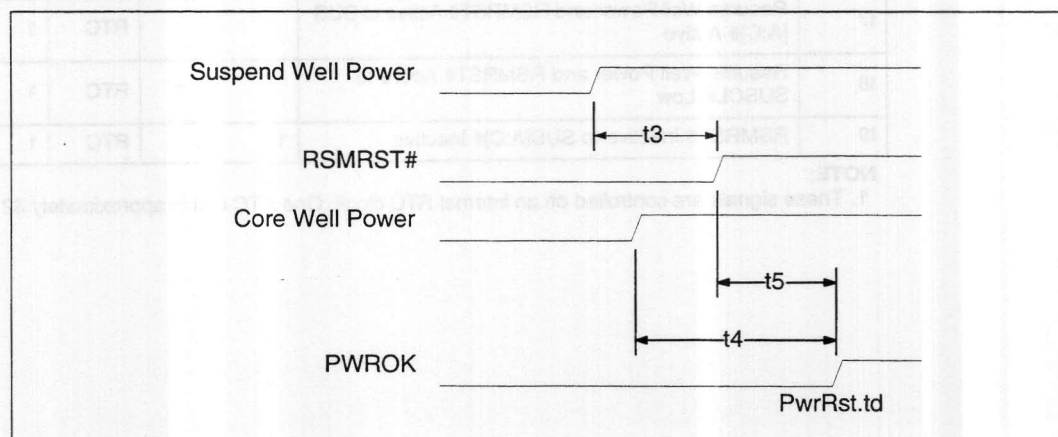


Table 32. RSMRST# and PWROK Timing

Sym	Parameter	Min	Max	Unit	Notes
t3	Suspend Well Power to RSMRST# Inactive	1		ms	
t4	Core Well Power to PWROK Active	1		ms	
t5	RSMRST# Inactive to PWROK Active	0		ns	



#### 7.1.4.4 Suspend Well Power and RSMRST# Activated Signals

This describes the timing relationships for the PIIX4E power management signals that are powered from the Suspend Power well. These timings hold independent of the condition of Core Well power or the PWROK signal.

Figure 21. Suspend Well Power and RSMRST# Activated Signals

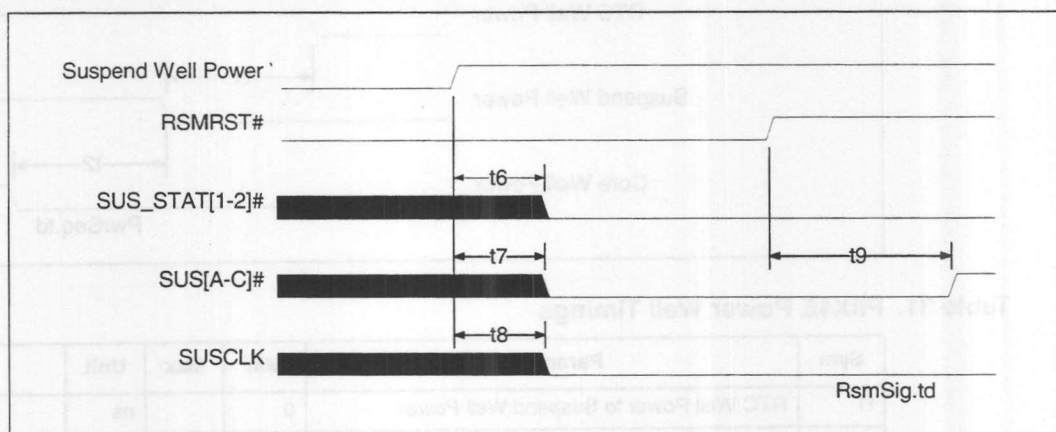


Table 33. Suspend Well Power and RSMRST# Timing

Sym	Parameter	Min	Max	Unit	Notes
t6	Resume Well Power and RSMRST# Active to SUS_STAT[1:2]# Active		1	RTC	1
t7	Resume Well Power and RSMRST# Active to SUS [A:C]# Active		1	RTC	1
t8	Resume Well Power and RSMRST# Active to SUSCLK Low		1	RTC	1
t9	RSMRST# Inactive to SUS[A:C]# Inactive	1	2	RTC	1

**NOTE:**

1. These signals are controlled off an internal RTC clock. One RTC unit is approximately 32  $\mu$ s.

### 7.1.4.5 PCI Clock Control Timings

This section describes the timing requirements for the control of the system PCICLK. The system PCICLK timing shown in Figure 22 must be followed exactly for proper operation of the PC/PCI DMA or Serial IRQ logic. When the PC/PCI DMA and Serial IRQs are not used in the system, the system PCICLK stop timings must meet the system developer's requirements.

Figure 22. PCI Clock Stop Timing

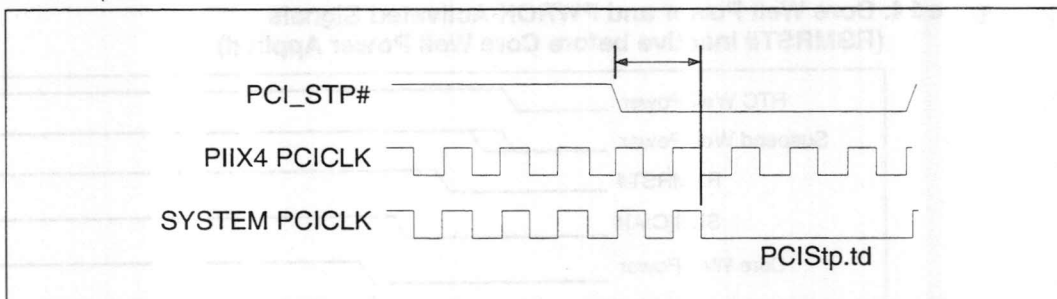
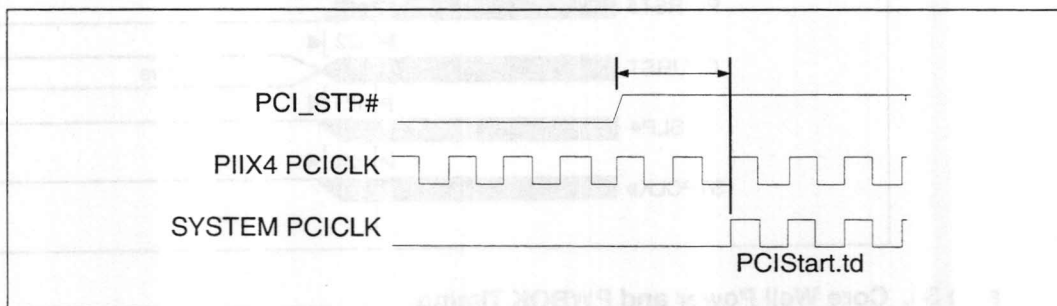


Figure 23 describes the timing requirements for the control of the system PCICLK. The system PCICLK timings shown Figure 23 must be followed exactly for proper operation of PC/PCI DMA or Serial IRQ logic. When PC/PCI DMA and Serial IRQs are not used in the system, the system PCICLK stop timings must meet system developers requirements.

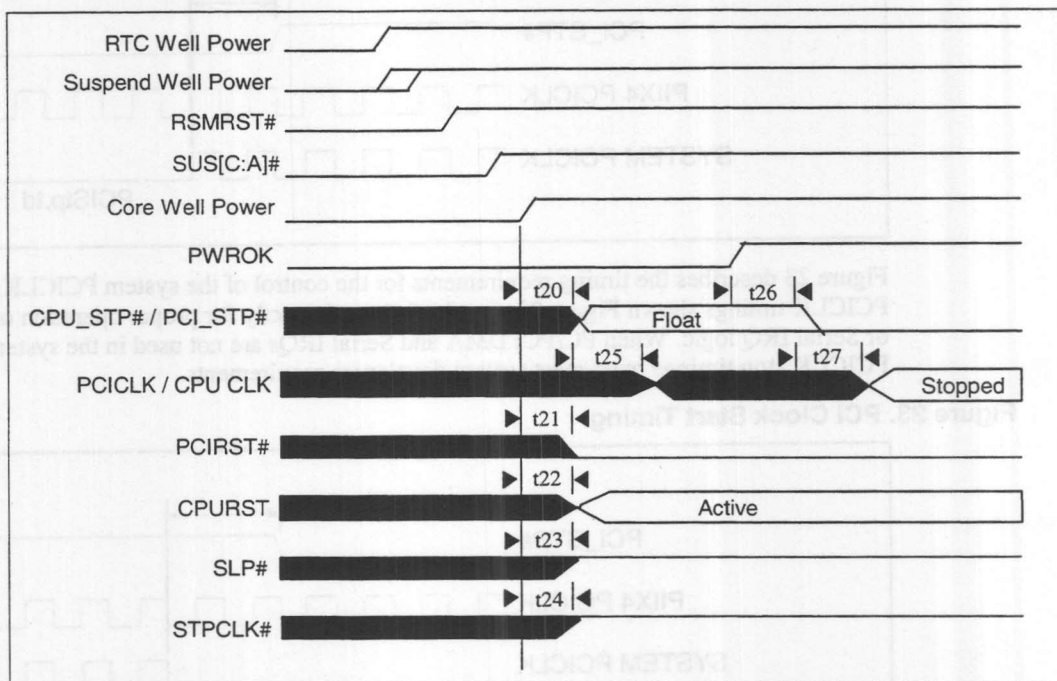
Figure 23. PCI Clock Start Timing



#### 7.1.4.6 Core Well Power and PWROK Activated Signals (RSMRST# Inactive Before Core Well Power Applied)

Figure 24 shows the timing relations for Power Management signals powered from the PIIX4E Main Core well. Here the Suspend well power active status signals (RSMRST#) transitions before the application of core well power to the PIIX4E. This figure corresponds to the usage model for PIIX4E power management.

**Figure 24. Core Well Power and PWROK Activated Signals (RSMRST# Inactive before Core Well Power Applied)**



**Table 34. Core Well Power and PWROK Timing**

Sym	Parameter	Min	Max	Unit	Notes
t20	Core Well Power and PWROK Inactive to CPU_STP# and PCI_STP# Float		1	RTC	1
t21	Core Well Power and PWROK Inactive to PCIRST# Active		1	RTC	1
t22	Core Well Power and PWROK Inactive to CPURST Active		1	RTC	1
t23	Core Well Power and PWROK Inactive to SLP# Active		1	RTC	1
t24	Core Well Power and PWROK Inactive to STPCLK# Active		1	RTC	1
t25	CPU_STP# and PCI_STP# Float to Clocks Running				2
t26	PWROK Active to CPU_STP# and PCI_STP# Active		1	RTC	1
t27	CPU_STP# and PCI_STP# Active to Clocks Stopped				2

**NOTES:**

1. These signals are controlled off an internal RTC clock. One RTC unit is approximately 32  $\mu$ s.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks on power up meet any other system specifications. As a minimum, the clocks must be available and stable after time t29 shown in Figure 26.



### 7.1.4.7 Core Well Power and PWROK Activated Signals (Core Well Power Applied Before RSMRST# Inactive)

Figure 25 shows the timing relations for Power Management signals powered from the PIIX4E Core well. Here the power active status signals (RSMRST# and PWROK) transition after the application of all power to the PIIX4E. This is an example of an implementation in which the Core Well power plane is not controlled by the SUSB# signal. It can be applied to situations where two or more of the PIIX4E power planes are connected together. It also shows timings when RSMRST# and PWROK are connected together.

**Figure 25. Core Well Power and PWROK Activated Signals (Core Well Power Applied before RSMRST# Inactive)**

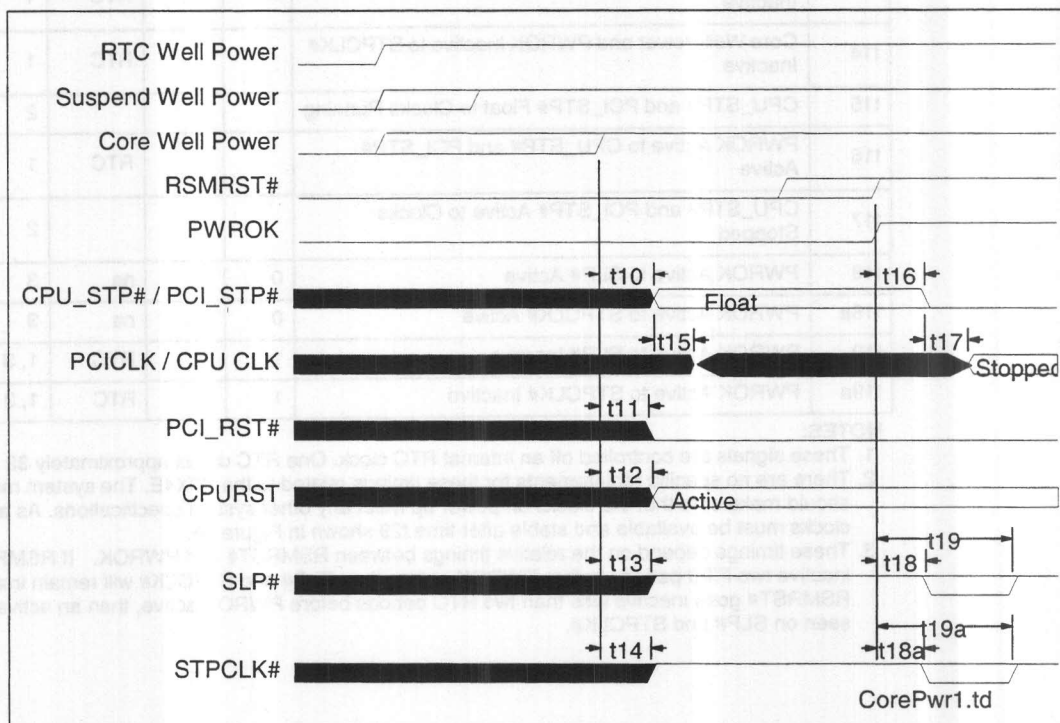


Table 35. Core Well Power and PWROK Timing

Sym	Parameter	Min	Max	Unit	Notes
t10	Core Well Power and PWROK Inactive to CPU_STP# and PCI_STP# Float		1	RTC	1
t11	Core Well Power and PWROK Inactive to PCIRST# Active		1	RTC	1
t12	Core Well Power and PWROK Inactive to CPURST Active		1	RTC	1
t13	Core Well Power and PWROK Inactive to SLP# Inactive		1	RTC	1
t14	Core Well Power and PWROK Inactive to STPCLK# Inactive		1	RTC	1
t15	CPU_STP# and PCI_STP# Float to Clocks Running				2
t16	PWROK Active to CPU_STP# and PCI_STP# Active		1	RTC	1
t17	CPU_STP# and PCI_STP# Active to Clocks Stopped				2
t18	PWROK Active to SLP# Active	0		ns	3
t18a	PWROK Active to STPCLK# Active	0		ns	3
t19	PWROK Active to SLP# Inactive	1	2	RTC	1, 3
t19a	PWROK Active to STPCLK# Inactive	1	2	RTC	1, 3

**NOTES:**

1. These signals are controlled off an internal RTC clock. One RTC unit is approximately 32  $\mu$ s.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks on power up meet any other system specifications. As a minimum, the clocks must be available and stable after time t29 shown in Figure 26.
3. These timings depend on the relative timings between RSMRST# and PWROK. If RSMRST# goes inactive two RTC periods before PWROK active, then SLP# and STPCLK# will remain inactive. If RSMRST# goes inactive less than two RTC periods before PWROK active, then an active pulse will be seen on SLP# and STPCLK#.

## 7.1.5 Power Management State Transition Timings

### 7.1.5.1 Mechanical Off to On

Figure 26 shows the transition from a Mechanical Off condition to the On condition.

Figure 26. Mechanical Off to On

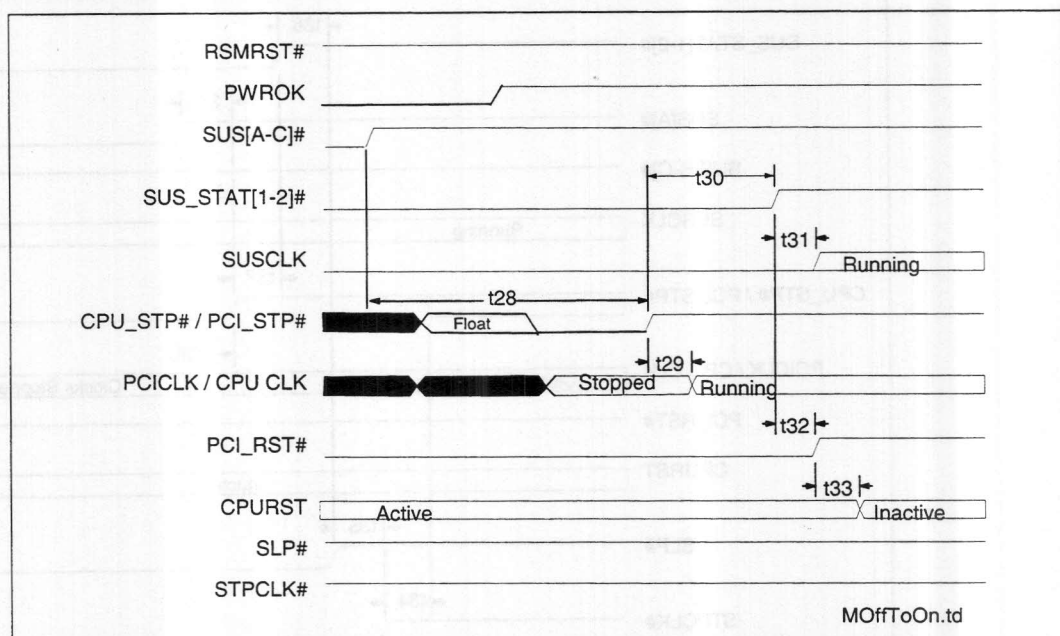


Table 36. Mechanical Off to On Timing

Sym	Parameter	Min	Max	Unit	Notes
t28	SUS[A:C]# Inactive to CPU_STP# and PCI_STP# Inactive	16		ms	1
t29	CPU_STP# and PCI_STP# Inactive to Clocks Running		2	PCICLK	2
t30	CPU_STP# and PCI_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t31	SUS_STAT[1:2]# Inactive to SUSCLK Running		1	RTC	3
t32	SUS_STAT[1:2]# Inactive to PCI_RST# Inactive		1	RTC	3
t33	PCI_RST# Inactive to CPURST Inactive		1	RTC	3

**NOTES:**

1. This transition requires a minimum of 16 ms wait for the clock synthesizer PLL to lock and PWROK to be active. If PWROK goes active after 16 ms from SUS[A:C]# inactive, the transition occurs a minimum of one RTC period from PWROK active.
2. See Table 22 and Table 23 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.
3. These signals are controlled from an internal RTC clock. One RTC unit is approximately 32  $\mu$ s.

## 7.1.5.2 On to POS

Figure 27 describes the signal transitions from the On state to the Power On Suspend state.

Figure 27. On to POS

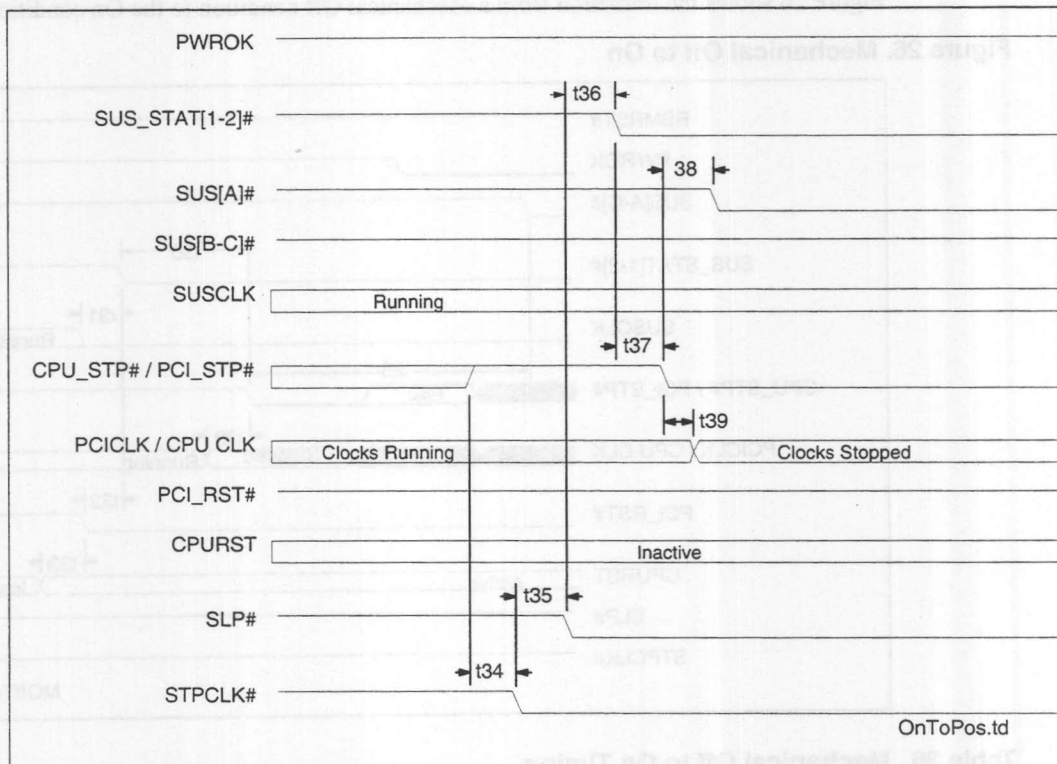


Table 37. On to POS Timing

Sym	Parameter	Min	Max	Unit	Notes
t34	CPU_STP# and PCI_STP# Inactive to STPCLK# Active	1		RTC	1, 2
t35	STPCLK# Active to SLP# Active	1		RTC	1, 3
t36	SLP# Active to SUS_STAT[1:2]# Active		1	RTC	1
t37	SUS_STAT[1:2]# Active to CPU_STP# and PCI_STP# Active		1	RTC	1
t38	CPU_STP# and PCI_STP# Active to SUS[A]# Active		1	RTC	1
t39	CPU_STP# and PCI_STP# Active to Clocks Stopped (if applicable)		2	PCICLK	4, 5

**NOTES:**

- These signals are controlled from an internal RTC clock. One RTC unit is approximately 32  $\mu$ s.
- CPU\_STP# and PCI\_STP# will only be active when the system is under clock control.
- This transition waits for the Stop Grant cycle to execute.
- It is up to the system vendor to determine whether CPU\_STP# and PCI\_STP# signals are used to control system clocks.
- See Table 22 and Table 23 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.



### 7.1.5.3 POS to On (with Processor and PCI Reset)

Figure 28 describes the system transition from Power On Suspend to On with a full system reset.

Figure 28. POS to On (with Processor and PCI Reset)

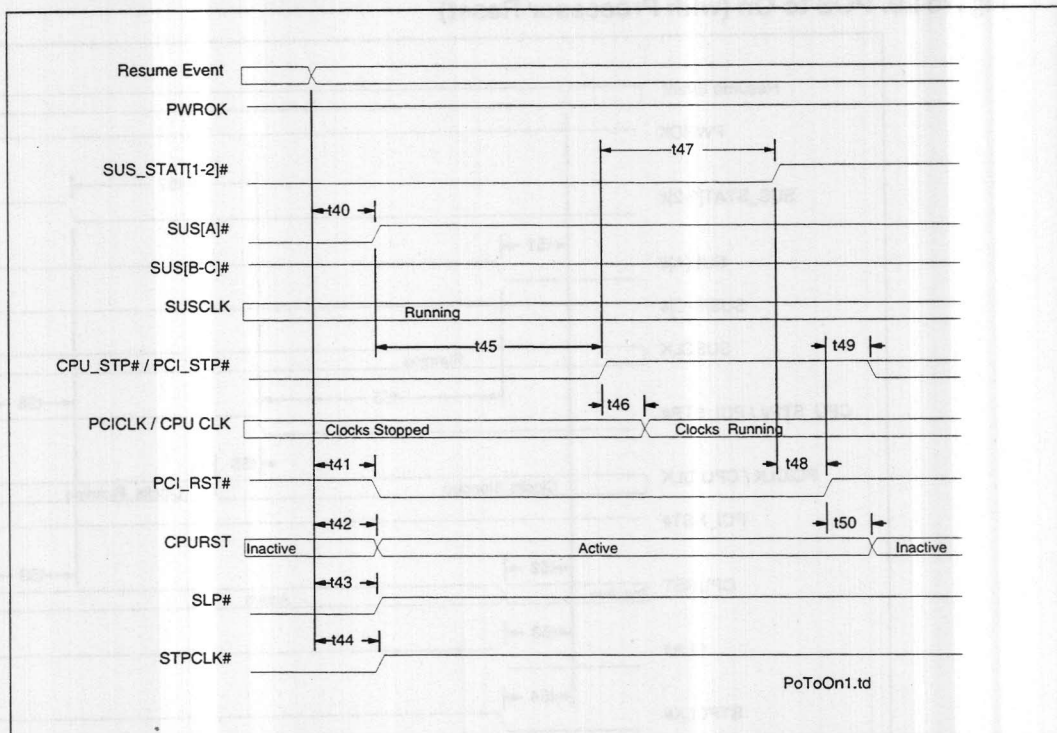


Table 38. POS to On Timing

Sym	Parameter	Min	Max	Unit	Notes
t40	Resume Event to SUS[A]# Inactive	1		RTC	1
t41	Resume Event to PCI_RST# Active	1		RTC	1
t42	Resume Event to CPURST Active	1		RTC	1
t43	Resume Event to SLP# Inactive	1		RTC	1
t44	Resume Event to STPCLK# Inactive	1		RTC	1
t45	SUS[A]# Inactive to PCI_STP# and CPU_STP# Inactive	16		ms	2
t46	PCI_STP# and CPU_STP# Inactive to Clocks Running		2	PCICLK	3
t47	PCI_STP# and CPU_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t48	SUS_STAT[1:2]# Inactive to PCI_RST# Inactive		1	RTC	1
t49	PCI_RST# Inactive to PCI_STP# and CPU_STP# allowed to change		1	RTC	1
t50	PCI_RST# Inactive to CPURST Inactive		1	RTC	1

**NOTES:**

1. These signals are controlled from an internal RTC clock. One RTC unit is approximately 32  $\mu$ s.
2. This transition requires a minimum of 16 ms wait for the clock synthesizer PLL to lock and PWROK to be active. If PWROK goes active after 16 ms from SUS[A:C]# inactive, the transition will occur a minimum of one RTC period from PWROK active. PWROK remains active throughout POS system usage.
3. See Table 22 and Table 23 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.

### 7.1.5.4 POS to On (with Processor Reset)

Figure 29 describes the system transition from Power On Suspend (POS) to On with only a processor reset.

Figure 29. POS to On (with Processor Reset)

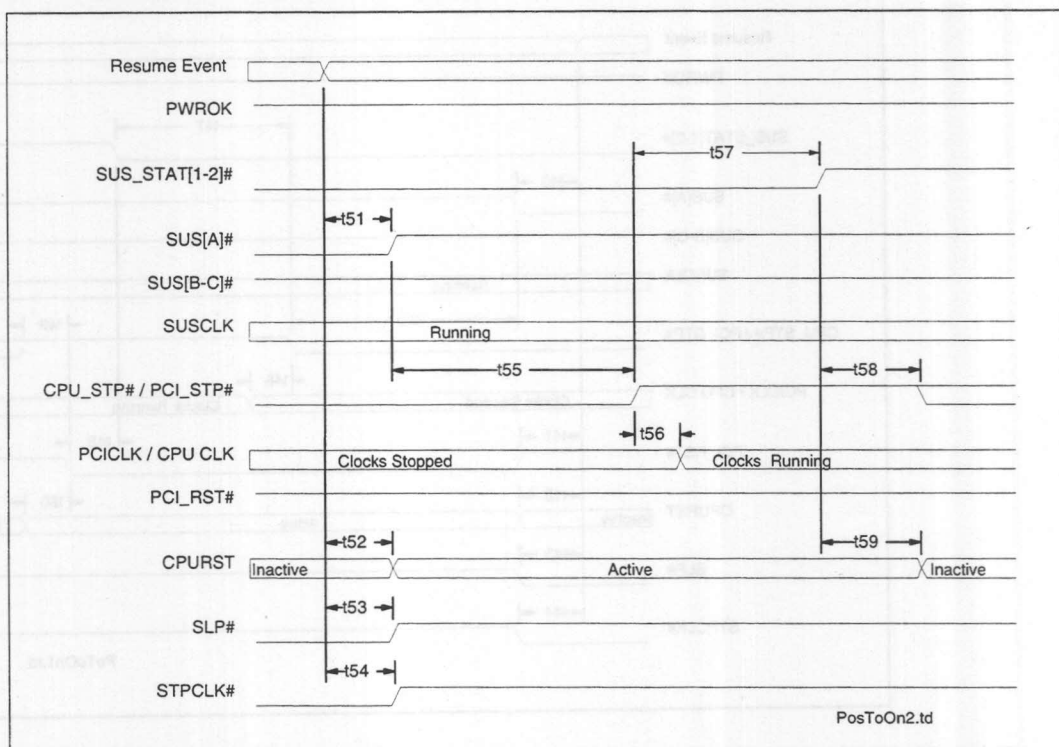


Table 39. POS to On (with Processor Reset) Timing (Sheet 1 of 2)

Sym	Parameter	Min	Max	Unit	Notes
t51	Resume Event to SUS[A]# Inactive	1		RTC	1
t52	Resume Event to CPURST Active	1		RTC	1
t53	Resume Event to SLP# Inactive	1		RTC	1
t54	Resume Event to STPCLK# Inactive	1		RTC	1
t55	SUS[A]# Inactive to PCI_STP# and CPU_STP# Inactive	16		ms	2
t56	PCI_STP# and CPU_STP# Inactive to Clocks Running		2	PCICLK	3

**NOTES:**

1. These signals are controlled from an internal RTC clock. One RTC unit is approximately 32  $\mu$ s.
2. This transition requires both a minimum of 16 ms wait for the clock synthesizer PLL to lock and PWROK to be active. If PWROK goes active after 16 ms from SUS[A:C]# inactive, the transition will occur a minimum of one RTC period from PWROK active. PWROK remains active throughout POS system usage.
3. See Table 22 and Table 23 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.

Table 39. POS to On (with Processor Reset) Timing (Sheet 2 of 2)

Sym	Parameter	Min	Max	Unit	Notes
t57	PCI_STP# and CPU_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t58	SUS_STAT[1:2]# Inactive to PCI_STP# and CPU_STP# allowed to change		2	RTC	1
t59	SUS_STAT[1:2]# Inactive to CPURST Inactive		2	RTC	1

**NOTES:**

- These signals are controlled from an internal RTC clock. One RTC unit is approximately 32  $\mu$ s.
- This transition requires both a minimum of 16 ms wait for the clock synthesizer PLL to lock and PWROK to be active. If PWROK goes active after 16 ms from SUS[A:C]# inactive, the transition will occur a minimum of one RTC period from PWROK active. PWROK remains active throughout POS system usage.
- See Table 22 and Table 23 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.

### 7.1.5.5 POS to On (No Reset)

Figure 30 describes the system transition from Power On Suspend to On with no resets performed.

Figure 30. POS to On (No Reset)

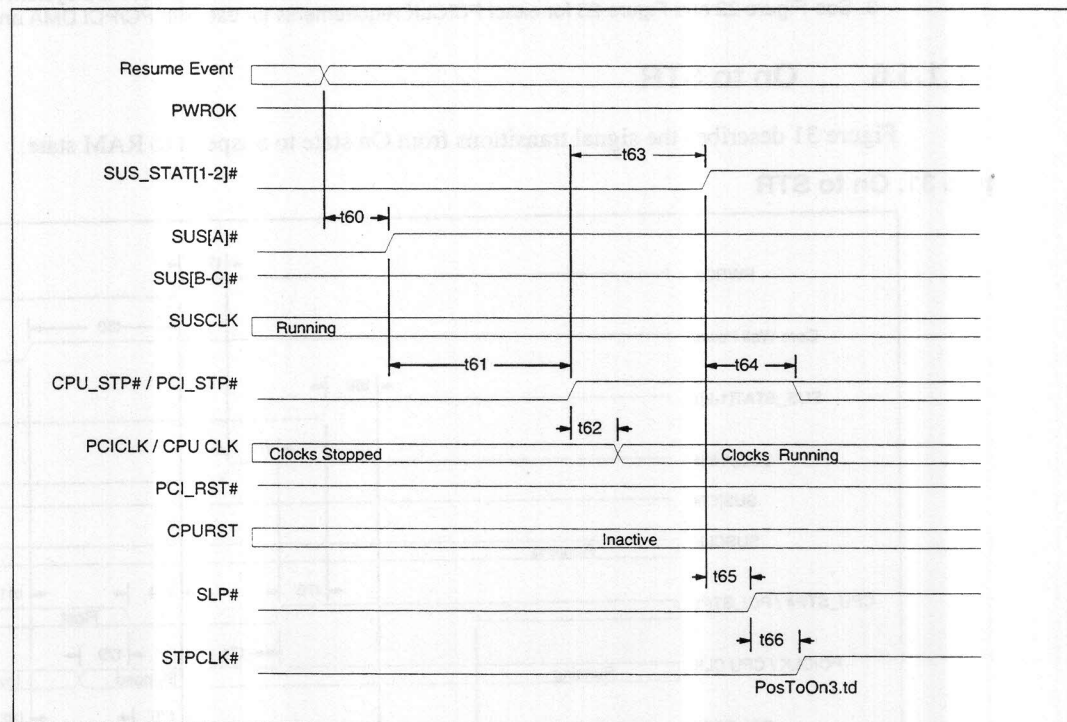




Table 40. POS to On (No Reset) Timing

Sym	Parameter	Min	Max	Unit	Notes
t60	Resume Event to SUS[A]# Inactive	1		RTC	1
t61	SUS[A]# Inactive to PCI_STP# and CPU_STP# Inactive	16		ms	2
t62	PCI_STP# and CPU_STP# Inactive to Clocks Running		2	PCICLK	3
t63	PCI_STP# and CPU_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t64	SUS_STAT[1:2]# Inactive to PCI_STP# and CPU_STP# allowed to change		2	RTC	1
t65	SUS_STAT[1:2]# Inactive to SLP# Inactive		1	RTC	1
t66	SLP# Inactive to STPCLK# Inactive		1	RTC	1

**NOTES:**

1. These signals are controlled from the internal RTC clock. One RTC is approximately 32  $\mu$ s.
2. This transition requires both a minimum of 16 ms wait for the clock synthesizer PLL to lock and PWROK to be active. If PWROK goes active after 16 ms from SUS[A:C]# inactive, the transition will occur a minimum of one RTC period from PWROK active. PWROK remains active throughout POS system usage.
3. See Figure 22 and Figure 23 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.

### 7.1.5.6 On to STR

Figure 31 describes the signal transitions from On state to Suspend to RAM state.

Figure 31. On to STR

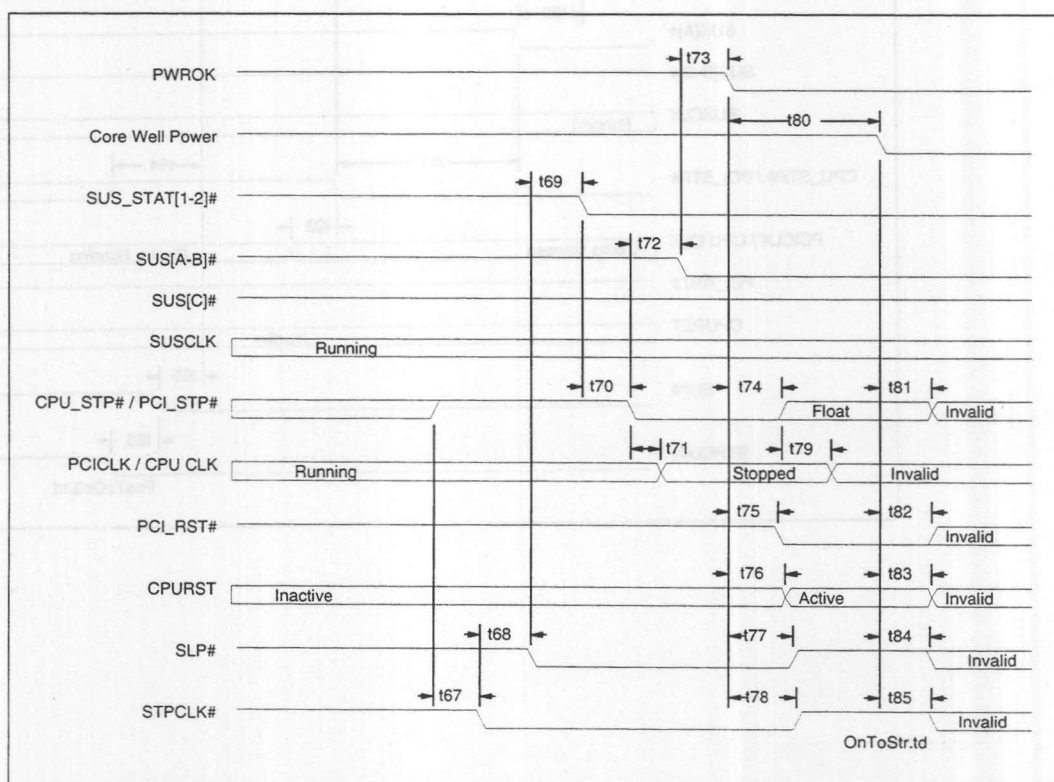




Table 41. On to STR Timing

Sym	Parameter	Min	Max	Unit	Notes
t67	CPU_STP# and PCI_STP# Inactive to STPCLK# Active	1		RTC	1, 2
t68	STPCLK# Active to SLP# Active	1		RTC	1, 3
t69	SLP# Active to SUS_STAT[1:2]# Active		1	RTC	1
t70	SUS_STAT[1:2]# Active to CPU_STP# and PCI_STP# Active		1	RTC	1
t71	CPU_STP# and PCI_STP# Active to CLOCKS Stopped		2	PCICLK	4, 5
t72	CPU_STP# and PCI_STP# Inactive to SUS[A:B]# Active		1	RTC	1
t73	SUS[A:B]# Active to PWROK Inactive	0		ns	6
t74	PWROK Inactive to CPU_STP# and PCI_STP# Float		1	RTC	1
t75	PWROK Inactive to PCI_RST# Active		1	RTC	1
t76	PWROK Inactive to CPURST Active		1	RTC	1
t77	PWROK Inactive to SLP# Inactive		1	RTC	1
t78	PWROK Inactive to STPCLK# Inactive		1	RTC	1
t79	CPU_STP# and PCI_STP# Float to Clocks Invalid	0		ns	7
t80	PWROK Inactive to Core Well Power Removed	0		ns	
t81	Core Well Power Removed to PCI_STP# and CPU_STP# Invalid	0		ns	
t82	Core Well Power Removed to PCIRST# Invalid	0		ns	
t83	Core Well Power Removed to CPURST Invalid	0		ns	
t84	Core Well Power Removed to SLP# Invalid	0		ns	
t85	Core Well Power Removed to STPCLK# Invalid	0		ns	

**NOTES:**

1. These signals are controlled from the internal RTC clock. One RTC is approximately 32  $\mu$ s.
2. CPU\_STP# and PCI\_STP# will only be active if the system is under clock control.
3. This transition will also wait for the Stop Grant cycle to execute.
4. It is up to the system vendor to determine if CPU\_STP# and PCI\_STP# signals are used to control system clocks.
5. See Figure 22 and Figure 23 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.
6. It is up to the system vendor to determine if SUS[A:B]# signals are used to control system power planes. If power remains applied to system board and PWROK stays active during STR, the PIIX4E signals will remain in the states shown after t73.
7. Clocks may or may not be running depending on the condition of the Power Supply voltages.

## 7.1.5.7 STR to On

Figure 32 describes the system transition from Suspend To RAM to On with a full system reset.

Figure 32. STR to On

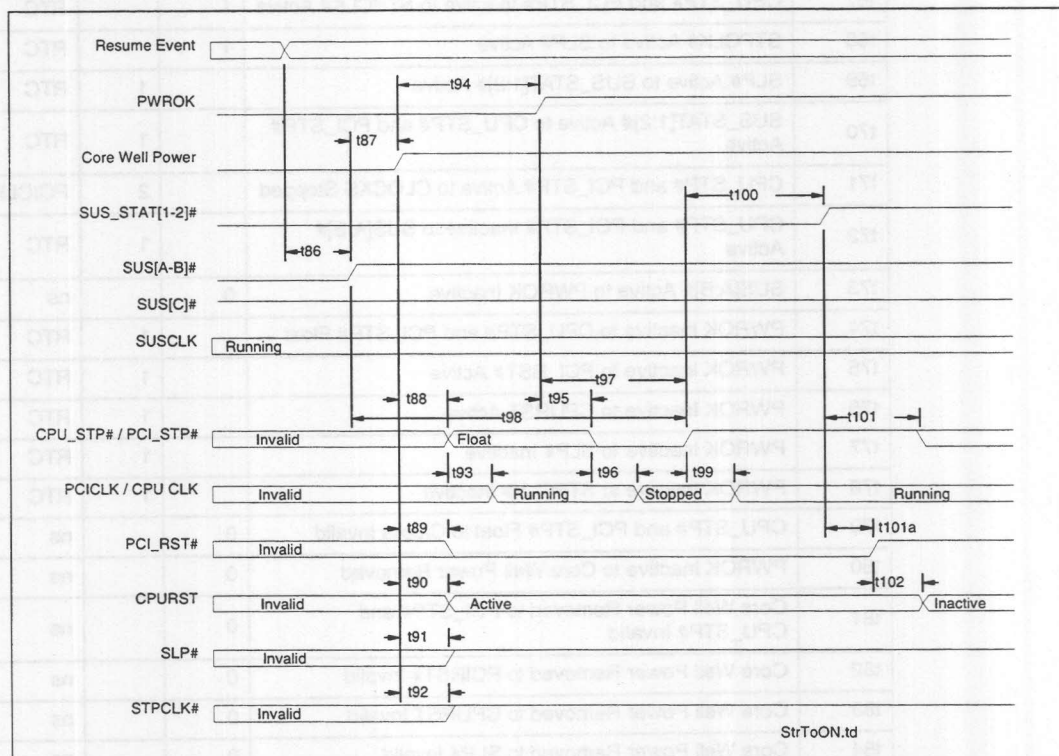


Table 42. STR to On Timing (Sheet 1 of 2)

Sym	Parameter	Min	Max	Unit	Notes
t86	Resume Event to SUS[A:B]# Inactive	1		RTC	1
t87	SUS[A:B]# Inactive to Core Well Power Applied	0		ns	
t88	Core Well Power Applied to PCI_STP# and CPU_STP# Float	0		ns	
t89	Core Well Power Applied to PCI_RST# Active	0		ns	
t90	Core Well Power Applied to CPURST Active	0		ns	
t91	Core Well Power Applied to SLP# Inactive	0		ns	
t92	Core Well Power Applied to STPCLK# Inactive	0		ns	
t93	PCI_STP# and CPU_STP# Float to Clocks Running				2
t94	Core Well Power Applied to PWROK Active	1		ms	

## NOTES:

- These signals are controlled from the internal RTC clock. One RTC is approximately 32  $\mu$ s.
- There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks meet any other system specifications upon power up. At a minimum, the clocks must be available and stable after time t99.
- See Figure 22 and Figure 23 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.

Table 42. STR to On Timing (Sheet 2 of 2)

Sym	Parameter	Min	Max	Unit	Notes
t95	PWROK Active to CPU_STP# and PCI_STP# Active	0		ns	
t96	PCI_STP# and CPU_STP# Active to Clocks Stopped		2	PCICLK	3
t97	PWROK Active to CPU_STP# and PCI_STP# Inactive	1		RTC	1
t98	SUS[A-B]# Inactive to CPU_STP# and PCI_STP# Inactive	16		ms	
t99	CPU_STP# and PCI_STP# Inactive to Clocks Running		2	PCICLK	3
t100	CPU_STP# and PCI_STP# Inactive to SUS_STAT[1-2]# Inactive	1		ms	
t101	SUS_STAT[1-2]# Inactive to CPU_STP# and PCI_STP# allowed to change	2		RTC	1
t101a	SUS_STAT[1-2]# Inactive to PCI_RST# Inactive	1		RTC	1
t102	PCI_RST# Inactive to CPURST Inactive	1		RTC	1

**NOTES:**

1. These signals are controlled from the internal RTC clock. One RTC is approximately 32  $\mu$ s.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks meet any other system specifications upon power up. At a minimum, the clocks must be available and stable after time t99.
3. See Figure 22 and Figure 23 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.



## 7.1.5.8 On to STD/SOff

Figure 33 describes the signal transitions from the On state to the Suspend to Disk/Soft Off state.

Figure 33. On to STD/SOff

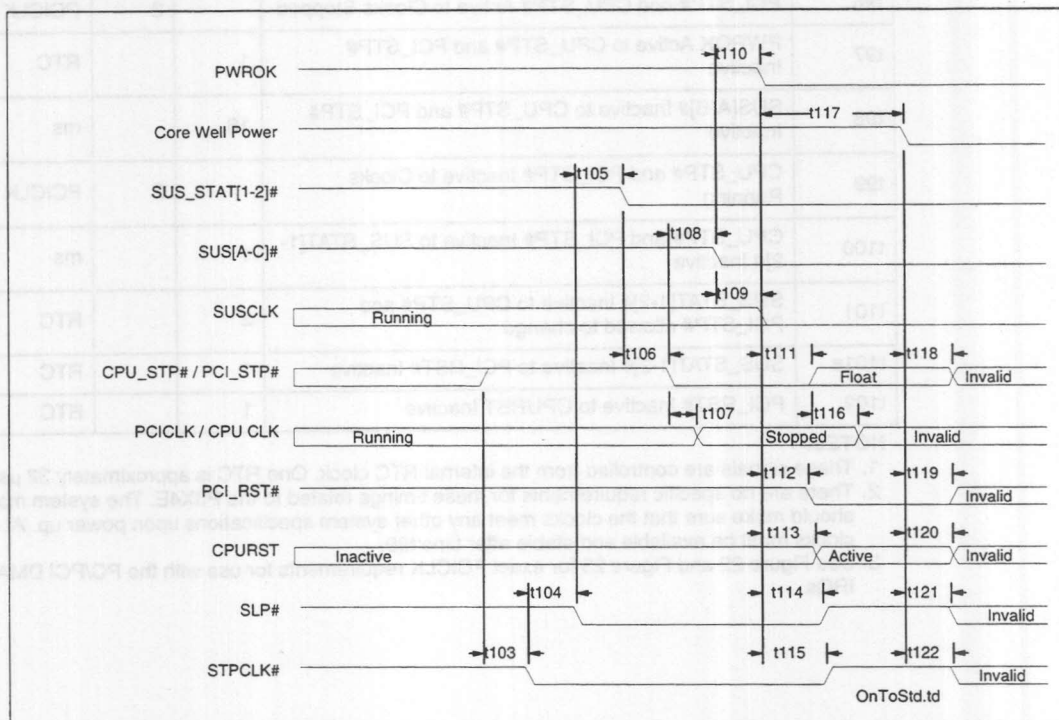


Table 43. On to STD/SOff Timing (Sheet 1 of 2)

Sym	Parameter	Min	Max	Unit	Notes
t103	CPU_STP# and PCI_STP# Inactive to STPCLK# Active	1		RTC	1, 2
t104	STPCLK# Active to SLP# Active	1		RTC	1, 3
t105	SLP# Active to SUS_STAT[1:2]# Active		1	RTC	1
t106	SUS_STAT[1:2]# Active to CPU_STP# and PCI_STP# Active		1	RTC	1
t107	CPU_STP# and PCI_STP# Inactive to CLOCKS Stopped		2	PCICLK	1, 4, 5

**NOTES:**

1. These signals are controlled from the internal RTC clock. One RTC is approximately 32  $\mu$ s.
2. CPU\_STP# and PCI\_STP# will only be active if the system is under clock control.
3. This transition will also wait for the Stop Grant cycle to execute.
4. It is up to the system vendor to determine if CPU\_STP# and PCI\_STP# signals are used to control system clocks.
5. See Figure 22 and Figure 23 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.
6. It is up to the system vendor to determine if SUS[A:C]# signals are used to control system power planes. If the power remains applied to the system board and the PWROK stays active during STD, the PII4E signals will remain in the states shown after t110.



Table 43. On to STD/SOff Timing (Sheet 2 of 2)

Sym	Parameter	Min	Max	Unit	Notes
t108	CPU_STP# and PCI_STP# Inactive to SUS[A:C]# Active		1	RTC	1
t109	SUS[A:C]# Active to SUSCLK Low		1	RTC	1
t110	SUS[A:C]# Active to PWROK Inactive	0		ns	6
t111	PWROK Inactive to CPU_STP# and PCI_STP# Float		1	RTC	1
t112	PWROK Inactive to PCI_RST# Active		1	RTC	1
t113	PWROK Inactive to CPURST Active		1	RTC	1
t114	PWROK Inactive to SLP# Inactive		1	RTC	1
t115	PWROK Inactive to STPCLK# Inactive		1	RTC	1
t116	CPU_STP# and PCI_STP# Float to Clocks Invalid	0		ns	1
t117	PWROK Inactive to Core Well Power Removed	0		ns	
t118	Core Well Power Removed to PCI_STP# and CPU_STP# Invalid	0		ns	
t119	Core Well Power Removed to PCIRST# Invalid	0		ns	
t120	Core Well Power Removed to CPURST Invalid	0		ns	
t121	Core Well Power Removed to SLP# Invalid	0		ns	
t122	Core Well Power Removed to STPCLK# Invalid	0		ns	

**NOTES:**

- These signals are controlled from the internal RTC clock. One RTC is approximately 32  $\mu$ s.
- CPU\_STP# and PCI\_STP# will only be active if the system is under clock control.
- This transition will also wait for the Stop Grant cycle to execute.
- It is up to the system vendor to determine if CPU\_STP# and PCI\_STP# signals are used to control system clocks.
- See Figure 22 and Figure 23 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.
- It is up to the system vendor to determine if SUS[A:C]# signals are used to control system power planes. If the power remains applied to the system board and the PWROK stays active during STD, the PIIX4E signals will remain in the states shown after t110.

## 7.1.5.9 STD/SOff to On

Figure 34 describes the system transition from Suspend To Disk to On with a full system reset.

Figure 34. STD/SOff to On

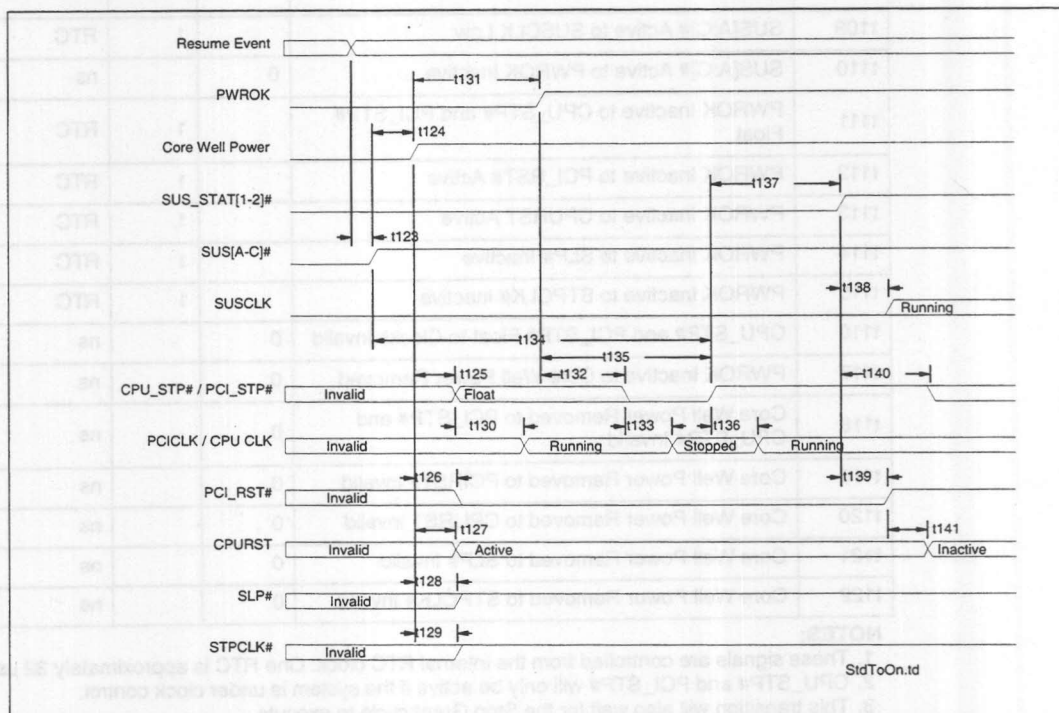


Table 44. STD/SOff to On Timing (Sheet 1 of 2)

Sym	Parameter	Min	Max	Unit	Notes
t123	Resume Event to SUS[A:C]# Inactive	1		RTC	1
t124	SUS[A-C]# Inactive to Core Well Power Applied	0		ns	
t125	Core Well Power Applied to PCI_STP# and CPU_STP# Float	0		ns	
t126	Core Well Power Applied to PCI_RST# Active	0		ns	
t127	Core Well Power Applied to CPURST Active	0		ns	
t128	Core Well Power Applied to SLP# Inactive	0		ns	
t129	Core Well Power Applied to STPCLK# Inactive	0		ns	
t130	PCI_STP# and CPU_STP# Float to Clocks Running				2
t131	Core Well Power Applied to PWROK Active	1		ms	

1. These signals are controlled from the internal RTC clock. One RTC is approximately 32  $\mu$ s.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks on power up meet any other system specifications. At a minimum, the clocks must be available and stable after time t136.
3. See Figure 22 and Figure 23 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.

Table 44. STD/SOff to On Timing (Sheet 2 of 2)

Sym	Parameter	Min	Max	Unit	Notes
t132	PWROK Active to CPU_STP# and PCI_STP# Active	0		ns	
t133	PCI_STP# and CPU_STP# Active to Clocks Stopped		2	PCICLK	3
t134	SUS[A-C]# Inactive to CPU_STP# and PCI_STP# Inactive	16		ms	
t135	PWROK Active to CPU_STP# and PCI_STP# Inactive	1		RTC	1
t136	PCI_STP# and CPU_STP# Active to Clocks Running	1	2	PCICLK	3
t137	CPU_STP# and PCI_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t138	SUS_STAT[1:2]# Inactive to SUSCLK Running		1	RTC	1
t139	SUS_STAT[1:2]# Inactive to PCI_RST# Inactive	1		RTC	1
t140	SUS_STAT[1:2]# Inactive to CPU_STP# and PCI_STP# allowed to change	2		RTC	1
t141	PCI_RST# Inactive to CPURST Inactive	1		RTC	1

1. These signals are controlled from the internal RTC clock. One RTC is approximately 32  $\mu$ s.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks on power up meet any other system specifications. At a minimum, the clocks must be available and stable after time t136.
3. See Figure 22 and Figure 23 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.

## 7.2 82443BX Host Bridge Controller Power Sequencing

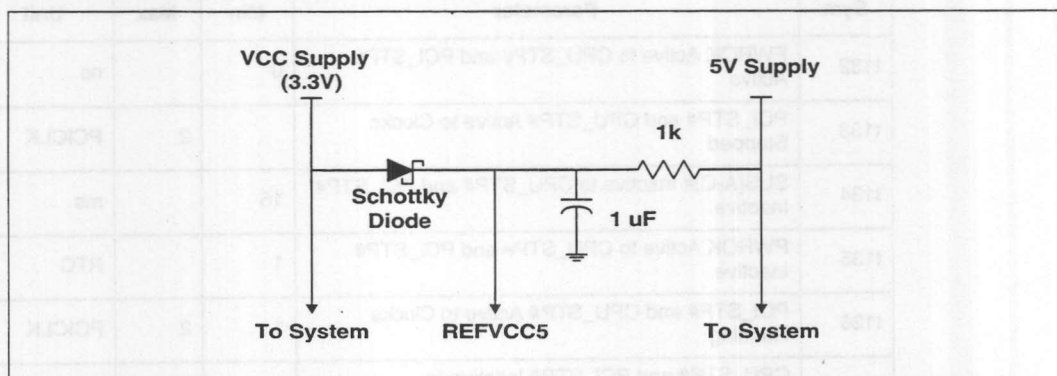
### 7.2.1 Power Sequencing Requirements

In systems requiring 5-V tolerance, the REFVCC5 signal must be tied to 5-V. This signal must power up before or simultaneous to  $V_{CC}$ . It must power down after or simultaneous to  $V_{CC}$ . In a non-5-V tolerant system (3.3-V only), this signal can be tied directly to  $V_{CC}$ . There are then no sequencing requirements. Refer to Figure 35 for an example circuit schematic that may be used to ensure the proper REFVCC5 sequencing. This is the same circuit that is recommended for the PIIX4E VREF supply. However, different power planes may supply the PIIX4E core and the 82443BX Host Bridge controller (the PIIX4E core may be powered down during STR). In this case a separate circuit must be used for each of the two devices.

$V_{CC}$  must power up before or simultaneous to the AGP supplies ( $V_{CC\_AGP}$  and  $AGP\_REF$ ) and Low Power GTL+ supplies ( $V_{TT}$  and  $GTL\_REF$ ).  $V_{CC}$  must power down after or simultaneous to the AGP and Low Power GTL+ supplies. The AGP and Low Power GTL+ supplies must not be powered up while  $V_{CC}$  is powered down. There are no other power sequencing requirements for the 82443BX Host Bridge controller.



Figure 35. REFVCC5 Supply Circuit Schematic



## 7.2.2 440BX AGPset Power Management

The 440BX AGPset supports a variety of system-wide low-power modes using the following functions:

- Hardware interface with the PIIX4E that is used to indicate:
  - Suspend mode entry
  - Resume from suspend
  - Whether to automatically switch from suspend to normal refresh
- Automatic transition from normal to suspend refresh
- Optional automatic transition from suspend to normal refresh
- Optional CPU reset during resume from Power On Suspend (POS)
- Variety of Suspend refresh types:
  - Self Refresh for SDRAMs
  - Optional Self Refresh for EDO
  - Optional CAS Before RAS (CBR) refresh for EDO. An Integrated Ring oscillator is used to provide the time base for the associated logic.
  - Programmable slow refresh (relevant for CBR refresh only)
- Isolated I/O pins to significantly reduce power consumption while in POS and STR modes

Based on the above functions, the 440BX AGPset recognizes the following system-wide low power modes:

- STR and POS suspend entry and exit are generally handled in the same manner. The following exceptions are related to POS mode:
  - The POS resume sequence may or may not include a processor reset. STR, with PCIRST# active always includes a processor reset.
  - The POS resume sequence requires a hardware transition from suspend to a normal refresh. STR with PCIRST# active requires a software initiated transition.
- STD resume is handled in the same way as the power on sequence, including a complete reset of the 440BX AGPset state.

### 7.2.2.1 System Power Modes

The following table provides an overview of how the above features map into system-wide low power modes.

**Table 45. System-wide Low-power Modes**

System Suspend State	82443BX State	Description	POS Exit PCIRST	External Clk HCLK PCLK	
Power On	ON	82443BX is fully on and operating normally. Internal clock gating as well as PCI CLKRUN# may be enabled.	N/A	Active	Active
CPU STOP_GRANT or QUICK_START (C2)	ON	This is transparent to the 82443BX since the external HCLK and PCLK are unaffected. The Host Bus is Idle. Internal clock gating and PCI CLKRUN# may be enabled.	N/A	Active	Active
CPU STOP CLOCK (C3) (DEEP SLEEP)	POS	System PLLs remain powered, but are disabled. HCLK clock is kept low. The only guaranteed running clock is SUSCLK. The 82443BX maintains DRAM refresh using suspend refresh. The 82443BX's internal PLLs are disabled. The 82443BX PCI and AGP arbiters are disabled.	N	Low	Low or Active
Power On Suspend (POS)	POS	System PLLs are powered down. The only running clock is the RTC clock and SUSCLK. The 82443BX maintains DRAM refresh using suspend refresh. The 82443BX's PLLs are disabled. The 82443BX PCI and AGP arbiters are disabled. When resumed, the 82443BX may or may not generate a processor reset. All 82443BX logic, with the exception of resume and refresh, are inactive.	Y	Low	Low
Suspend to RAM (STR)	POS	The processor and other components (with the exception of the DRAM and PIIX4E resume logic) are assumed to be powered OFF. The 82443BX V <sub>CC</sub> supply is on and all I/O buffers are isolated (with the exception of suspend and DRAM signals). The 82443BX Low Power GTL+ supplies should be powered down with the processor. The 82443BX maintains DRAM refresh using a suspend refresh. All 82443BX logic, with the exception of resume and refresh, are inactive.	Y	Low	Low
Suspend -to-Disk (STD) or Powered-Off	OFF	The entire system is powered OFF except for the PIIX4E resume and RTC wells. Upon resume, the 82443BX resets its entire state.	N/A	X	X

**NOTE:** The processor will generally be powered off during STR (the processor voltage regulator will be controlled by the PIIX4E's SUSB# signal). In this case, the 82443BX Low Power GTL+ supply (VTT and GTL\_REF) should also be controlled by SUSB#, and hence be powered off during STR.

### 7.2.2.2 System Power-up Sequencing

The following waveforms show the powerup sequence and timing information for the 440BX AGPset.

Figure 36. System Power-up Sequencing

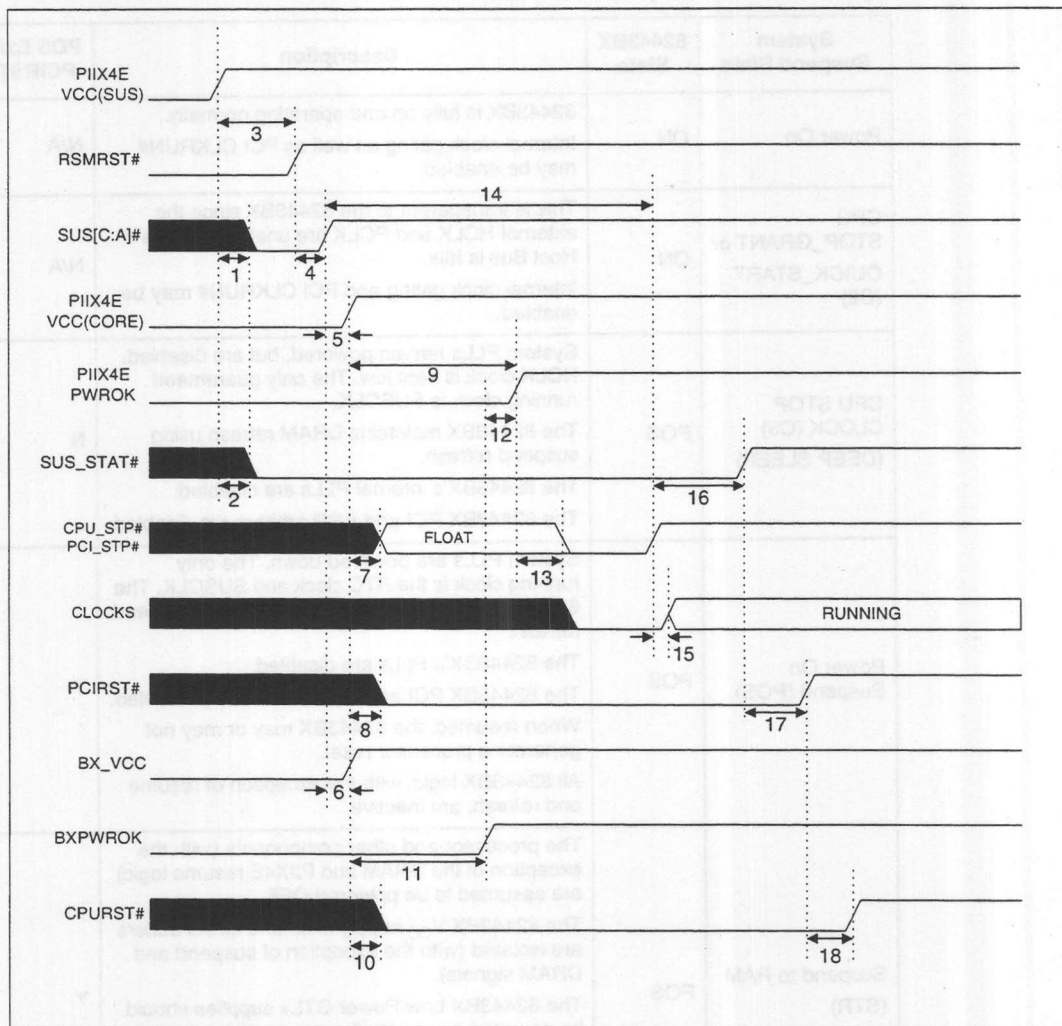




Table 46. System Power-up Sequencing Timing

Sym	Parameter	Min	Max	Units	Notes
t <sub>1</sub>	PIIX4E VCC(SUS) nominal to SUS[C:A]# active		1	RTC	1
t <sub>2</sub>	PIIX4E VCC(SUS) nominal to SUS_STAT[2:1]# active		1	RTC	1
t <sub>3</sub>	PIIX4E VCC(SUS) nominal to RSMRST# active	1		ms	
t <sub>4</sub>	RSMRST# inactive to SUS[C:A]# inactive	1	2	RTC	1
t <sub>5</sub>	SUS[B]# inactive to PIIX4E VCC(CORE) nominal	0		ms	
t <sub>6</sub>	SUS[C]# inactive to BX_VCC nominal	0		ms	
t <sub>7</sub>	PIIX4E VCC(CORE) nominal to CPU_STP#, PCI_STP# float		1	RTC	1
t <sub>8</sub>	PIIX4E VCC(CORE) nominal to PCIRST# active		1	RTC	1
t <sub>9</sub>	PIIX4E VCC(CORE) nominal to PIIX4E PWROK active	1		ms	
t <sub>10</sub>	BX_VCC nominal to CPURST# active		10	ns	
t <sub>11</sub>	BX_VCC nominal to BXPWROK active	1		ms	
t <sub>12</sub>	BXPWROK active to PIIX4E PWROK active	0		ns	2
t <sub>13</sub>	PIIX4E PWROK active to CPU_STP#, PCI_STP# active		1	RTC	1
t <sub>14</sub>	SUS[C:A]# inactive to CPU_STP#, PCI_STP# inactive	16		ms	3
t <sub>15</sub>	CPU_STP#, PCI_STP# inactive to clocks running		2	PCICLK	
t <sub>16</sub>	CPU_STP#, PCI_STP# inactive to SUS_STAT[2:1]# inactive	1		ms	
t <sub>17</sub>	SUS_STAT[2:1]# inactive to PCIRST# inactive		1	RTC	1
t <sub>18</sub>	PCIRST# inactive to CPURST# inactive	1		ms	

**NOTES:**

1. One RTC unit is approximately 32  $\mu$ s
2. This parameter only applies if BXPWROK will not transition to an active state within 15 ms of SUS[C:A]# de-assertion
3. This transition requires both a minimum of 16 ms wait for the clock synthesizer PLL lock and PIIX4 PWROK to be active. If PWROK goes active after 16 ms from SUS[C:A]# inactive, the transition will occur a minimum of one RTC period from PWROK active.

### 7.2.2.3 Suspend Resume Protocols

The suspend resume sequences are indicated to the 82443BX by the PIIX4E, using SUS\_STAT# and PCIRST#. In addition, the 82443BX contains NREF\_EN and CRst\_En configuration bits that participate in the suspend resume sequences.

As a result of suspend resume, the 82443BX performs the following activities:

- Changing its refresh mode
- Performing internal and processor reset
- Isolate or re-enable normal IO buffers

Table 47 describes the suspend resume events and activities.

Table 47. Suspend Resume Events And Activities

SUSSTAT#	PCIRST#	CrstEn	Reset	Refresh	I/O Buffers
Assert	Inactive	-	-	Switch to suspend refresh	Isolate
Deassert	Active	-	Reset exclude resume/ref logic	Suspend refresh NREF_EN remains inactive	Enable
Deassert	Inactive	0	No resets	Auto switch to normal ref NREF_EN is set	Enable
Deassert	Inactive	1	Reset processor only	Auto switch to normal ref NREF_EN is set	Enable

The requirements for suspending the 82443BX are:

- The system must be idle when SUS\_STAT# is asserted. There must be no active processor or bus masters' cycles and there must be no meaningful pending cycle's information in a chipset or peripheral device's buffers.
- After the assertion of SUS\_STAT#, the PIIX4E provides the 82443BX 32  $\mu$ s with stable power and clocks to perform the necessary suspend sequence.
- The PCICLK must not be stopped with CLKRUN# during the suspend sequence.
- The 82443BX isolates its IO buffers within less than 32  $\mu$ s time allocated from SUS\_STAT# assertion.
  - The 82443BX does not isolate PCIRST# (being pulled up) or clock inputs. The clock inputs are driven low by the clock synthesizer, and 32  $\mu$ s later the clock synthesizer device may be powered down.

The requirements for resuming the 82443BX are:

- Power and clocks must be stable for at least 1 ms before SUS\_STAT# is deasserted.
- When resuming from POS, STPCLK# remains active for about 100  $\mu$ s after SUS\_STAT# deassertion, to allow an automatic switch to normal DRAM operation before processor pending cycles take place.

The 82443BX provides isolation of its I/O buffers during POS and STR. During the events that were specified in Table 47, the isolation takes effect. Table 48 provides information about the state of each of the 82443BX signals during POS and STR.

Table 48. 443BX Signal States During POS and STR Modes (Sheet 1 of 3)

Signal Name	State During POS/STR
CPURST#	Tri-state
A[31:3]#	Tri-state
HD[63:0]#	Tri-state
ADS#	Tri-state
BNR#	Tri-state
BPRI#	Tri-state
DBSY#	Tri-state
DEFER#	Tri-state
DRDY#	Tri-state
HIT#	Tri-state
HITM#	Tri-state
HLOCK#	
HREQ[4:0]#	Tri-state
HTRDY#	Tri-state
RS[2:0]#	Tri-state
RASA[5:0]# / CSA[5:0]#	High1
RASB[5:0]# / CSB[5:0]#	High1
CKE[3:2] / CSA[7:6]#	Low/High2
CKE[5:4] / CSB[7:6]#	Low/High2
CASA[7:0]# / DQMA[7:0]#	High1
CASB[5,1]# / DQMB[5,1]#	High1
GCKE / CKE1	Low/High2
SRAS[B:A]#	Low/High2
CKE0 / FENA	Low/High2
SCAS[B:A]#	High/Low2
MAA[13:0]	Driven3
MAB[9:7]# / MAB[13,10]	Driven3
MAB[12:11]#	Driven3
MAB[6:0]#	Driven3
WEA#, WEB#	High
MD [63:0]	Driven3
MECC[7:0]	Driven3

**NOTES:**

1. SDRAM Mode: After putting the SDRAMs into self-refresh mode, these signals are driven high. EDO Mode: For self-refresh mode, RAS and CAS are driven low. Otherwise, the 82443BX continues to refresh during the POS/STR state.
2. SDRAM Mode: SRAS#, SCAS#, CKE[5:0] and GCKE are driven to the first value listed. EDO Mode: These signals are driven to the second value listed.
3. MA lines are always driven by the 82443BX, except for MAB[13:11,9:0]# and MAB10, which are three-stated during reset. MD/MECC are always driven by the 82443BX when there is no active cycle. The values driven on MA, MD and MECC are indeterminate during and after reset.



Table 48. 443BX Signal States During POS and STR Modes (Sheet 2 of 3)

Signal Name	State During POS/STR
AD[31:0]	Low
DEVSEL#	Tri-state
FRAME#	Tri-state
IRDY#	Tri-state
C/BE[3:0]#	Low
PAR	Low
PLOCK#	Tri-state
TRDY#	Tri-state
SERR#	Tri-state
STOP#	Tri-state
PHOLD#	Tri-state
PHLDA#	Tri-state
WSC#	Tri-state
PREQ[4:0]#	Tri-state
PGNT[4:0]#	Tri-state
PIPE#	Tri-state
SBA[7:0]	Tri-state
RBF#	Tri-state
ST[2:0]	Low
AD_STBA	Tri-state
AD_STBB	Tri-state
SB_STB	Tri-state
G_FRAME#	Tri-state
G_IRDY#	Tri-state
G_TRDY#	Tri-state
G_STOP#	Tri-state
G_DEVSEL#	Tri-state
G_REQ#	Tri-state
G_GNT#	Tri-state
G_AD[31:0]	Low
G_C/BE[3:0]#	Low
G_PAR	Low
HCLKIN	

**NOTES:**

1. SDRAM Mode: After putting the SDRAMs into self-refresh mode, these signals are driven high. EDO Mode: For self-refresh mode, RAS and CAS are driven low. Otherwise, the 82443BX continues to refresh during the POS/STR state.
2. SDRAM Mode: SRAS#, SCAS#, CKE[5:0] and GCKE are driven to the first value listed. EDO Mode: These signals are driven to the second value listed.
3. MA lines are always driven by the 82443BX, except for MAB[13:11,9:0]# and MAB10, which are three-stated during reset. MD/MECC are always driven by the 82443BX when there is no active cycle. The values driven on MA, MD and MECC are indeterminate during and after reset.

Table 48. 443BX Signal States During POS and STR Modes (Sheet 3 of 3)

Signal Name	State During POS/STR
PCLKIN	
DCLKO	Low
DCLKRD	
DCLKWR	
CRESET#	Tri-state
PCIRST#	
GCLKIN	
GCLKO	Low
TESTIN#	
SMBCLK	Tri-state
SMBDATA	Tri-state
CLKRUN#	Tri-state
SUSTAT#	

**NOTES:**

1. SDRAM Mode: After putting the SDRAMs into self-refresh mode, these signals are driven high. EDO Mode: For self-refresh mode, RAS and CAS are driven low. Otherwise, the 82443BX continues to refresh during the POS/STR state.
2. SDRAM Mode: SRAS#, SCAS#, CKE[5:0] and GCKE are driven to the first value listed. EDO Mode: These signals are driven to the second value listed.
3. MA lines are always driven by the 82443BX, except for MAB[13:11,9:0]# and MAB10, which are three-stated during reset. MD/MECC are always driven by the 82443BX when there is no active cycle. The values driven on MA, MD and MECC are indeterminate during and after reset.

### 7.2.2.4 82443BX Suspend/Resume Sequences and Timing

Table 49. Suspend/Resume Timing (Sheet 1 of 2)

Sym	Parameter	Min	Max	Unit
t1	BX_VCC stable to BXPWROK asserted. †	1		ms
t2	BXPWROK asserted to SUS_STAT# inactive	1		ms
t3	Clocks running to SUS_STAT# inactive, guarantee	1		ms
t4	BX_VCC active and BXPWROK inactive to CPURST# active		10	ns
t5	SUS_STAT# deasserted to PCIRST# deasserted, guarantee		32	μs
t6	PCIRST# deasserted to CPURST# deasserted	1		ms
t7	SUS_STAT# deasserted to buffers valid	2		HCLK
t8	SUS_STAT# asserted to clocks stopped, guarantee	32		μs
t9	SUS_STAT# asserted to suspend refresh		32	μs

† "BX\_VCC stable" means BX\_VCC is within the specified Functional Operating Range.

Table 49. Suspend/Resume Timing (Sheet 2 of 2)

Sym	Parameter	Min	Max	Unit
t10	SUS_STAT# asserted to buffers isolated		32	μs
t11	PCIRST# asserted to CPURST# asserted		10	ns
t12	PCIRST# asserted to SUS_STAT# de-asserted, guarantee	1		ms
t13	SUS_STAT# de-asserted to normal refresh		32	μs
t14	SUS_STAT# de-asserted to CPURST# asserted	0	4	HCLK
t15	CPURST# pulse width	1		ms

† "BX\_VCC stable" means BX\_VCC is within the specified Functional Operating Range.

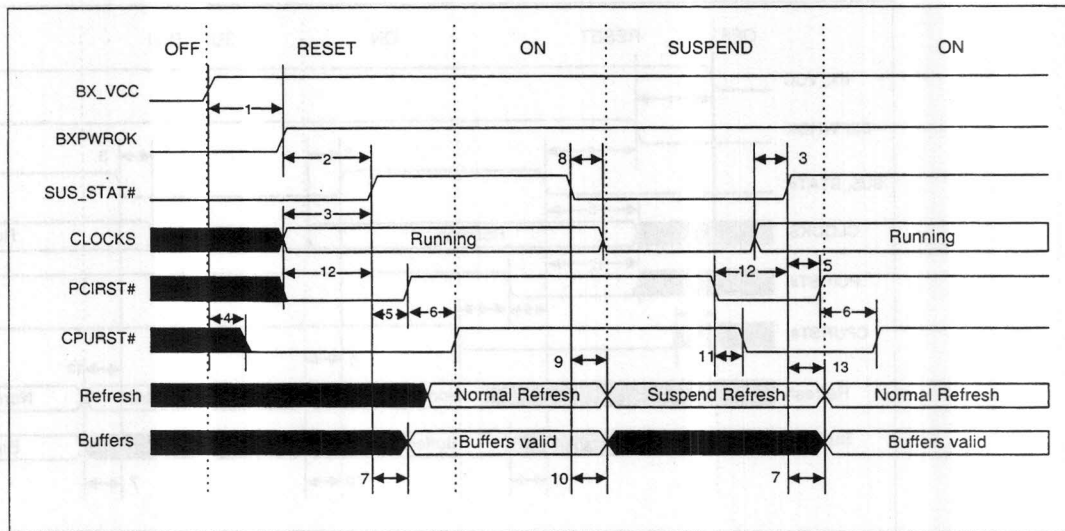
### 7.2.2.5 Suspend/Resume with PCIRST# Active

The following resume sequence is typically used when resuming from STR. It includes the following components:

- BXPWROK must transition from inactive (low) to active (high) a minimum of 1 ms after BX\_VCC is within the specified Functional Operating Range.
- When 15 ms or more may elapse from the time that the PIIX4E deasserts SUS[C:A]# until BXPWROK is asserted, BXPWROK must be asserted before or simultaneous to PWROK being asserted to the PIIX4E.
- Upon resume, the 82443BX detects that the PCIRST# signal is active (low) and drives CPURST# to the processor. Note that CPURST# is driven active based on PCIRST# timing, independent of SUS\_STAT# timing.
- Based on the assertion of SUS\_STAT#, the 82443BX isolates its I/O buffer within 32 μs.
- Based on the deassertion of SUS\_STAT#, the 82443BX enables its I/O buffer to normal operation within 32 μs. Clock inputs and PCIRST# are never gated by the 82443BX and thus affect it before the deassertion of SUS\_STAT#.
- Software must release the memory controller from its suspend refresh state to its normal refresh state.
- The 82443BX clears its internal state, with the exception of resume/refresh logic, since it sampled PCIRST# asserted.



Figure 37. Suspend/Resume with PCIRST# Active

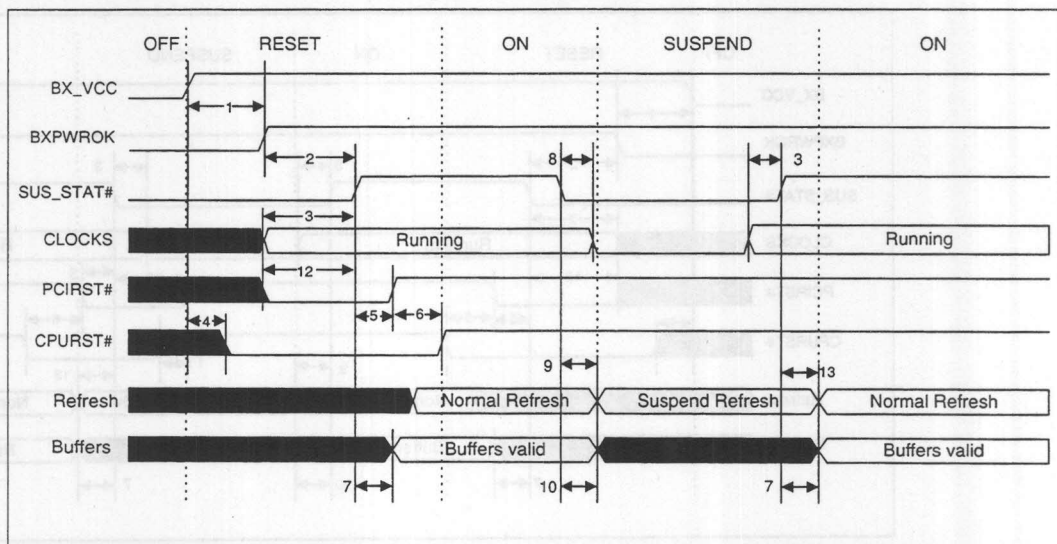


### 7.2.2.6 Suspend/Resume with inactive PCIRST#, CPURST#

The following resume sequence is typically used when resuming from POS. It includes the following components:

- Since PCIRST# signal is inactive, per resume the 82443BX does not drive CPURST# to the processor, since CrstEn is '0'.
- Based on the assertion of SUS\_STAT#, the 82443BX isolates its I/O buffer within 32  $\mu$ s.
- Based on the deassertion of SUS\_STAT#, the 82443BX enables its I/O buffer to normal operation within 32  $\mu$ s.
- The 82443BX switches from suspend refresh to normal DRAM operation mode.
- The processor starts execution from the instruction just prior to the stop grant request being recognized. The 82443BX switches to normal DRAM operation before the deassertion of STPCLK#.
- The 82443BX state is not reset.

Figure 38. Suspend/Resume with CPURST, PCIRST# Inactive

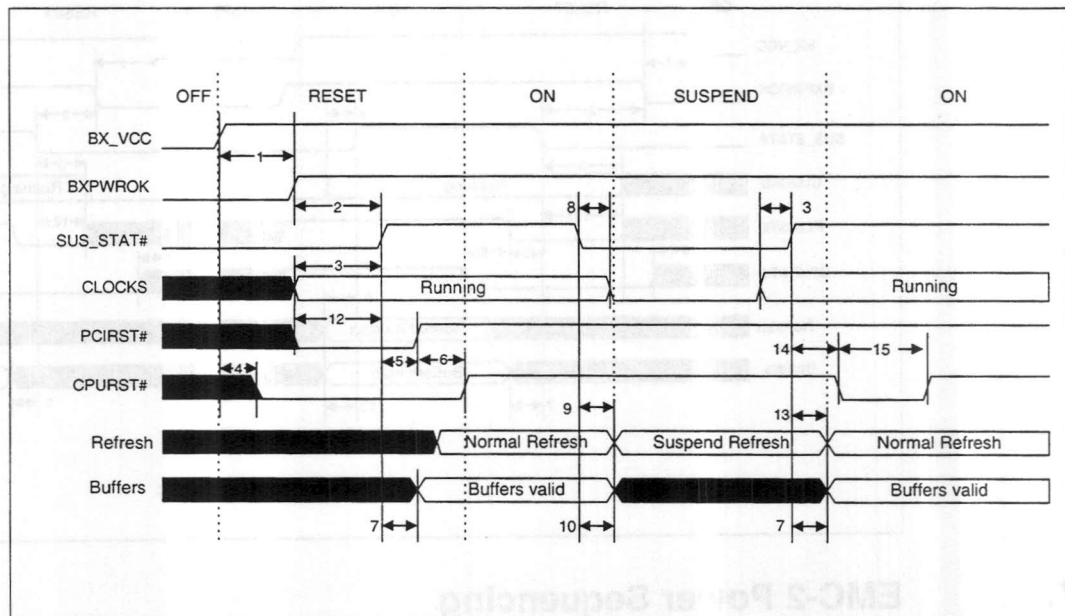


### 7.2.2.7 Suspend/Resume with CPURST Active, PCIRST# Inactive

The following resume sequence is typically used when resuming from POS. It includes the following components:

- The PCIRST# signal is inactive, upon resume the 82443BX drives CPURST# to the processor since CrstEn is '1'. CPURST# is active for 1 ms.
- Based on the assertion of SUS\_STAT#, the 82443BX isolates its I/O buffer within 32  $\mu$ s.
- Based on the deassertion of SUS\_STAT#, the 82443BX enables its I/O buffer to normal operation within 32  $\mu$ s.
- The 82443BX automatically switches from suspend refresh to normal DRAM operation mode when SUS\_STAT# deassertion is detected.
- The 82443BX state is not reset.

Figure 39. Suspend/Resume with Inactive PCIRST and Active CPURST#



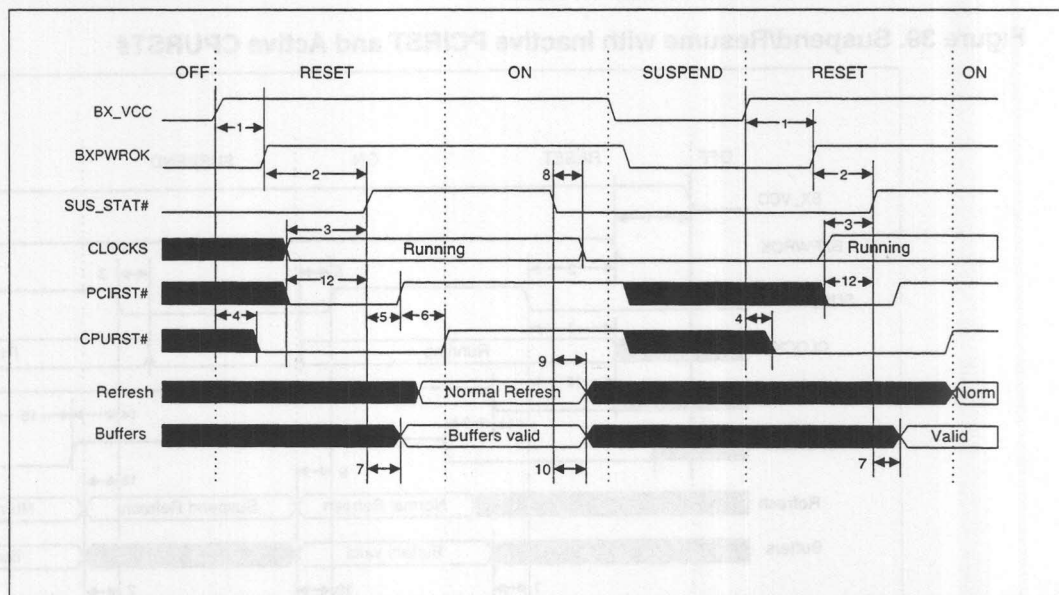


### 7.2.2.8 Suspend/Resume from STD

The following resume sequence is typically used when resuming from STD. It includes the following components:

- When BXPWROK is sampled low '0', the 82443BX undergoes a complete reset and asserts CPURST#.
- Based on the deassertion of SUS\_STAT#, the 82443BX enables its buffer to normal operation within less than 32  $\mu$ s. Clock inputs and PCIRST# are never gated by the 82443BX and thus affect it before the deassertion of SUS\_STAT#.
- Software must release the memory controller from its suspend refresh state to its normal refresh state, and enable refresh with the appropriate refresh rate.

Figure 40. Suspend/Resume from STD



## 7.3 EMC-2 Power Sequencing

### 7.3.1 Voltage Regulator Control

The EMC-2 VR\_ON pin on the EMC-2 module connector allows a digital signal (3.3 V, 5 V safe) to control the voltage regulator. The system manufacturer can use this signal to turn the Pentium II processor module voltage regulator on or off. VR\_ON should be controlled as a function of the same digital control signal (SUSB#) used to control the system's switched 5-V /3.3-V power planes. The PIIX4E defines Suspend to RAM (STR) as the power-management state in which power is physically removed from most of the system components except DRAM. In this state, the SUSB# pin on the PIIX4E controls these power planes.

**Caution:** VR\_ON should switch high only when the following conditions are met: V\_5(s) ≥ 4.5-V, and V\_DC ≥ 4.75-V. Turning on VR\_ON prior to meeting these conditions will severely damage the module.

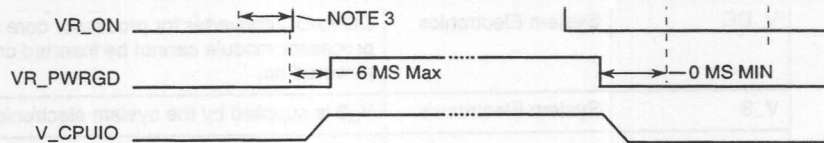
## 7.3.2 Voltage Signal Definition and Sequencing

**Table 50. Voltage Signal Definitions and Sequences**

Signal	Source	Definitions and Sequences
V_DC	System Electronics	DC voltage driven from the power supply and is required to be between 5-V and 21-V DC. V_DC powers the processor module's DC-to-DC converter for processor core and I/O voltages. The processor module cannot be inserted or removed while V_DC is powered on.
V_3	System Electronics	V_3 is supplied by the system electronics for the 82443BX.
V_5	System Electronics	V_5 is supplied by the system electronics for the 82443BX's 5-V reference voltage and processor module's voltage regulator.
V_3S	System Electronics	V_3S is supplied by the system electronics for the L2 cache devices. Each must be powered off during system STR and STD states.
VR_ON	System Electronics	VR_ON enables the processor module's voltage regulator circuit. When driven active high (3.3-V) the voltage regulator circuit on the processor module is activated. The signal driving VR_ON should be a digital signal with a rise/fall time of less than or equal to 1 μs.
V_CORE (also used as host bus GTL+ termination voltage VTT)	Processor module only; not on module interface.	A result of VR_ON being asserted, V_CORE is an output of the DC-DC regulator on the processor module and is driven to the core voltage of the processor. It is also used as the host bus GTL+ termination voltage (VTT).
V_BSB_IO	Processor module only; not on module interface.	V_BSB_IO is 1.8-V. The system electronics uses this voltage to power the L2 cache-to-processor interface circuitry.
VR_PWRGD	Processor module	Upon sampling the voltage level of V_CORE for the processors, minus tolerances for ripple, VR_PWRGD is driven active high (3.3 V) for the system electronics to sample prior to providing PWROK to the PIIX4. If VR_PWRGD is not sampled active within 1 second of the assertion of VR_ON the system electronics should de-assert VR_ON.
V_CPUPU	Processor module	V_CPUPU is 2.5-V. The system electronics uses this voltage to power the PIIX4E-to-processor interface circuitry
V_CLK	Processor module	V_CLK is 2.5-V. The system electronics uses this voltage to power the HCLK_(0:1) drivers for the processor clock.

Figure 41 details the sequencing of signals and voltage planes required for normal operation of the processor module.

The processor module provides the VR\_PWRGD signal, which indicates that the voltage regulator power is operating at a stable voltage level. The system manufacturer should use this signal on the system electronics to control power inputs and to gate PWROK to the PIIX4E.



#### Power Sequence Timing

1. PWROK on I/O board should be active on when VR\_PWRGD is active and V\_3S is good.
2. CPU\_RST from I/O board should be active for a minimum of 6 ms after PWROK is active and PLL\_STP# and CPU\_STP# are inactive. Note that PLL\_STP# is an AND condition of RSMRST# and SUSB# on the PIIX4.
3.  $V_{DC} \geq 4.7V$ ,  $V_5 \geq 4.5V$ ,  $V_3S \geq 3.0V$ .
4. V\_CPUIO is generated on the Intel® Pentium® II Processor Mobile Module.
5. This is the 5V power supplied to the processor module connector. This should be the first 5V plane to power up.

A6072-01



**Low Power Embedded Pentium®  
Processor with MMX™ Technology  
Datasheet**







# Low-Power Embedded Pentium® Processor with MMX™ Technology

## Advance Information Datasheet

### Product Features

- Support for MMX™ Technology
- Low-Power 0.25 Micron Process Technology
  - 1.9 V (166/266 MHz) Core Supply for PPGA
  - 1.8 V (166 MHz) or 2.0 V (266 MHz) Core Supply for HL-PBGA
  - 2.5 V I/O Interface (166/266 MHz)
- 32-Bit CPU with 64-Bit Data Bus
- Fractional Bus Operation
  - 166-MHz Core/66-MHz Bus
  - 266-MHz Core/66-MHz Bus
- Superscalar Architecture
  - Enhanced Pipelines
  - Two Pipelined Integer Units Capable of Two Instructions/Clock
  - Pipelined MMX Technology
  - Pipelined Floating-Point Unit
- Separate Code and Data Caches
  - 16-Kbyte Code, 16-Kbyte Write-Back Data
  - MESI Cache Protocol
- Compatible with Large Software Base
  - MS-DOS\*, Windows\*, OS/2\*, UNIX\*
- 4-Mbyte Pages for Increased TLB Hit Rate
- IEEE 1149.1 Boundary Scan
- Advanced Design Features
  - Deeper Write Buffers
  - Enhanced Branch Prediction Feature
  - Virtual Mode Extensions
- Internal Error Detection Features
- On-Chip Local APIC Controller
- Power Management Features
  - System Management Mode
  - Clock Control
- 296-pin PPGA or 352-ball HL-PBGA

**Notice:** This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Order Number: 273184-001  
October, 1998

# Low-Power Embedded Pentium® Processor with MMX™ Technology

## Advance Information Datasheet

## Product Features

- Support for MMX™ Technology
- Low-Power 0.5 Micron Process Technology
- 1.5 V (1600 mV) Core Supply for FPDs
- 1.5 V (1600 mV) or 2.0 V (200 mV) Core Supply for L2-PBGA
- 2.2 V I/O Buffers (1600 mV)
- 32-Bit CPU with 64-Bit Data Bus
- Fractional Bus Operation
- 160-MHz Core-to-Mem Bus
- 160-MHz Core-to-Mem Bus
- Symmetrical Architecture
- Enhanced Floating Point
- Two Pipelined Integer Units Capable of Two Instructions/Clock
- Pipelined MMX Technology
- Pipelined Floating-Point Unit
- 200-pin FPD or 320-pin L2-PBGA
- Clock Control
- System Management Mode
- Power Management Features
- On-Chip Local APIC Controller
- Internal Error Detection Features
- Virtual Mode Extensions
- Enhanced Branch Prediction Feature
- Deep-Write Buffer
- Advanced Design Features
- IEEE 1149.1 Boundary Scan
- 4-Mbyte Page for Increased TLB Hit Rate
- MS-DOS™, Windows™, OS/2™, UNIX™
- Compatible with Large Software Base
- MESI Cache Protocol
- Write-Back Data
- 16-Kbyte Code, 16-Kbyte
- System Code and Data Caches

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## 1.0 Overview

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The Low-Power Embedded Pentium® Processor with MMX™ Technology extends the Pentium processor family, providing additional performance and low power for embedded applications. The low-power embedded Pentium processor with MMX technology is compatible with the entire installed base of applications for MS-DOS\*, Windows\*, OS/2\*, and UNIX\* and is one of the major microprocessors to support Intel MMX technology. Furthermore, the low-power embedded Pentium processor with MMX technology has superscalar architecture which can execute two instructions per clock cycle, and enhanced branch prediction and separate caches also increase performance. The pipelined floating-point unit delivers workstation level performance. Separate code and data caches reduce cache conflicts while remaining software transparent.

The low-power embedded Pentium processor with MMX technology has 4.5 million transistors, is built on Intel's 0.25 micron manufacturing process technology and has full SL Enhanced power management features including System Management Mode (SMM) and clock control. The low-power embedded Pentium processor with MMX technology is available in a 296-pin Plastic Pin Grid Array (PPGA) or 352-ball High-Thermal Low-Profile-Plastic Ball Grid Array (HL-PBGA). The HL-PBGA package allows designers to use surface mount technology to create small form-factor designs.

The additional SL Enhanced features, low-power dissipation and PPGA or HL-PBGA package make the low-power embedded Pentium processor with MMX technology ideal for embedded designs.

## 2.0 Introduction

---

The low-power embedded Pentium processors with MMX technology for high performance embedded applications (166 and 266 MHz) are fully compatible with the existing Pentium processors with MMX technology (200 and 233 MHz) with the following differences: voltage supplies, power consumption, and performance. Additionally, Pentium processors with MMX technology are socket compatible with the Pentium processor (100, 133, and 166 MHz), making it possible to design a flexible motherboard that supports both the Pentium processor and the embedded Pentium processors with MMX technology (166–266 MHz).

The low-power embedded Pentium processor with MMX technology has all the advanced architectural and internal features of the desktop version of the Pentium processor with MMX technology, except that several features have been eliminated. The differences are specified in "Differences from Desktop Processors" on page 14.

The low-power embedded Pentium processor with MMX technology has several features which allow for high-performance embedded designs. These features include the following:

- 1.9 V core (PPGA – 166/266 MHz)
- 1.8 V core (HL-PBGA – 166), 2.0 V core (HL-PBGA – 266)
- 2.5 V I/O buffer  $V_{CC3}$  inputs to reduce power consumption
- SL Enhanced feature set

This document should be used in conjunction with *Embedded Pentium® Processor Family Developer's Manual* (order number 273204).



### 3.0 Microprocessor Architecture Overview

---

The low-power embedded Pentium processor with MMX technology extends the family of Pentium processors with MMX technology. It is binary compatible with the 8086/88, 80286, Intel386™ DX, Intel386 SX, Intel486™ SX, IntelDX2™, IntelDX4™, and Pentium processors with voltage reduction technology (75–150 MHz).

The embedded Pentium processor family consists of the embedded Pentium processor (100, 133, and 166 MHz), the embedded Pentium processor with voltage reduction technology (133 MHz), the embedded Pentium processor with MMX technology (200, 233 MHz), and the low-power embedded Pentium processor with MMX technology (166, 266 MHz).

The low-power embedded Pentium processor with MMX technology contains all of the features of previous Intel architecture processors and provides significant enhancements and additions, including the following:

- Support for MMX™ Technology
- Superscalar Architecture
- Enhanced Branch Prediction Algorithm
- Pipelined Floating-Point Unit
- Improved Instruction Execution Time
- Separate 16-Kbyte Code Cache and 16-Kbyte Data Cache
- Writeback MESI Protocol in the Data Cache
- 64-Bit Data Bus
- Enhanced Bus Cycle Pipelining
- Address Parity
- Internal Parity Checking
- Execution Tracing
- Performance Monitoring
- IEEE 1149.1 Boundary Scan
- System Management Mode
- Virtual Mode Extensions
- 0.25 Micron Process Technology
- SL Power Management Features
- Pool of Four Write Buffers Used by Both Pipes

### 3.1 Pentium® Processor Family Architecture

The application instruction set of the Pentium processor family includes the complete Intel486 CPU family instruction set with extensions to accommodate some of the additional functionality of the Pentium processors. All application software written for the Intel386 and Intel486 family microprocessors will run on the Pentium processors without modification. The on-chip memory management unit (MMU) is completely compatible with the Intel386 and Intel486 families of processors.

The Pentium processors implement several enhancements to increase performance. The two instruction pipelines and the floating-point unit on Pentium processors are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating-point instruction (under certain circumstances, two floating-point instructions) in one clock.

Branch prediction is implemented in the Pentium processors. To support this, Pentium processors implement two prefetch buffers, one that prefetches code in a linear fashion, and one that prefetches code according to the Branch Target Buffer (BTB) so that code is almost always prefetched before it is needed for execution.

The floating-point unit has been completely redesigned over the Intel486 processor. Faster algorithms provide up to 10x speed-up for common operations including add, multiply, and load.

Pentium processors include separate code and data caches integrated on-chip to meet performance goals. Each cache has a 32-byte line size and is 4-way set associative. Each cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to physical addresses. The data cache is configurable to be writeback or writethrough on a line-by-line basis and follows the MESI protocol. The data cache tags are triple ported to support two data transfers and an inquire cycle in the same clock. The code cache is an inherently write-protected cache. The code cache tags are also triple ported to support snooping and split line accesses. Individual pages can be configured as cacheable or non-cacheable by software or hardware. The caches can be enabled or disabled by software or hardware.

The Pentium processors have increased the data bus to 64 bits to improve the data transfer rate. Burst read and burst writeback cycles are supported by the Pentium processors. In addition, bus cycle pipelining has been added to allow two bus cycles to be in progress simultaneously. The Pentium processors' MMU contains optional extensions to the architecture that allow 4-Kbyte and 4-Mbyte page sizes.

The Pentium processors have added significant data integrity and error detection capability. Data parity checking is still supported on a byte-by-byte basis. Address parity checking and internal parity checking features have been added along with a new exception, the machine check exception.

As more and more functions are integrated on-chip, the complexity of board level testing is increased. To address this, the Pentium processors have increased test and debug capability. The Pentium processors implement IEEE Boundary Scan (Standard 1149.1). In addition, the Pentium processors have specified four breakpoint pins that correspond to each of the debug registers and externally indicate a breakpoint match. Execution tracing provides external indications when an instruction has completed execution in either of the two internal pipelines, or when a branch has been taken.

System Management Mode (SMM) has been implemented along with some extensions to the SMM architecture. Enhancements to virtual 8086 mode have been made to increase performance by reducing the number of times it is necessary to trap to a virtual 8086 monitor.

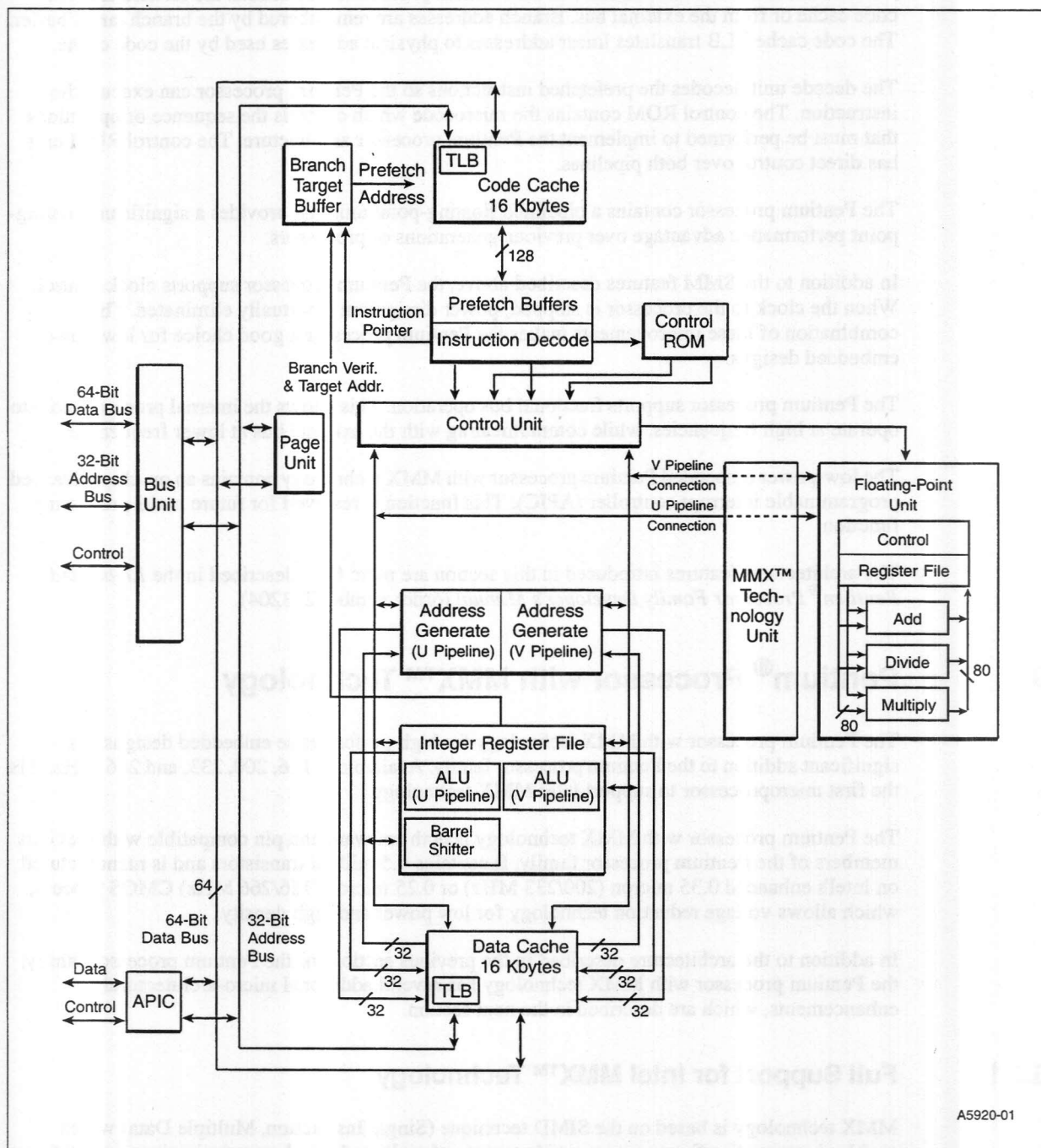
Figure 1 shows a block diagram of the Pentium processor with MMX technology.

The block diagram shows the two instruction pipelines, the “u” pipe and “v” pipe. The u-pipe can execute all integer and floating-point instructions. The v-pipe can execute simple integer instructions and the FXCH floating-point instructions.

The separate code and data caches are shown. The data cache has two ports, one for each of the two pipes (the tags are triple ported to allow simultaneous inquire cycles). The data cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses used by the data cache.



Figure 1. Pentium® Processor with MMX™ Technology Block Diagram



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The code cache, branch target buffer and prefetch buffers are responsible for getting raw instructions into the execution units of the Pentium processor. Instructions are fetched from the code cache or from the external bus. Branch addresses are remembered by the branch target buffer. The code cache TLB translates linear addresses to physical addresses used by the code cache.

The decode unit decodes the prefetched instructions so the Pentium processor can execute the instruction. The control ROM contains the microcode which controls the sequence of operations that must be performed to implement the Pentium processor architecture. The control ROM unit has direct control over both pipelines.

The Pentium processor contains a pipelined floating-point unit that provides a significant floating-point performance advantage over previous generations of processors.

In addition to the SMM features described above, the Pentium processor supports clock control. When the clock to the processor is stopped, power dissipation is virtually eliminated. The combination of these improvements makes the Pentium processor a good choice for low-power embedded designs.

The Pentium processor supports fractional bus operation. This allows the internal processor core to operate at high frequencies, while communicating with the external bus at lower frequencies.

The low-power embedded Pentium processor with MMX technology contains an on-chip advanced programmable interrupt controller (APIC). This function is reserved for future multi-processing function.

The architectural features introduced in this section are more fully described in the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204).

## 3.2 Pentium® Processor with MMX™ Technology

The Pentium processor with MMX technology for high-performance embedded designs is a significant addition to the Pentium processor family. Available at 166, 200, 233, and 266 MHz, it is the first microprocessor to support Intel MMX technology.

The Pentium processor with MMX technology is both software and pin compatible with previous members of the Pentium processor family. It contains 4.5 million transistors and is manufactured on Intel's enhanced 0.35 micron (200/233 MHz) or 0.25 micron (166/266 MHz) CMOS process, which allows voltage reduction technology for low power and high density.

In addition to the architecture described in the previous section for the Pentium processor family, the Pentium processor with MMX technology has several additional micro-architectural enhancements, which are described in the next section.

### 3.2.1 Full Support for Intel MMX™ Technology

MMX technology is based on the SIMD technique (Single Instruction, Multiple Data) which enables increased performance on a wide variety of multimedia and communications applications. Fifty-seven new instructions and four new 64-bit data types are supported in the Pentium processor with MMX technology. All existing operating system and application software are fully-compatible.



### **3.2.2 16-Kbyte Code and Data Caches**

On-chip level-1 data and code cache sizes are 16 Kbytes each and are 4-way set associative on the Pentium processor with MMX technology. Large separate internal caches improve performance by reducing average memory access time and providing fast access to recently-used instructions and data. The instruction and data caches can be accessed simultaneously while the data cache supports two data references simultaneously. The data cache supports a write-back (or alternatively, write-through, on a line-by-line basis) policy for memory updates.

### **3.2.3 Improved Branch Prediction**

Dynamic branch prediction uses the Branch Target Buffer (BTB) to boost performance by predicting the most likely set of instructions to be executed. The BTB has been improved on the Pentium processor with MMX technology to increase its accuracy. This processor has four prefetch buffers that can hold up to four successive code streams.

### **3.2.4 Enhanced Pipeline**

An additional pipeline stage has been added and the pipeline has been enhanced to improve performance. The integration of the MMX technology pipeline with the integer pipeline is very similar to that of the floating-point pipeline. Under some circumstances, two MMX instructions or one integer and one MMX instruction can be paired and issued in one clock cycle to increase throughput. The enhanced pipeline is described in more detail in the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204).

### **3.2.5 Deeper Write Buffers**

A pool of four write buffers is now shared between the dual pipelines to improve memory write performance.

## **3.3 0.25 Micron Technology**

The 0.25 micron technology is the state-of-the-art CMOS manufacturing process Intel unveiled on April 12, 1997, enabling the use of lower core supply to sub-2 V. As a result, the low-power embedded Pentium processor with MMX technology consumes significantly less power at even higher speeds.



## 4.0 Package Information

### 4.1 Differences from Desktop Processors

The following features have been eliminated in the low-power embedded Pentium processor with MMX technology: Upgrade, Dual Processing (DP), and Master/Checker functional redundancy.

Table 1 lists the corresponding pins that exist on the Pentium processor with MMX technology but have been removed on the low-power embedded Pentium processor with MMX technology.

**Table 1. Signals Removed from the Low-Power Embedded Pentium® Processor with MMX™ Technology**

Signal	Function
ADSC#	Additional Address Status. This signal is mainly used for large or standalone L2 cache memory subsystem support required for high-performance desktop or server models.
BRDYC#	Additional Burst Ready. This signal is mainly used for large or standalone L2 cache memory subsystem support required for high-performance desktop or server models.
CPUTYP	CPU Type. This signal is used for dual processing systems.
D/P#	Dual/Primary processor identification. This signal is only used for an upgrade processor.
FRCMC#	Functional Redundancy Checking. This signal is only used for error detection via processor redundancy and requires two Pentium processors (master/checker).
PBGNT#	Private Bus Grant. This signal is only used for dual processing systems.
PBREQ#	Private Bus Request. This signal is used only for dual processing systems.
PHIT#	Private Hit. This signal is only used for dual processing systems.
PHITM#	Private Modified Hit. This signal is only used for dual processing systems.

## 4.2 PPGA Pinout and Pin Descriptions

The text orientation on the top side view drawings in this section represents the orientation of the ink mark on the actual packages. (Note that the text shown in this section is not the actual text that will be marked on the packages).

Figure 2. PPGA Package Top Side View

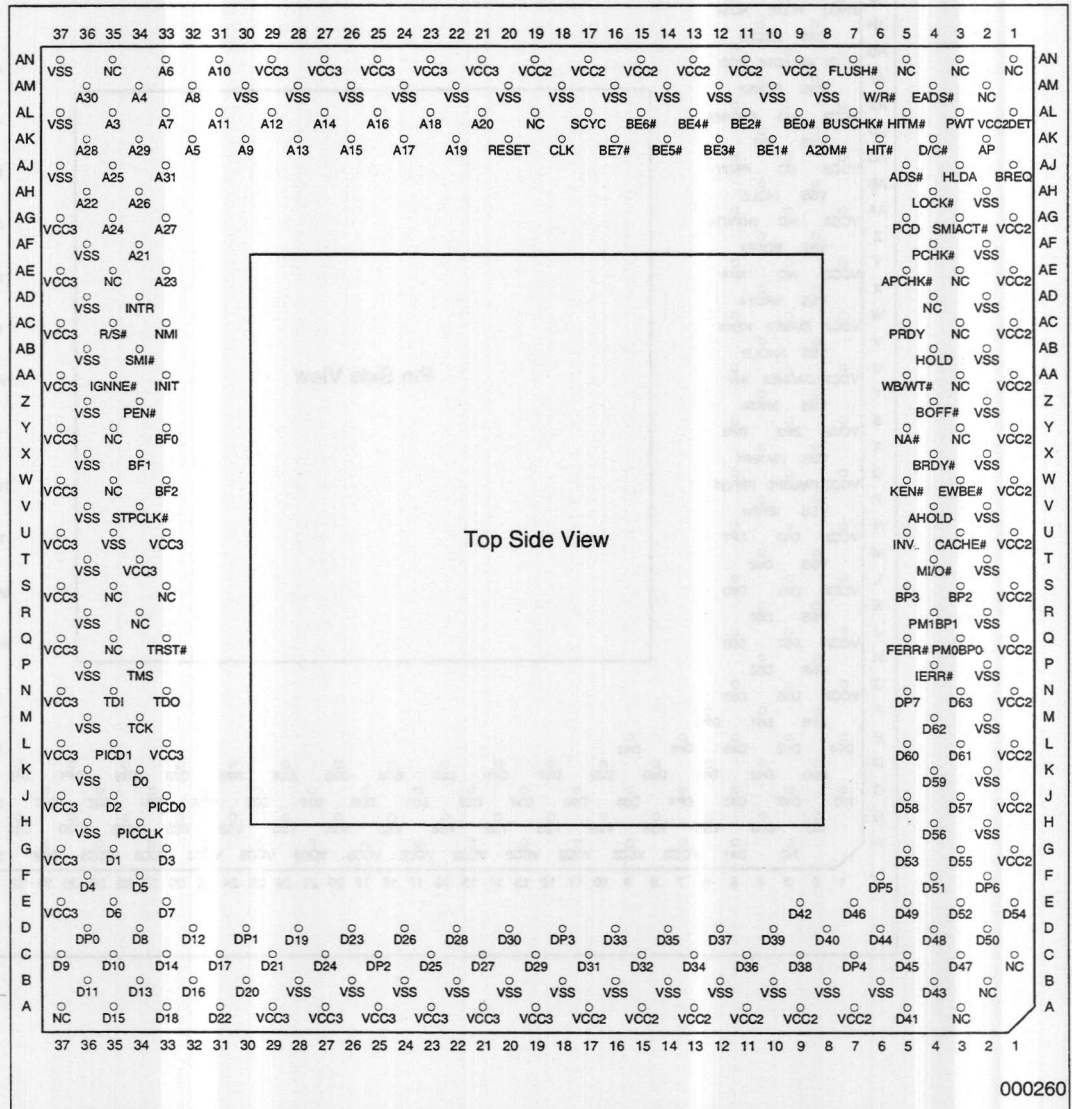


Figure 3. PPGA Package Pin Side View

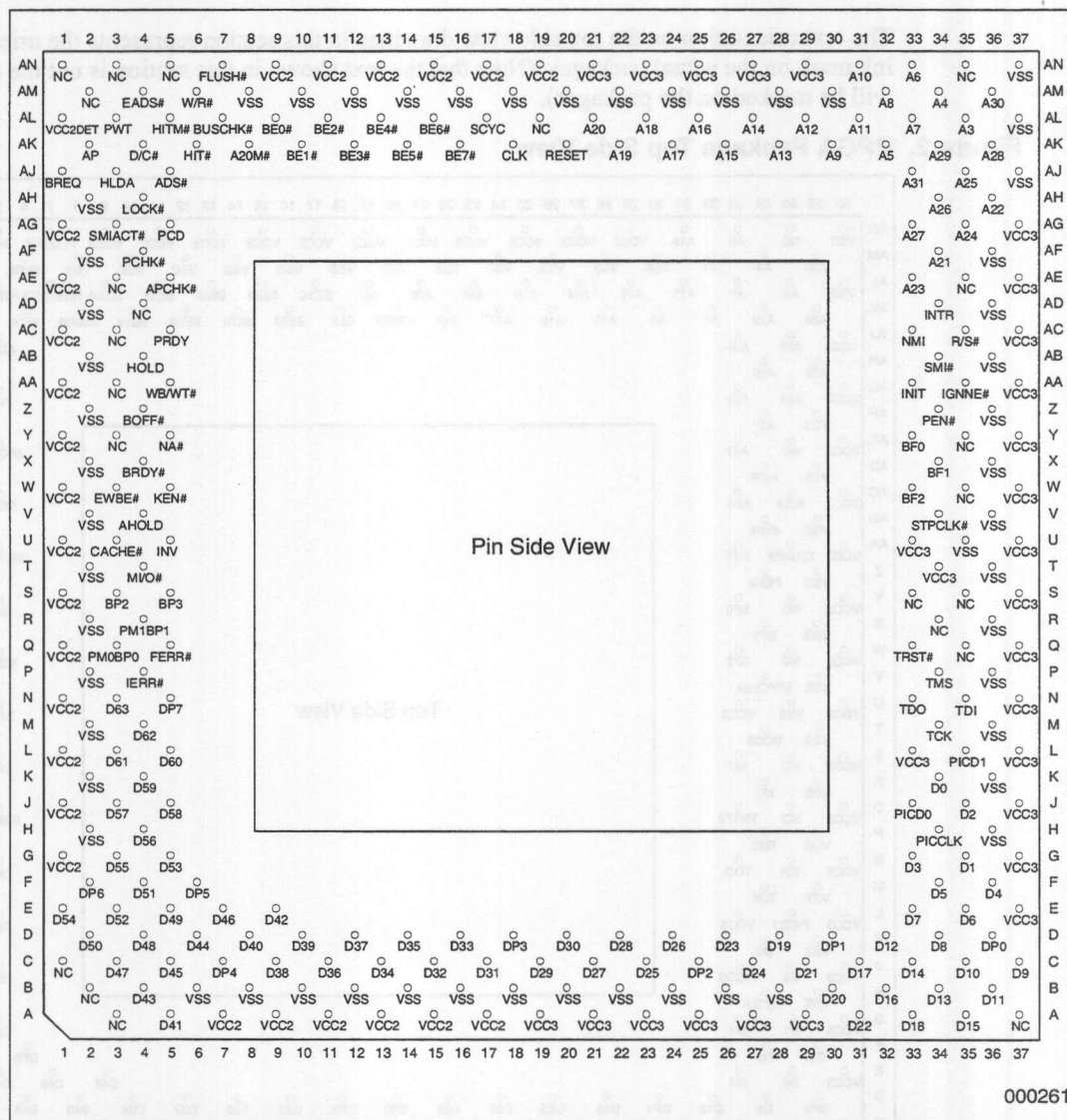






Table 2. Pin Cross Reference by Pin Name (PPGA Package) (Sheet 1 of 2)

Pin	Location	Pin	Location	Pin	Location	Pin	Location
Address							
A3	AL35	A11	AL31	A19	AK22	A27	AG33
A4	AM34	A12	AL29	A20	AL21	A28	AK36
A5	AK32	A13	AK28	A21	AF34	A29	AK34
A6	AN33	A14	AL27	A22	AH36	A30	AM36
A7	AL33	A15	AK26	A23	AE33	A31	AJ33
A8	AM32	A16	AL25	A24	AG35		
A9	AK30	A17	AK24	A25	AJ35		
A10	AN31	A18	AL23	A26	AH34		
Data							
D0	K34	D16	B32	D32	C15	D48	D04
D1	G35	D17	C31	D33	D16	D49	E05
D2	J35	D18	A33	D34	C13	D50	D02
D3	G33	D19	D28	D35	D14	D51	F04
D4	F36	D20	B30	D36	C11	D52	E03
D5	F34	D21	C29	D37	D12	D53	G05
D6	E35	D22	A31	D38	C09	D54	E01
D7	E33	D23	D26	D39	D10	D55	G03
D8	D34	D24	C27	D40	D08	D56	H04
D9	C37	D25	C23	D41	A05	D57	J03
D10	C35	D26	D24	D42	E09	D58	J05
D11	B36	D27	C21	D43	B04	D59	K04
D12	D32	D28	D22	D44	D06	D60	L05
D13	B34	D29	C19	D45	C05	D61	L03
D14	C33	D30	D20	D46	E07	D62	M04
D15	A35	D31	C17	D47	C03	D63	N03
Control							
A20M#	AK08	BREQ	AJ01	HITM#	AL05	PM1/BP1	R04
ADS#	AJ05	BUSCHK#	AL07	HLDA	AJ03	PRDY	AC05
AHOLD	V04	CACHE#	U03	HOLD	AB04	PWT	AL03
AP	AK02	D/C#	AK04	IERR#	P04	R/S#	AC35
APCHK#	AE05	DP0	D36	IGNNE#	AA35	RESET	AK20
BE0#	AL09	DP1	D30	INIT	AA33	SCYC	AL17
BE1#	AK10	DP2	C25	INTR/ LINT0	AD34	SMI#	AB34
BE2#	AL11	DP3	D18	INV	U05	SMIACT#	AG03
BE3#	AK12	DP4	C07	KEN#	W05	TCK	M34
BE4#	AL13	DP5	F06	LOCK#	AH04	TDI	N35
BE5#	AK14	DP6	F02	M/IO#	T04	TDO	N33
BE6#	AL15	DP7	N05	NA#	Y05	TMS	P34
BE7#	AK16	EADS#	AM04	NMI/LINT1	AC33	TRST#	Q33
BOFF#	Z04	EWBE#	W03	PCD	AG05	VCC2DET#	AL01
BP2	S03	FERR#	Q05	PCHK#	AF04	W/R#	AM06

Table 2. Pin Cross Reference by Pin Name (PPGA Package) (Sheet 2 of 2)

Pin	Location	Pin	Location	Pin	Location	Pin	Location
BP3	S05	FLUSH#	AN07	PEN#	Z34	WB/WT#	AA05
BRDY#	X04	HIT#	AK06	PM0/BP0	Q03		
APIC							
PICCLK	H34	PICD0	J33	PICD1 [APICEN]	L35		
Clock Control							
BF0	Y33	BF1	X34	BF2	W33	CLK	AK18
STPCLK#	V34						

Table 3. No Connect, Power Supply and Ground Pin Cross Reference (PPGA Package)

V <sub>CC2</sub>							
A07	A15	J01	Q01	W01	AC01	AN09	AN15
A09	A17	L01	S01	Y01	AE01	AN11	AN17
A11	G01	N01	U01	AA01	AG01	AN13	AN19
A13							
V <sub>CC3</sub>							
A19	A27	J37	Q37	U37	AA37	AG37	AN25
A21	A29	L37	S37	W37	AC37	AN29	AN23
A23	E37	L33	T34	Y37	AE37	AN27	AN21
A25	G37	N37	U33				
V <sub>SS</sub>							
B06	B20	K02	R36	X36	AF02	AM12	AM26
B08	B22	K36	T02	Z02	AF36	AM14	AM28
B10	B24	M02	T36	Z36	AH02	AM16	AM30
B12	B26	M36	U35	AB02	AJ37	AM18	AN37
B14	B28	P02	V02	AB36	AL37	AM20	
B16	H02	P36	V36	AD02	AM08	AM22	
B18	H36	R02	X02	AD36	AM10	AM24	
No Connect (NC)							
A03		S33		AC03		AN01	
A37		S35		AD04		AN03	
B02		W35		AE03		AN05	
C01		Y03		AE35		AN35	
Q35		Y35		AL19			
R34		AA03		AM02			

**NOTE:** Shaded pins differ functionally from the Pentium® Processor with MMX™ Technology pinout.

### 4.3 HL-PBGA Pinout and Pin Descriptions

**Figure 4. HL-PBGA Package Top Side View**

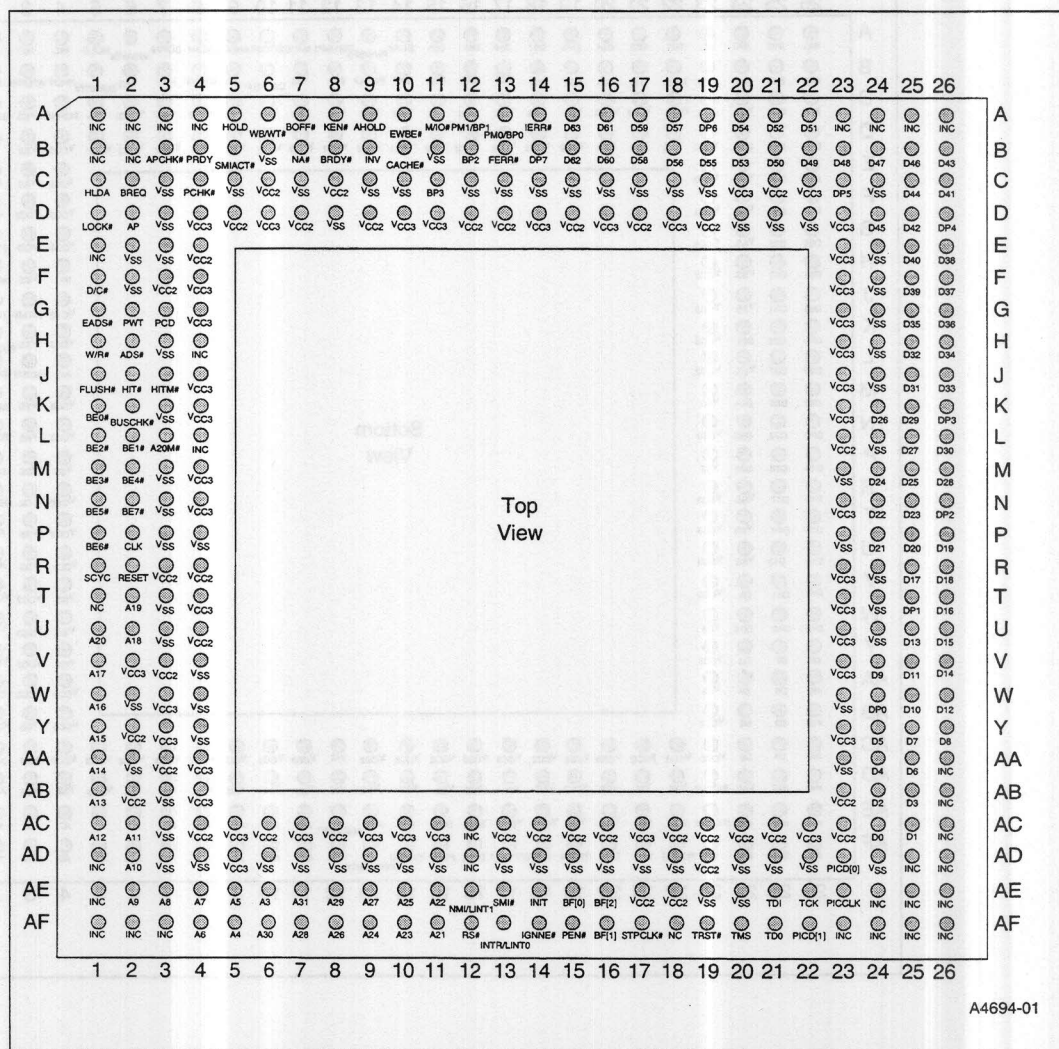




Figure 5. HL-PBGA Package Pin Side View

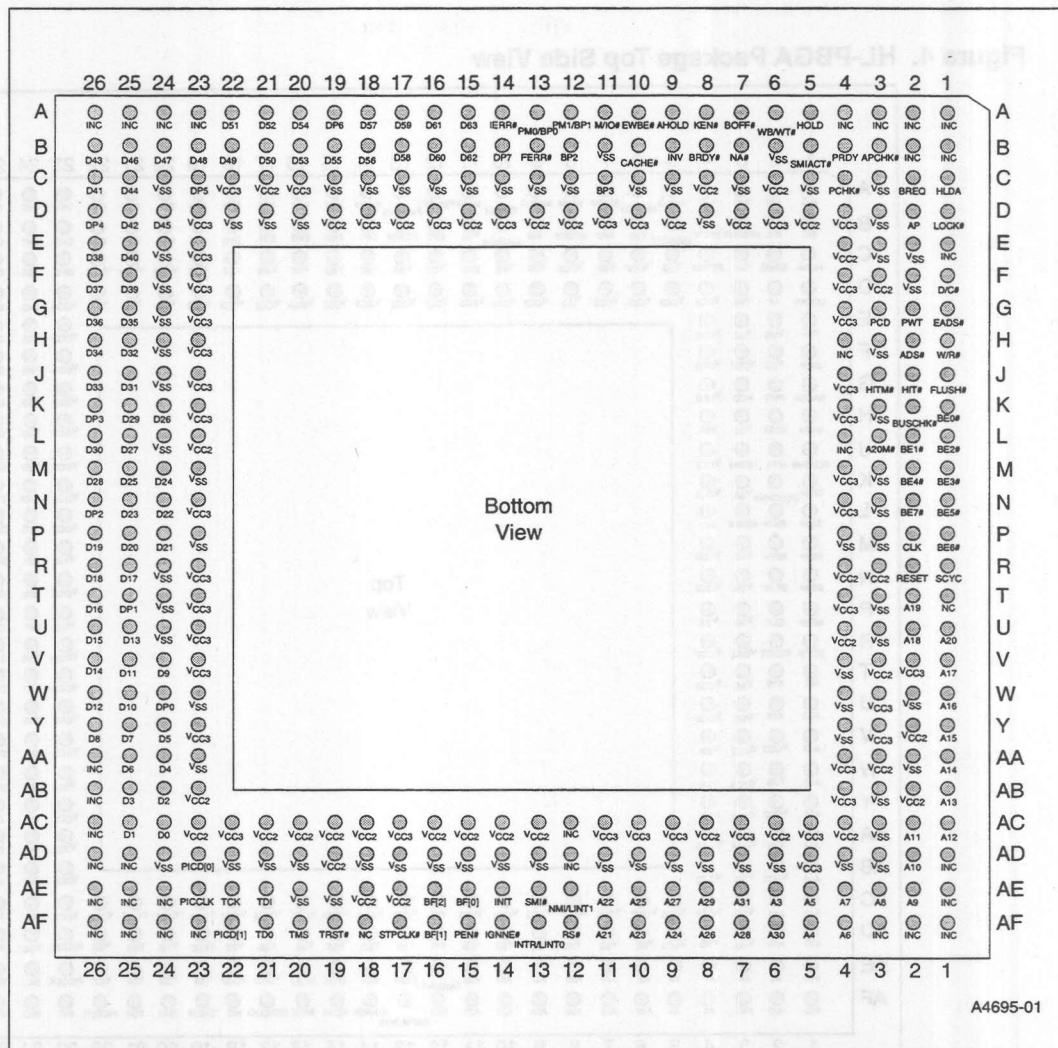


Table 4. Pin Cross Reference by Pin Name (HL-PBGA Package) (Sheet 1 of 2)

Pin	Location	Pin	Location	Pin	Location	Pin	Location
Address							
A3	AE6	A11	AC2	A19	T2	A27	AE9
A4	AF5	A12	AC1	A20	U1	A28	AF7
A5	AE5	A13	AB1	A21	AF11	A29	AE8
A6	AF4	A14	AA1	A22	AE11	A30	AF6
A7	AE4	A15	Y1	A23	AF10	A31	AE7
A8	AE3	A16	W1	A24	AF9		
A9	AE2	A17	V1	A25	AE10		
A10	AD2	A18	U2	A26	AF8		
Data							
D0	AC24	D16	T26	D32	H25	D48	B23
D1	AC25	D17	R25	D33	J26	D49	B22
D2	AB24	D18	R26	D34	H26	D50	B21
D3	AB25	D19	P26	D35	G25	D51	A22
D4	AA24	D20	P25	D36	G26	D52	A21
D5	Y24	D21	P24	D37	F26	D53	B20
D6	AA25	D22	N24	D38	E26	D54	A20
D7	Y25	D23	N25	D39	F25	D55	B19
D8	Y26	D24	M24	D40	E25	D56	B18
D9	V24	D25	M25	D41	C26	D57	A18
D10	W25	D26	K24	D42	D25	D58	B17
D11	V25	D27	L25	D43	B26	D59	A17
D12	W26	D28	M26	D44	C25	D60	B16
D13	U25	D29	K25	D45	D24	D61	A16
D14	V26	D30	L26	D46	B25	D62	B15
D15	U26	D31	J25	D47	B24	D63	A15
Control							
A20M#	L3	BREQ	C2	HITM#	J3	PM1/BP1	A12
ADS#	H2	BUSCHK#	K2	HLDA	C1	PRDY	B4
AHOLD	A9	CACHE#	B10	HOLD	A5	PWT	G2
AP	D2	D/C#	F1	IERR#	A14	R/S#	AF12
APCHK#	B3	DP0	W24	IGNNE#	AF14	RESET	R2
BE0#	K1	DP1	T25	INIT	AE14	SCYC	R1
BE1#	L2	DP2	N26	INTR/ LINT0	AF13	SMI#	AE13
BE2#	L1	DP3	K26	INV	B9	SMIACK#	B5
BE3#	M1	DP4	D26	KEN#	A8	TCK	AE22
BE4#	M2	DP5	C23	LOCK#	D1	TDI	AE21
BE5#	N1	DP6	A19	M/IO#	A11	TDO	AF21
BE6#	P1	DP7	B14	NA#	B7	TMS	AF20
BE7#	N2	EADS#	G1	NMI/LINT1	AE12	TRST#	AF19
BOFF#	A7	EWBE#	A10	PCD	G3	W/R#	H1
BP2	B12	FERR#	B13	PCHK#	C4	WB/WT#	A6

D10	AE10	D11	AF10	D12	AE10	CLK	F2
STPCLK#	AF17						

**Table 5. No Connect, Power Supply and Ground Pin Cross Reference (HL-PBGA Package)**

V <sub>CC2</sub>							
C6	D9	D19	R4	AB2	AC13	AC19	AE17
C8	D12	E4	U4	AB23	AC14	AC20	AE18
C21	D13	F3	V3	AC4	AC15	AC21	
D5	D15	L23	Y2	AC6	AC16	AC23	
D7	D17	R3	AA3	AC8	AC18	AD19	
V <sub>CC3</sub>							
C20	D14	F23	J23	N23	V2	AA4	AC10
C22	D16	G4	K4	R23	V23	AB4	AC11
D4	D18	G23	K23	T4	W3	AC5	AC17
D6	D23	H23	M4	T23	Y3	AC7	AC22
D10	E23	J4	N4	U23	Y23	AC9	AD5
D11	F4						
V <sub>SS</sub>							
B6	C14	D20	H3	P4	W4	AD6	AD16
B11	C15	D21	H24	P23	W23	AD7	AD17
C3	C16	D22	J24	R24	Y4	AD8	AD18
C5	C17	E2	K3	T3	AA2	AD9	AD20
C7	C18	E3	L24	T24	AA23	AD10	AD21
C9	C19	E24	M3	U3	AB3	AD11	AD22
C10	C24	F2	M23	U24	AC3	AD13	AD24
C12	D3	F24	N3	V4	AD3	AD14	AE19
C13	D8	G24	P3	W2	AD4	AD15	AE20
No Connect (NC)							
AF18	T1						
Internal No Connect (INC)							
A1	A23	B1	L4	AC26	AD26	AE26	AF23
A2	A24	B2	AA26	AD1	AE1	AF1	AF24
A3	A25	E1	AB26	AD12	AE24	AF2	AF25
A4	A26	H4	AC12	AD25	AE25	AF3	AF26



## 4.4 Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to  $V_{CC3}$ . Unused active high inputs should be connected to GND ( $V_{SS}$ ).

No Connect (NC) pins must remain unconnected. Connection of NC pins may result in component failure or incompatibility with processor steppings.

## 4.5 Pin Quick Reference

This section gives a brief functional description of each pin. For a detailed description, see the Hardware Interface chapter in the *Embedded Pentium® Processor Family Developer's Manual*.

**Note:** All input pins must meet their AC/DC specifications to guarantee proper functional behavior.

The # symbol at the end of a signal name indicates that the active or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level. Square brackets around a signal name indicate that the signal is defined only at RESET.

The pins are classified as Input or Output based on their function in Master Mode. See the Error Detection chapter of the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204) for further information.

**Table 6. Quick Pin Reference (Sheet 1 of 6)**

Symbol	Type	Name and Function
A20M#	I	When the <b>address bit 20 mask</b> pin is asserted, the Pentium® processor with MMX™ technology emulates the address wraparound at 1 Mbyte, which occurs on the 8086. When A20M# is asserted, the processor masks physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode.
A31–A3	I/O	As outputs, the <b>address</b> lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31–A5.
ADS#	O	The <b>address status</b> indicates that a new valid bus cycle is currently being driven by the processor.
AHOLD	I	In response to the assertion of <b>address hold</b> , the processor will stop driving the address lines (A31–A3) and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	<b>Address parity</b> is driven by the processor with even parity information on all processor generated cycles in the same clock that the address is driven. Even parity must be driven back to the processor during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated.
APCHK#	O	The <b>address parity check</b> status pin is asserted two clocks after EADS# is sampled active if the processor has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected.
BE7#–BE5# BE4#–BE0#	O I/O	The <b>byte enable</b> pins are used to determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31–3).

Table 6. Quick Pin Reference (Sheet 2 of 6)

Symbol	Type	Name and Function
BF2–BF0	I	<p>The <b>Bus Frequency</b> pins determine the bus-to-core frequency ratio. BF [2:0] are sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF[2:0] must not change values while RESET is active. See Table 7 for Bus Frequency Selection.</p> <p>In order to override the internal defaults and guarantee that the BF[2:0] inputs remain stable while RESET is active, these pins should be strapped directly to or through a pullup/pulldown resistor to <math>V_{CC3}</math> or ground. Driving these pins with active logic is not recommended unless stability during RESET can be guaranteed.</p> <p>During power up, RESET should be asserted prior to or ramped simultaneously with the core voltage supply to the processor.</p>
BOFF#	I	<p>The <b>backoff</b> input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the processor will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the processor restarts the aborted bus cycle(s) in their entirety.</p>
[APICEN] PICD1	I	<p><b>Advanced Programmable Interrupt Controller Enable</b> enables or disables the on-chip APIC interrupt controller. If sampled high at the falling edge of RESET, the APIC is enabled. APICEN shares a pin with the PICD1 signal.</p>
BP3–BP2 PM/BP1–BP0	O	<p>The <b>breakpoint</b> pins (BP3–0) correspond to the debug registers, DR3–DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches.</p> <p>BP1 and BP0 are multiplexed with the <b>performance monitoring</b> pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.</p>
BRDY#	I	<p>The <b>burst ready</b> input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the processor data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.</p>
BREQ	O	<p>The <b>bus request</b> output indicates to the external system that the processor has internally generated a bus request. This signal is always driven whether or not the processor is driving its bus.</p>
BUSCHK#	I	<p>The <b>bus check</b> input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the processor will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the processor will vector to the machine check exception.</p> <p>To assure that BUSCHK# will always be recognized, STPCLK# must be deasserted any time BUSCHK# is asserted by the system, before the system allows another external bus cycle. If BUSCHK# is asserted by the system for a snoop cycle while STPCLK# remains asserted, usually (if MCE=1) the processor will vector to the exception after STPCLK# is deasserted. But if another snoop to the same line occurs during STPCLK# assertion, the processor can lose the BUSCHK# request.</p>
CACHE#	O	<p>For processor-initiated cycles, the <b>cache</b> pin indicates internal cacheability of the cycle (if a read), and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, the processor will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).</p>
CLK	I	<p>The <b>clock</b> input provides the fundamental timing for the processor. Its frequency is the operating frequency of the processor external bus and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST# and PICD0–1 are specified with respect to the rising edge of CLK.</p> <p>This pin is 2.5 V-tolerant-only on the low-power embedded Pentium processor with MMX technology.</p> <p>It is recommended that CLK begin 150 ms after <math>V_{CC}</math> reaches its proper operating level. This recommendation is only to assure the long term reliability of the device.</p>



Table 6. Quick Pin Reference (Sheet 3 of 6)

Symbol	Type	Name and Function
D/C#	O	The <b>data/code</b> output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D63–D0	I/O	These are the 64 <b>data lines</b> for the processor. Lines D7–D0 define the least significant byte of the data bus; lines D63–D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12 or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7–DP0	I/O	These are the <b>data parity</b> pins for the processor. There is one for each byte of the data bus. They are driven by the processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor with voltage reduction technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the processor. DP7 applies to D63–D56; DP0 applies to D7–D0.
EADS#	I	This signal indicates that a valid <b>external address</b> has been driven onto the processor address pins to be used for an inquire cycle.
EWBE#	I	The <b>external write buffer empty</b> input, when inactive (high), indicates that a write cycle is pending in the external system. When the processor generates a write and EWBE# is sampled inactive, the processor will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The <b>floating-point error</b> pin is driven active when an unmasked floating-point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using MS-DOS type floating-point error reporting.
FLUSH#	I	When asserted, the <b>cache flush</b> input forces the processor to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the processor indicating completion of the writeback and invalidation. If FLUSH# is sampled low when RESET transitions from high to low, three-state test mode is entered.
HIT#	O	The <b>hit</b> indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The <b>hit to a modified line</b> output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The <b>bus hold acknowledge</b> pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the processor will resume driving the bus. If the processor has a bus cycle pending, it will be driven in the same clock that HLDA is de-asserted.
HOLD	I	In response to the <b>bus hold request</b> , the processor will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The processor will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The processor will recognize HOLD during reset.
IERR#	O	The <b>internal error</b> pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the processor will assert the IERR# pin for one clock and then shutdown.



		On the first clock after <b>INIT</b> is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will stop execution and wait for an external interrupt.
INIT	I	The processor <b>initialization</b> input pin forces the processor to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power up.  If INIT is sampled high when RESET transitions from high to low, the processor will perform built-in self test prior to the start of program execution.
INTR	I	An active <b>maskable interrupt</b> input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the processor will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized.
INV	I	The <b>invalidation</b> input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The <b>cache enable</b> pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the processor generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.
LOCK#	O	The <b>bus lock</b> pin indicates that the current bus cycle is locked. The processor will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be de-asserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The <b>memory/input-output</b> is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active <b>next address</b> input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The processor will issue ADS# for a pending cycle two clocks after NA# is asserted. The processor supports up to two outstanding bus cycles.
NMI	I	The <b>non-maskable interrupt</b> request signal indicates that an external non-maskable interrupt has been generated.
PCD	O	The <b>page cache disable</b> pin reflects the state of the PCD bit in CR3; Page Directory Entry or Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page-by-page basis.
PCHK#	O	The <b>parity check</b> output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned.

Table 6. Quick Pin Reference (Sheet 5 of 6)

Symbol	Type	Name and Function
PEN#	I	The <b>parity enable</b> input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock, a data parity error is detected. The processor will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the processor will vector to the machine check exception before the beginning of the next instruction.
PICCLK	I	The APIC interrupt controller serial data bus clock is driven into the <b>programmable interrupt controller clock</b> input of the Pentium processor with MMX technology.
PICD0– PICD1 [APICEN]	I/O	<b>Programmable interrupt controller data lines 0–1</b> of the Pentium processor with MMX technology comprise the data portion of the APIC 3-wire bus. They are open-drain outputs that require external pull-up resistor. These signals are multiplexed with APICEN.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1–0 pins are multiplexed with the <b>performance monitoring 1-0</b> pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The <b>probe ready</b> output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active or Probe Mode being entered.
PWT	O	The <b>page writethrough</b> pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external writeback indication on a page-by-page basis.
R/S#	I	The <b>run/stop</b> input is provided for use with the Intel debug port. Please refer to the <i>Embedded Pentium® Processor Family Developer's Manual</i> (Order Number 273204) for more details.
RESET	I	<b>RESET</b> forces the processor to begin execution at a known state. All the processor internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH# and INIT are sampled when RESET transitions from high to low to determine if three-state test mode will be entered or if BIST will be run.
SCYC	O	The <b>split cycle</b> output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SMI#	I	The <b>system management interrupt</b> causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACK#	O	An active <b>system management interrupt active</b> output indicates that the processor is operating in System Management Mode.
STPCLK#	I	Assertion of the <b>stop clock</b> input signifies a request to stop the internal clock of the Pentium processor with voltage reduction technology thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a Stop Grant Acknowledge cycle. When STPCLK# is asserted, the processor will still respond to external snoop requests.
TCK	I	The <b>testability clock</b> input provides the clocking function for the processor boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the processor during boundary scan.
TDI	I	The <b>test data input</b> is a serial input for the test logic. TAP instructions and data are shifted into the processor on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.

Table 6. Quick Pin Reference (Sheet 6 of 6)

Symbol	Type	Name and Function
TDO	O	The <b>test data output</b> is a serial output of the test logic. TAP instructions and data are shifted out of the processor on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the <b>test mode select</b> input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the <b>test reset</b> input allows the TAP controller to be asynchronously initialized.
VCC2DET#	N/A	Differentiate between the Pentium Processor with MMX technology and the low-power embedded Pentium processor with MMX technology. This is an Internal No Connect (INC) pin on the low-power embedded Pentium processor with MMX technology. This pin is not defined on the HL-PBGA package.
V <sub>CC2</sub>	I	These pins are the power inputs to the core: 1.9 V input for 166/266 MHz PPGA; 1.8 V for 166 MHz HL-PBGA; 2.0 V for 166 MHz HL-PBGA.
V <sub>CC3</sub>	I	These pins are the 2.5 V power inputs to the I/O.
V <sub>SS</sub>	I	These pins are the ground inputs.
W/R#	O	<b>Write/read</b> is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The <b>writeback/writethrough</b> input allows a data cache line to be defined as writeback or writethrough on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

## 4.6 Bus Fraction (BF) Selection

Each low-power embedded Pentium processor with MMX technology must be externally configured with the BF2–BF0 pins to operate in the specified bus fraction mode. Operation out of the specification is not supported. For example, a 266 MHz low-power embedded Pentium processor with MMX technology supports only the 1/4 bus fraction mode and not the 2/5 mode.

The BF configuration pins are provided to select the allowable bus/core ratios of 2/5 and 1/4. The low-power embedded Pentium processor with MMX technology multiplies the input CLK to achieve the higher internal core frequencies. The internal clock generator requires a constant frequency CLK input to within  $\pm 250$  ps; therefore, the CLK input cannot be changed dynamically.

The external bus frequency is set during power-up Reset through the CLK pin. The low-power embedded Pentium processor with MMX technology samples the BF0, BF1 and BF2 pins on the falling edge of RESET to determine which bus/core ratio to use.

Table 7 summarizes the operation of the BF pins on the low-power embedded Pentium processor with MMX technology.

**Note:** BF pins must meet a 1 ms setup time to the falling edge of RESET and *must not change value while RESET is active*. Once a frequency is selected, it may not be changed with a warm reset. Changing this speed or ratio requires a “power on” RESET pulse initialization.



Table 7. Bus Frequency Selection

BF2	BF1	BF0	Bus/Core Ratio	Max Bus/Core Frequency (MHz)
0	0	0	2/5	66/166
1	0	0	1/4	66/266

NOTE: All other BF2–BF0 settings are reserved on the low-power embedded Pentium processor with MMX technology.

## 4.7 The CPUID Instruction

The CPUID instruction allows software to determine the type and features of the processor on which it is executing. When executing CPUID, the low-power embedded Pentium processor with MMX technology behaves like the Pentium processor and the Pentium processor with MMX technology as follows:

- If the value in EAX is '0', then the 12-byte ASCII string "Genuine Intel" (little endian) is returned in EBX, EDX and ECX. Also, a '1' is returned to EAX.
- If the value in EAX is '1', then the processor version is returned in EAX and the processor capabilities are returned in EDX. The values of EAX and EDX for the low-power embedded Pentium processor with MMX technology are given below.
- If the value in EAX is neither '0' nor '1', the low-power embedded Pentium processor with MMX technology writes '0' to all registers.

The following EAX and EDX values are defined for the CPUID instruction executed with EAX = '1'. The processor version EAX bit assignments are given in Figure 6. The EDX bit assignments are shown in Figure 7.

Figure 6. EAX Bit Assignments for CPUID

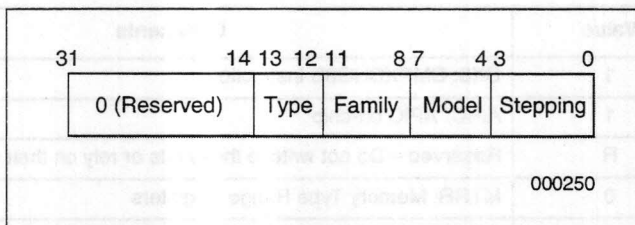
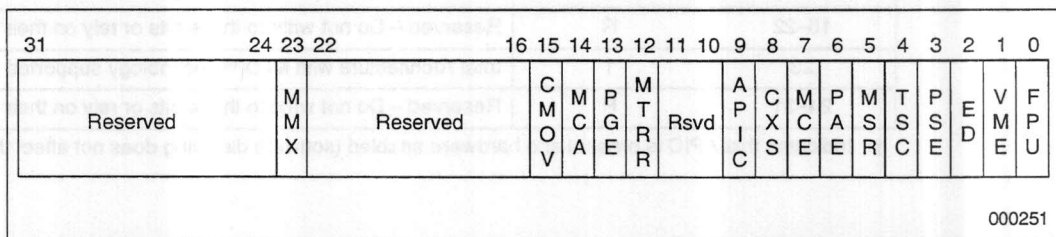


Figure 7. EDX Bit Assignments for CPUID



The type field for low-power embedded Pentium processor with MMX technology is the same as Pentium processor with MMX technology (type = 00H). The family field is the same as all other Pentium processors (family = 5H). However, the model field is different: the Pentium processor model number is 2H, the Pentium processor with MMX technology model number is 4H, and the low-power embedded Pentium processor with MMX technology model number is 8H. The stepping field indicates the revision number of a model. The stepping ID of A-step for the low-power embedded Pentium processor with MMX technology is 1H. Stepping ID will be documented in the low-power embedded Pentium processor with MMX technology stepping information.

After masking the reserve bits, all low-power embedded Pentium processor with MMX technology-based products will get a value of 0x008003BF (assuming the APIC is enabled at boot), or 0x008001BF (when the APIC is disabled, using the APICEN boot pin) in EDX upon completion of the CPUID instruction.

**Table 8. EDX Bit Assignment Definitions for CPUID**

Bit	Value	Comments
0	1	FPU: Floating-point Unit on-chip
1	1	VME: Virtual-8086 Mode Enhancements
2	1	DE: Debugging Extensions
3	1	PSE: Page Size Extension
4	1	TSC: Time Stamp Counter
5	1	MSR Pentium® Processor MSR
6	0	PAE: Physical Address Extension
7	1	MCE: Machine Check Exception

**Table 9. EDX Bit Assignment Definitions for CPUID**

Bit	Value	Comments
8	1	CX8: CMPXCHG8B Instruction
9	1	APIC: APIC on-chip <sup>†</sup>
10–11	R	Reserved – Do not write to these bits or rely on their values
12	0	MTRR: Memory Type Range Registers
13	0	PGE: Page Global Enable
14	0	MCA: Machine Check Architecture
15–22	R	Reserved – Do not write to these bits or rely on their values
23	1	Intel Architecture with MMX™ technology supported
24–31	R	Reserved – Do not write to these bits or rely on their values

<sup>†</sup> Indicates that APIC is present and hardware enabled (software disabling does not affect this bit).

## 4.8 Boundary Scan Chain List

The boundary scan chain list for the low-power embedded Pentium processor with MMX technology is different than the Pentium processor with MMX technology due to the removal of some pins. The boundary scan register for the low-power embedded Pentium processor with MMX technology contains a cell for each pin. Following is the bit order of the low-power embedded Pentium processor with MMX technology boundary scan register (left to right, top to bottom):

TDI → disapsba<sup>†</sup>, PICD1, PICD0, Reserved, PICCLK, D0, D1, D2, D3, D4, D5, D6, D7, DP0, D8, D9, D10, D11, D12, D13, D14, D15, DP1, D16, D17, D18, D19, D20, D21, D22, D23, DP2, D24, D25, D26, D27, D28, D29, D30, D31, DP3, D32, D33, D34, D35, D36, D37, D38, D39, DP4, D40, D41, D42, D43, D44, D45, D46, diswr<sup>†</sup>, D47, DP5, D48, D49, D50, D51, D52, D53, D54, D55, DP6, D56, D57, D58, D59, D60, D61, D62, D63, DP7, IERR#, FERR#, PM0BP0, PM1BP1, BP2, BP3, MIO#, CACHE#, EWBE#, INV, AHOLD, KEN#, BRDYC#, BRDY#, BOFF#, NA#, WBWT#, HOLD, disbus<sup>†</sup>, disbusl<sup>†</sup>, dismisc<sup>†</sup>, dismisca<sup>†</sup>, SMIACT#, PRDY, PCHK#, APCHK#, BREQ, HLDA, AP, LOCK#, PCD, PWT, DC#, EADS#, ADS#, HITM#, HIT#, WR#, BUSCHK#, FLUSH#, A20M#, BE0#, BE1#, BE2#, BE3#, BE4#, BE5#, BE6#, BE7#, SCYC, CLK, RESET, disabus<sup>†</sup>, A20, A19, A18, A17, A16, A15, A14, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A31, A30, A29, A28, A27, A26, A25, A24, A23, A22, A21, NMI, RS#, INTR, SMI#, IGNNE#, INIT, PEN#, Reserved, BF0, BF1, BF2, STPCLK#, Reserved, Reserved, Reserved, Reserved → TDO

“Reserved” includes the no connect “NC” signals on the low-power embedded Pentium processor with MMX technology.

The cells marked with a dagger (†) are control cells that are used to select the direction of bi-directional pins or three-state the output pins. If “1” is loaded into the control cell, the associated pin(s) are three-stated or selected as input. The following lists the control cells and their corresponding pins:

Disabus:	A31–A3, AP
Disbus:	BE7#–BE0#, CACHE#, SCYC, M/IO#, D/C#, W/R#, PWT, PCD
Disbusl:	ADS#, LOCK#, ADSC#
Dismisc:	APCHK#, PCHK#, PRDY, BP3, BP2, PM1/BP1, PM0/BP0, FERR#, SMIACT#, BREQ, HLDA, HIT#, HITM#
Dismisca:	IERR#
Diswr:	D63–D0, DP7–DP0
Disapsba:	PICD1–PICD0



## 4.9 Pin Reference Tables

Table 10. Output Pins

Name <sup>(1)</sup>	Active Level	When Floated
ADS#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#–BE4#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#	Low	Bus Hold, BOFF#
FERR#	Low	
HIT#	Low	
HITM# <sup>(2)</sup>	Low	
HLDA	High	
IERR#	Low	
LOCK#	Low	Bus Hold, BOFF#
M/IO#, D/C#, W/R#	N/A	Bus Hold, BOFF#
PCHK#	Low	
BP3–BP2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC	High	Bus Hold, BOFF#
SMIACK#	Low	
TDO	N/A	All states except Shift-DR and Shift-IR
VCC2DET# <sup>(3)</sup>	N/A	Differentiates between the Pentium® processor with MMX™ technology and the low-power embedded Pentium processor with MMX technology

**NOTE:**

1. All output and input/output pins are floated during three-state test mode (except TDO).
2. HITM# pin has an internal pull-up resistor.
3. This pin is not on the HL-PBGA pinout.

Table 11. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
A20M#	LOW	Asynchronous		
AHOLD	HIGH	Synchronous		
BF0	N/A	Synchronous/RESET	Pulldown	
BF1	N/A	Synchronous/RESET	Pullup	
BF2	N/A	Synchronous/RESET	Pulldown	
BOFF#	LOW	Synchronous		
BRDY#	LOW	Synchronous	Pullup	Bus State T2,T12,T2P
BUSCHK#	LOW	Synchronous	Pullup	BRDY#
CLK	N/A			
EADS#	LOW	Synchronous		
EWBE#	LOW	Synchronous		BRDY#
FLUSH#	LOW	Asynchronous		
HOLD	HIGH	Synchronous		
IGNNE#	LOW	Asynchronous		
INIT	HIGH	Asynchronous		
INTR	HIGH	Asynchronous		
INV	HIGH	Synchronous		EADS#
KEN#	LOW	Synchronous		First BRDY#/NA#
NA#	LOW	Synchronous		Bus State T2,TD,T2P
NMI	HIGH	Asynchronous		
PEN#	LOW	Synchronous		BRDY#
PICCLK	HIGH	Asynchronous	Pullup	
R/S#	N/A	Asynchronous	Pullup	
RESET	HIGH	Asynchronous		
SMI#	LOW	Asynchronous	Pullup	
STPCLK#	LOW	Asynchronous	Pullup	
TCK	N/A		Pullup	
TDI	N/A	Synchronous/TCK	Pullup	TCK
TMS	N/A	Synchronous/TCK	Pullup	TCK
TRST#	LOW	Asynchronous	Pullup	
WB/WT#	N/A	Synchronous		First BRDY#/NA#

Table 12. Input/Output Pins

Name	Active Level	When Floated <sup>(1)</sup>	Qualified (when an input)	Internal Resistor
A31–A3	N/A	Address Hold, Bus Hold, BOFF#	EADS#	
AP	N/A	Address Hold, Bus Hold, BOFF#	EADS#	
BE3#–BE0#	LOW	Bus Hold, BOFF#	RESET	Pulldown <sup>(2)</sup>
D63–D0	N/A	Bus Hold, BOFF#	BRDY#	
DP7–DP0	N/A	Bus Hold, BOFF#	BRDY#	
PICD0	N/A			Pullup
PICD1[APICEN]	N/A			Pulldown

**NOTE:**

1. All output and input/output pins are floated during three-state test mode (except TDO).
2. BE3#–BE0# have pulldowns during RESET only.

## 4.10 Pin Grouping According to Function

Table 13. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT, BF[2:0]
Address Bus	A31–A3, BE7#–BE0#
Address Mask	A20M#
Data Bus	D63–D0
Address Parity	AP, APCHK#
APIC Support	PICCLK, PICD0–PICD1
Data Parity	DP7–DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, BRDY#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Interrupts	INTR, NMI
Floating-point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3–BP2
Clock Control	STPCLK#
Debugging	R/S#, PRDY



## 5.0 Electrical Specifications

This section contains preliminary information on new products in production. The specifications are subject to change without notice.

### 5.1 Absolute Maximum Ratings

**Warning:** The following values are stress ratings only. Functional operation at the maximum ratings is not implied nor guaranteed. Functional operating conditions are given in the AC and DC specification tables. Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium processor with MMX technology contains protective circuitry to resist damage from Electrostatic Discharge (ESD), always take precautions to avoid high static voltages or electric fields.

Table 14. Absolute Maximum Ratings

Parameter	Maximum Rating
Case temperature under bias	–65° C to 110° C
Storage temperature	–65° C to 150° C
V <sub>CC3</sub> supply voltage with respect to V <sub>SS</sub>	–0.5 V to +3.2 V
V <sub>CC2</sub> supply voltage with respect to V <sub>SS</sub>	–0.5 V to +2.8 V
2.5 V only buffer DC input voltage	–0.5 V to V <sub>CC3</sub> +0.5 V (not to exceed V <sub>CC3</sub> max)

### 5.2 DC Specifications

Tables 16, 17, 18 and 19 list the DC specifications which apply to the low-power embedded Pentium processor with MMX technology.

#### 5.2.1 Power Sequencing

There is no specific sequence required for powering up or powering down the V<sub>CC2</sub> and V<sub>CC3</sub> power supplies. However, it is recommended that the V<sub>CC2</sub> and V<sub>CC3</sub> power supplies be either both ON or both OFF within one second of each other.

The I/O voltage V<sub>CC3</sub> is 2.5 V. The core voltage V<sub>CC2</sub> is 1.9 V for PPGA. The core voltage V<sub>CC2</sub> for the HL-PBGA package type is 1.8 V (166 MHz) or 2.0 V (266 MHz).

Table 15.  $V_{CC}$  and  $T_{CASE}$  Specifications

Package	$T_{CASE}$	Supply	Min Voltage	Max Voltage	Voltage Tolerance	Frequency
PPGA	0°C to 85°C	$V_{CC2}$	1.750 V	2.04 V	1.9 V $\pm$ 7.5%	166/266 MHz
		$V_{CC3}$	2.375 V	2.625 V	2.5 V $\pm$ 5%	166/266 MHz
HL-PBGA	0°C to 95°C	$V_{CC2}$	1.665 V	1.935 V	1.8 V $\pm$ 7.5%	166 MHz
		$V_{CC2}$	1.85 V	2.15 V	2.0 V $\pm$ 7.5%	266 MHz
		$V_{CC3}$	2.375 V	2.625 V	2.5 V $\pm$ 5%	166/266 MHz

Table 16. DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL3}$	Input Low Voltage	-0.3	0.5	V	
$V_{IH3}$	Input High Voltage	$V_{CC3} - 0.7$	$V_{CC3} + 0.3$	V	TTL Level
$V_{OL3}$	Output Low Voltage		0.4	V	TTL Level, (1)
$V_{OH3}$	Output High Voltage	$V_{CC3} - 0.4$ $V_{CC3} - 0.2$		V	TTL Level, (2)
				V	TTL Level, (3)

**NOTES:**

1. Parameter measured at -4 mA.
2. Parameter measured at 3 mA.
3. Parameter measured at 1 mA; not 100% tested, guaranteed by design.

The values in Table 17 should be used for power supply design. The values were determined using a worst case instruction mix and maximum  $V_{CC}$ . Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from Stop Clock to full Active modes.

Table 17.  $I_{CC}$  Specifications

Symbol	Parameter	Min	Max	Unit	Notes
$I_{CC2}$	Power Supply Current		2.35 (HL-PBGA)	A	166 MHz
			2.5 (PPGA)	A	166 MHz
			4.00	A	266 MHz
$I_{CC3}$	Power Supply Current		0.38	A	166 MHz
			0.38	A	266 MHz

Table 18. Power Dissipation Requirements for Thermal Design

Parameter	Typical <sup>(1)</sup>	Max <sup>(2)</sup>	Unit	Frequency
Thermal Design Power		4.1 (HL-PBGA)	Watts	166 MHz
		4.5 (PPGA)	Watts	166 MHz
		7.6	Watts	266 MHz
Active Power <sup>(3)</sup>	2.9		Watts	166 MHz
	4.5		Watts	266 MHz
Stop Grant/Auto Halt Powerdown Power Dissipation <sup>(4)</sup>		0.70	Watts	166 MHz
		0.70	Watts	266 MHz
Stop Clock Power <sup>(5)</sup>		0.06	Watts	166 MHz
		0.06	Watts	266 MHz

**NOTES:**

1. This is the typical power dissipation in a system. This value is expected to be the average value that will be measured in a system using a typical device at the specified voltage running typical applications. This value is dependent upon the specific system configuration. Typical power specifications are not tested.
2. Systems must be designed to thermally dissipate the maximum thermal design power unless the system uses thermal feedback to limit processor's maximum power. The maximum thermal design power is determined using a worst-case instruction mix and also takes into account the thermal time constant of the package.
3. Active power is the average power measured in a system using a typical device running typical applications under normal operating conditions at nominal  $V_{CC}$  and room temperature.
4. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction. When in this mode, the processor has a new feature which allows it to power down additional circuitry to enable lower power dissipation. This is the power without snooping at the specified voltage and with TR12 bit 21 set. In order to enable this feature, TR12 bit 21 must be set to 1 (the default is 0 or disabled). Stop grant/Auto Halt Powerdown power dissipation without TR12 bit 21 set may be higher. The Max rating may be changed in future specification updates.
5. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input. This is specified at a  $T_{CASE}$  of 50 °C.

Table 19. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
$C_{IN}$	Input Capacitance		15	pF	(4)
$C_O$	Output Capacitance		20	pF	(4)
$C_{I/O}$	I/O Capacitance		25	pF	(4)
$C_{CLK}$	CLK Input Capacitance		15	pF	(4)
$C_{TIN}$	Test Input Capacitance		15	pF	(4)
$C_{TOUT}$	Test Output Capacitance		20	pF	(4)
$C_{TCK}$	Test Clock Capacitance		15	pF	(4)
$I_{LI}$	Input Leakage Current		±15	μA	$0 < V_{IN} < V_{IL}$ , $V_{IH} < V_{IN} < V_{CC3}$ , (1)
$I_{LO}$	Output Leakage Current		±15	μA	$0 < V_{IN} < V_{IL}$ , $V_{IH} < V_{IN} < V_{CC3}$ , (1)
$I_{IH}$	Input High Leakage Current		200	μA	$V_{IN} = V_{CC3} - 0.4$ V, (3)
$I_{IL}$	Input Low Leakage Current		-400	μA	$V_{IN} = 0.4$ V (2, 5)

**NOTES:**

1. This parameter is for inputs/outputs without an internal pull up or pull down.
2. This parameter is for inputs with an internal pull up.
3. This parameter is for inputs with an internal pull down.
4. Guaranteed by design.
5. This specification applies to the HITM# pin when it is driven as an input (e.g., in JTAG mode).



## 5.3 AC Specifications

The AC specifications of the low-power embedded Pentium processor with MMX technology consist of setup times, hold times, and valid delays at 0 pF.

### 5.3.1 Power and Ground

For clean on-chip power distribution, the PPGA has 25  $V_{CC2}$  (core power), 28  $V_{CC3}$  (I/O power) and 53  $V_{SS}$  (ground) inputs. For the HL-PBGA package, there are 42  $V_{CC3}$ , 37  $V_{CC2}$  and 72  $V_{SS}$  inputs.

Power and ground connections must be made to all external  $V_{CC2}$ ,  $V_{CC3}$  and  $V_{SS}$  pins. On the circuit board, all  $V_{CC2}$  pins must be connected to a proper voltage  $V_{CC2}$  plane or island (core voltage determined by package type/frequency). All  $V_{CC3}$  pins must be connected to a 2.5 V  $V_{CC3}$  plane. All  $V_{SS}$  pins must be connected to a  $V_{SS}$  plane. Please refer to Table 2 on page 17 for the list of  $V_{CC2}$ ,  $V_{CC3}$  and  $V_{SS}$  pins.

### 5.3.2 Decoupling Recommendations

Liberal decoupling capacitance should be placed near the processor. The processor's large address and data buses can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible. These capacitors should be evenly distributed around each component on the power plane. Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

Power transients also occur as the processor rapidly transitions from a low level power consumption to a high level one (or high to low power transition). A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the processor to enter the Auto HALT Powerdown state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the processor.

Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100  $\mu$ F range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the processor on both  $V_{CC2}$  plane and  $V_{CC3}$  plane to ensure that the supply voltages stay within specified limits during changes in the supply current during operation.

### 5.3.3 Connection Specifications

All NC/INC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to  $V_{CC3}$ . Unused active high inputs should be connected to ground.

### 5.3.4 AC Timings

The AC specifications given in Table 20 consist of output delays, input setup requirements and input hold requirements for the standard 66 MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to  $V_{CC3}/V_{CC2}$  for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, asynchronous inputs must be stable for correct operation.

Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays. Do not select a bus fraction and clock speed which will cause the processor to exceed its internal maximum frequency.

The following specifications apply to all standard TTL signals used with the Pentium processor family:

- TTL input test waveforms are assumed to be 0 to 2.5 V transitions with 1.0 V/ns rise and fall times.
- $0.3 \text{ V/ns} \leq \text{input rise/fall time} \leq 5 \text{ V/ns}$ .
- All TTL timings are referenced from  $V_{CC3}/V_{CC2}$ .

**Table 20. Low-Power Embedded Pentium® Processor with MMX™ Technology AC Specifications (Sheet 1 of 3)**(See Table 15 for  $V_{CC}$  and  $T_{CASE}$  assumptions.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes (see Table 22)
	CLK Frequency	33.33	66.6	MHz		(1)
$t_{1a}$	CLK Period	15.0	30.0	ns	8	
$t_{1b}$	CLK Period Stability		±250	ps		(2, 3)
$t_2$	CLK High Time	4.0		ns	8	@ $V_{CC3} - 0.7$ V, (2)
$t_3$	CLK Low Time	4.0		ns	8	@ 0.5 V, (2)
$t_4$	CLK Fall Time	0.15	1.5	ns	8	$V_{CC3} - 0.7$ V to 0.5 V, (2, 4)
$t_5$	CLK Rise Time	0.15	1.5	ns	8	0.5 V to $V_{CC3} - 0.7$ V, (2, 4)
$t_{6a}$	PWT, PCD, CACHE# Valid Delay	1.0	7.0	ns	9	
$t_{6b}$	AP Valid Delay	1.0	8.5	ns	9	
$t_{6c}$	LOCK#, Valid Delay	0.9	7.0	ns	9	
$t_{6d}$	ADS# Valid Delay	1.0	6.2	ns	9	
$t_{6e}$	A31–A3 Valid Delay	0.8	6.4	ns	9	
$t_{6f}$	M/I/O# Valid Delay	0.8	6.2	ns	9	
$t_{6g}$	BE7#–BE0#, D/C#, W/R#, SCYC Valid Delay	0.8	7.0	ns	9	
$t_7$	ADS#, AP, A31–A3, PWT, PCD, BE7#–BE0#, M/I/O#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	ns	10	(2)
$t_{8a}$	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	ns	9	(5)
$t_{8b}$	PCHK# Valid Delay	1.0	7.0	ns	9	(5)
$t_{9a}$	BREQ Valid Delay	1.0	8.0	ns	9	(5)
$t_{9b}$	SMIACK# Valid Delay	1.0	7.3	ns	9	(5)
$t_{9c}$	HLDA Valid Delay	1.0	6.8	ns	9	(5)
$t_{10a}$	HIT# Valid Delay	1.0	6.8	ns	9	
$t_{10b}$	HITM# Valid Delay	0.9	6.0	ns	9	
$t_{11a}$	PM1–PM0, BP3–BP0 Valid Delay	1.0	10.0	ns	9	
$t_{11b}$	PRDY Valid Delay	1.0	8.0	ns	9	
$t_{12}$	D63–D0, DP7–DP0 Write Data Valid Delay	1.0	7.7	ns	9	
$t_{13}$	D63–D0, DP3–D0 Write Data Float Delay		10.0	ns	10	(2)
$t_{14}$	A31–A5 Setup Time	6.0		ns	11	(6)
$t_{15}$	A31–A5 Hold Time	1.0		ns	11	
$t_{16a}$	INV, AP Setup Time	5.0		ns	11	
$t_{16b}$	EADS# Setup Time	5.0		ns	11	
$t_{17}$	EADS#, INV, AP Hold Time	1.0		ns	11	



**Table 20. Low-Power Embedded Pentium® Processor with MMX™ Technology AC Specifications (Sheet 2 of 3)**

(See Table 15 for  $V_{CC}$  and  $T_{CASE}$  assumptions.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes (see Table 22)
$t_{18a}$	KEN# Setup Time	5.0		ns	11	
$t_{18b}$	NA#, WB/WT# Setup Time	4.5		ns	11	
$t_{19}$	KEN#, WB/WT#, NA# Hold Time	1.0		ns	11	
$t_{20}$	BRDY# Setup Time	4.75		ns	11	
$t_{21}$	BRDY# Hold Time	1.0		ns	11	
$t_{22}$	AHOLD, BOFF# Setup Time	5.5		ns	11	
$t_{23}$	AHOLD, BOFF# Hold Time	1.0		ns	11	
$t_{24a}$	BUSCHK#, EWBE#, HOLD, Setup Time	5.0		ns	11	
$t_{24b}$	PEN# Setup Time	4.8		ns	11	
$t_{25a}$	BUSCHK#, EWBE#, PEN# Hold Time	1.0		ns	11	
$t_{25b}$	HOLD Hold Time	1.5		ns	11	
$t_{26}$	A20M#, INTR, STPCLK# Setup Time	5.0		ns	11	(7, 8)
$t_{27}$	A20M#, INTR, STPCLK# Hold Time	1.0		ns	11	(9)
$t_{28}$	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		ns	11	(8, 10, 17)
$t_{29}$	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		ns	11	(9)
$t_{30}$	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs	11	(10, 11)
$t_{31}$	R/S# Setup Time	5.0		ns	11	(7, 8, 10)
$t_{32}$	R/S# Hold Time	1.0		ns	11	(9)
$t_{33}$	R/S# Pulse Width, Async.	2.0		CLKs	11	(10, 11)
$t_{34}$	D63–D0, DP7–0 Read Data Setup Time	2.8		ns	11	
$t_{35}$	D63–D0, DP7–0 Read Data Hold Time	1.5		ns	11	
$t_{36}$	RESET Setup Time	5.0		ns	11	(7, 8)
$t_{37}$	RESET Hold Time	1.0		ns	12	(9)
$t_{38}$	RESET Pulse Width, $V_{CC}$ & CLK Stable	15.0		CLKs	12	(10)
$t_{39}$	RESET Active After $V_{CC}$ & CLK Stable	1.0		mS	12	Power up

**Table 20. Low-Power Embedded Pentium® Processor with MMX™ Technology AC Specifications (Sheet 3 of 3)**

(See Table 15 for  $V_{CC}$  and  $T_{CASE}$  assumptions.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes (see Table 22)
$t_{40}$	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		ns	12	(7, 8, 10)
$t_{41}$	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		ns	12	(9)
$t_{42a}$	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	12	To RESET falling edge, (8)
$t_{42b}$	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	12	To RESET falling edge
$t_{43a}$	BF2–BF0 Setup Time	1.0		mS	12	To RESET falling edge, (10)
$t_{43b}$	BF2–BF0 Hold Time	2.0		CLKs	12	To RESET falling edge, (12)
$t_{43c}$	APICEN, BE4# Setup Time	2.0		CLKs	12	To RESET falling edge
$t_{43d}$	APICEN, BE4# Hold Time	2.0		CLKs	12	To RESET falling edge
$t_{44}$	TCK Frequency	—	16.0	MHz		
$t_{45}$	TCK Period	62.5		ns	8	
$t_{46}$	TCK High Time	25.0		ns	8	@ $V_{CC3} - 0.7$ V, (2)
$t_{47}$	TCK Low Time	25.0		ns	8	@ 0.5 V, (2)
$t_{48}$	TCK Fall Time		5.0	ns	8	$V_{CC3} - 0.7$ V to 0.5 V (2, 13, 14)
$t_{49}$	TCK Rise Time		5.0	ns	8	0.5 V to $V_{CC3} - 0.7$ V, (2, 13, 14)
$t_{50}$	TRST# Pulse Width	40.0		ns	14	Asynchronous, (2)
$t_{51}$	TDI, TMS Setup Time	5.0		ns	14	(15)
$t_{52}$	TDI, TMS Hold Time	13.0		ns	14	(15)
$t_{53}$	TDO Valid Delay	3.0	20.0	ns	14	(13)
$t_{54}$	TDO Float Delay		25.0	ns	14	(2, 13)
$t_{55}$	All Non-Test Outputs Valid Delay	3.0	20.0	ns	14	(13, 16, 17)
$t_{56}$	All Non-Test Outputs Float Delay		25.0	ns	14	(2, 13, 16, 17)
$t_{57}$	All Non-Test Inputs Setup Time	5.0		ns	14	(15, 16, 17)
$t_{58}$	All Non-Test Inputs Hold Time	13.0		ns	14	(15, 16, 17)

Table 21. APIC AC Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t <sub>60a</sub>	PICCLK Frequency	2	16.66	MHz		
t <sub>60b</sub>	PICCLK Period	60	500	ns	8	
t <sub>60c</sub>	PICCLK High Time	15		ns	8	
t <sub>60d</sub>	PICCLK Low Time	15		ns	8	
t <sub>60e</sub>	PICCLK Rise Time	0.15	2.5	ns	8	
t <sub>60f</sub>	PICCLK Fall Time	0.15	2.5	ns	8	
t <sub>60g</sub>	PICD0–1 Setup Time	3		ns	11	To PICCLK
t <sub>60h</sub>	PICD0–1 Hold Time	2.5		ns	11	To PICCLK
t <sub>60i</sub>	PICD0–1 Valid Delay (L to H)	4	38	ns	9	From PICCLK, (18)
t <sub>60j</sub>	PICD0–1 High Time (H to L)	4	22	ns	9	From PICCLK, (18)
t <sub>61</sub>	PICCLK Setup Time	5.0			11	To CLK
t <sub>62</sub>	PICCLK Hold Time	2.0			11	To CLK
t <sub>63</sub>	PICCLK Ratio (CLK/PICCLK)	4				(19)

Table 22. Notes to Tables 20 and 21

1. CLK input frequency must be either 33.33 MHz (+1 MHz) or 66.6 MHz (–1 MHz). Operation in the range between 33.33 MHz and 66.6 MHz is not supported.
2. Not 100 percent tested. Guaranteed by design.
3. These signals are measured on the rising edge of adjacent CLKs at V<sub>CC3</sub>/V<sub>CC2</sub>. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices. The internal clock generator requires a constant frequency CLK input to within +250 ps, and therefore the CLK input cannot be changed dynamically.
4. 0.87 V/ns ≤ CLK input rise/fall time ≤ 8.7 V/ns.
5. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions.
6. Timing (t<sub>14</sub>) is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active).
7. Setup time is required to guarantee recognition on a specific clock.
8. This input may be driven asynchronously.
9. Hold time is required to guarantee recognition on a specific clock.
10. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be de-asserted (inactive) for a minimum of two clocks before being returned active.
11. To guarantee proper asynchronous recognition, the signal must have been de-asserted (inactive) for a minimum of two clocks before being returned active and must meet the minimum pulse width.
12. BF2–BF0 should be strapped to V<sub>CC3</sub> or V<sub>SS</sub>.
13. Referenced to TCK falling edge.
14. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
15. Referenced to TCK rising edge.
16. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
17. During probe mode operation, do not use the boundary scan timings (t<sub>55</sub>–t<sub>58</sub>).
18. This assumes an external pull-up resistor to V<sub>CC</sub> and a lumped capacitive load. The pull-up resistor must be between 300 Ω and 1 KΩ, the capacitance must be between 20 pF and 120 pF, and the RC product must be between 6 ns and 36 ns.
19. The CLK to PICCLK ratio has to be an integer and the ratio (CLK/PICCLK) cannot be smaller than 4.



Figure 8. Clock Waveform

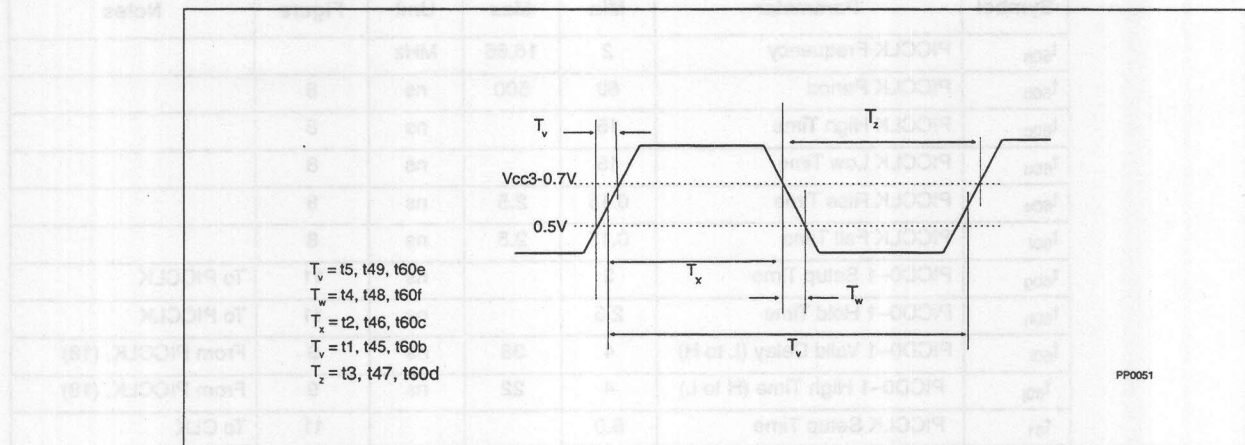


Figure 9. Valid Delay Timings

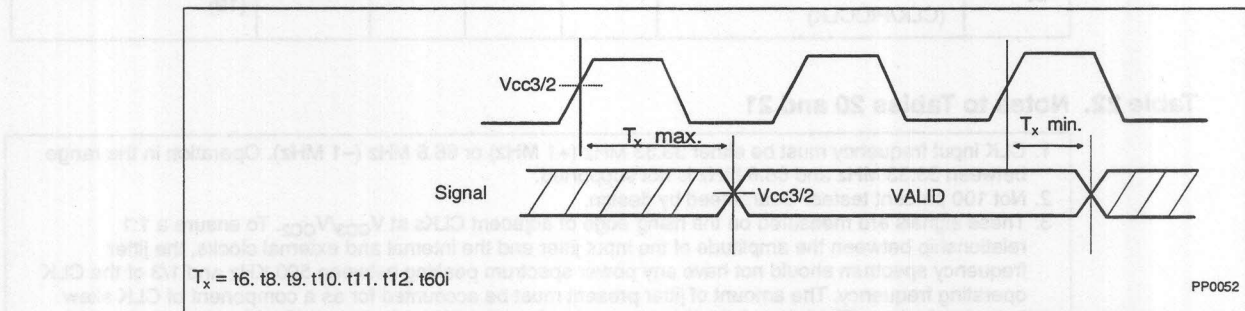


Figure 10. Float Delay Timings

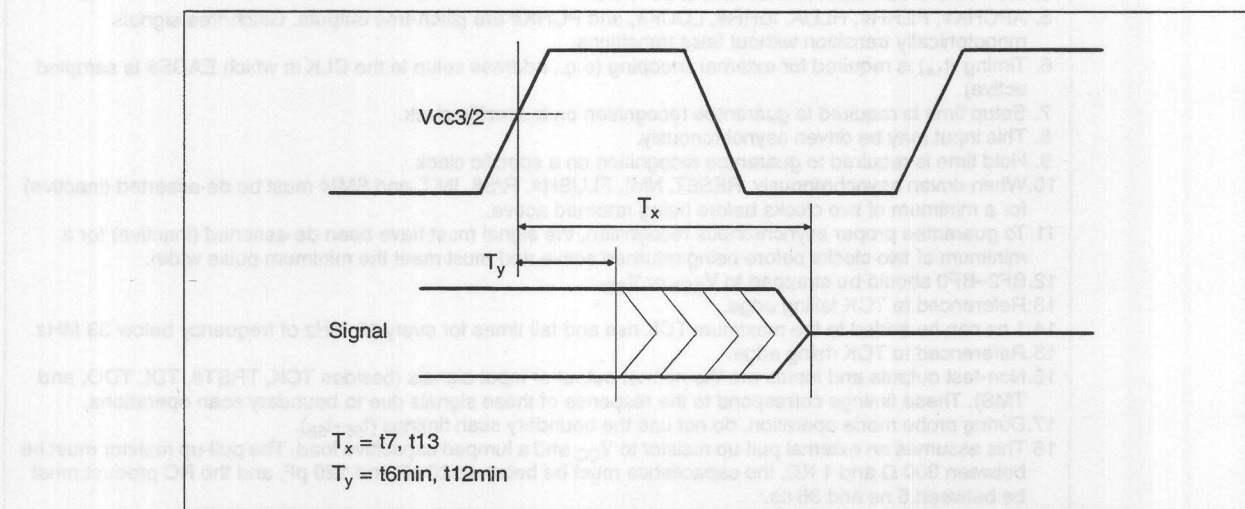


Figure 11. Setup and Hold Timings

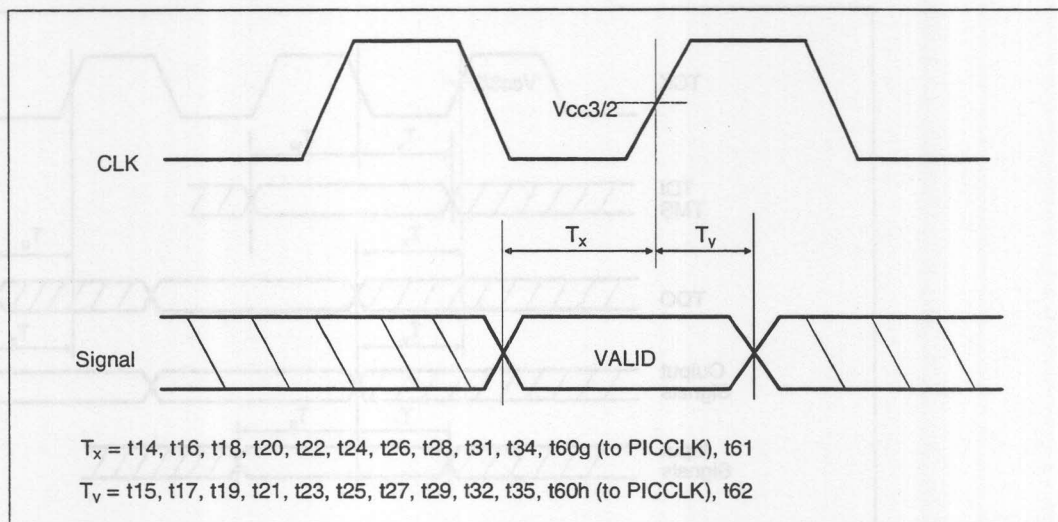


Figure 12. Reset and Configuration Timings

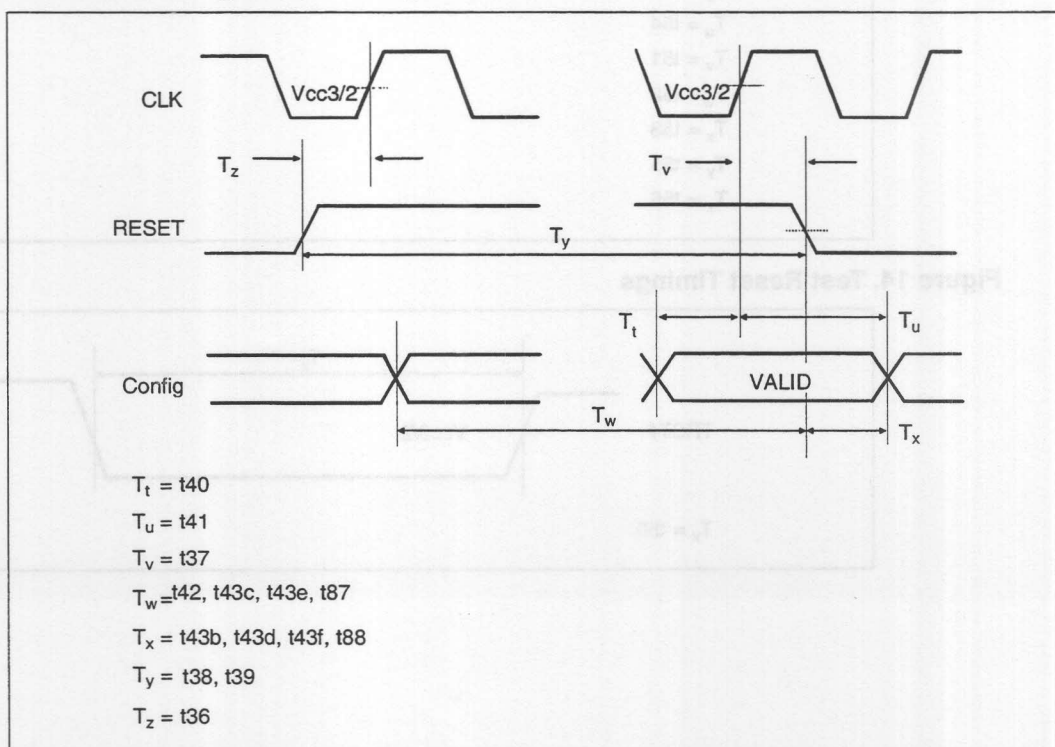


Figure 13. Test Timings

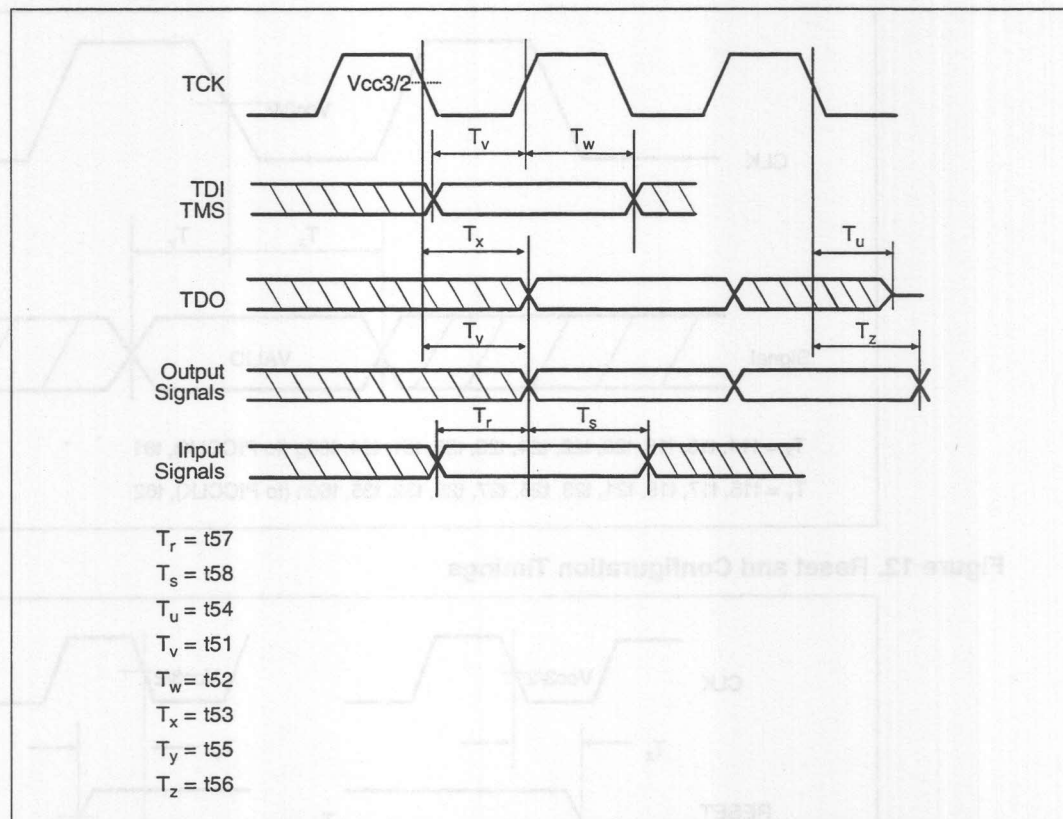
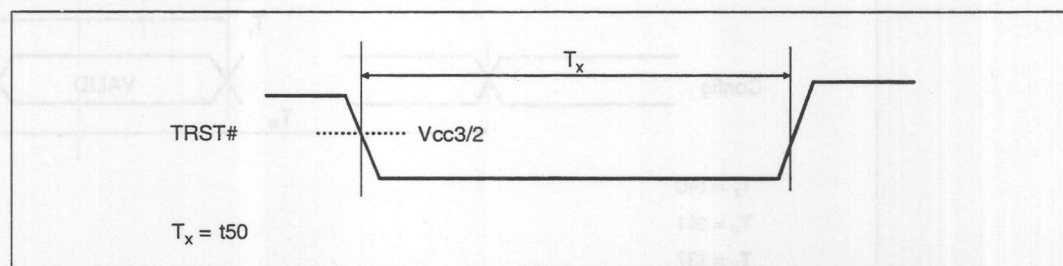


Figure 14. Test Reset Timings





## 5.4 I/O Buffer Models

This section describes the I/O buffer models of the low-power embedded Pentium processor with MMX technology.

The first order I/O buffer model is a simplified representation of the complex input and output buffers used. Figure 15 shows the structure of the input buffer model and Figure 16 shows the output buffer model. Table 23 and 24 show the parameters used to specify these models.

Although simplified, these buffer models will accurately model flight time and signal quality. For these parameters, there is very little added accuracy in a complete transistor model.

In addition to the input and output buffer parameters, input protection diode models are provided for added accuracy. These diodes have been optimized to provide ESD protection and provide some level of clamping. Although the diodes are not required for simulation, it may be more difficult to meet specifications without them.

Note, however, some signal quality specifications require that the diodes be removed from the input model. The series resistors ( $R_s$ ) are a part of the diode model. Remove these when removing the diodes from the input model.

**Figure 15. First Order Input Buffer Model**

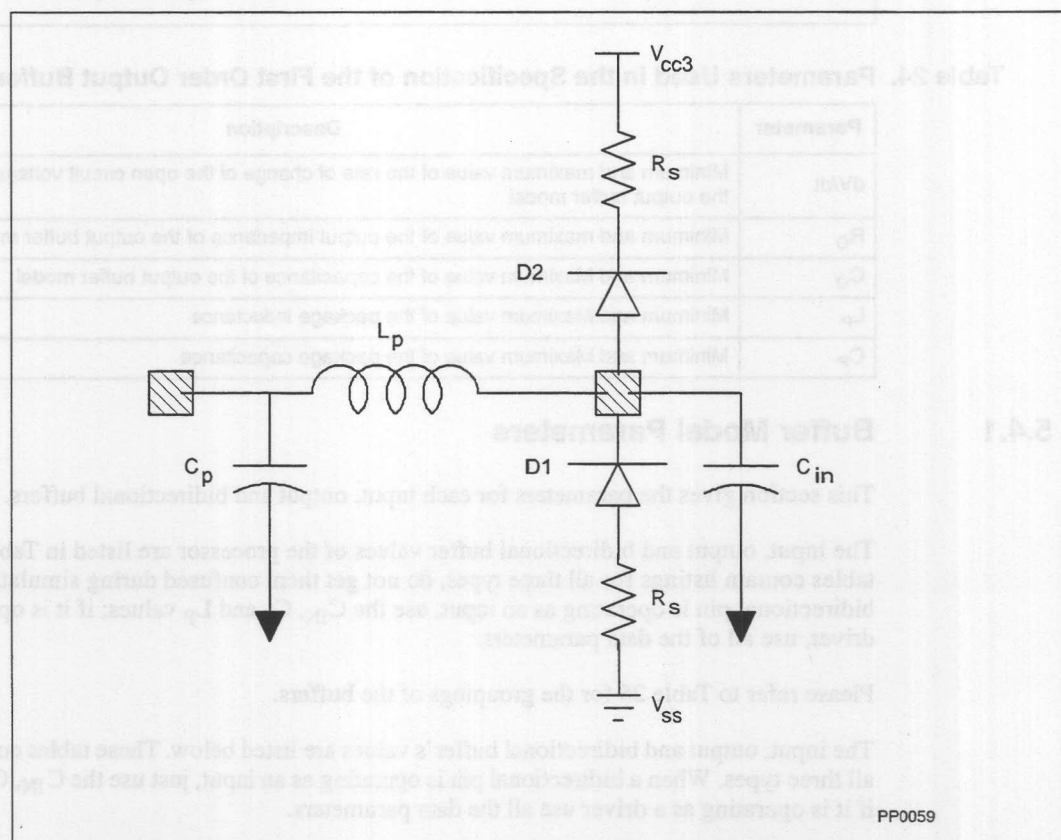


Table 23. Parameters Used in the Specification of the First Order Input Buffer Model

Parameter	Description
$C_{in}$	Minimum and Maximum value of the capacitance of the input buffer model
$L_p$	Minimum and Maximum value of the package inductance
$C_p$	Minimum and Maximum value of the package capacitance
$R_s$	Diode Series Resistance
D1, D2	Ideal Diodes

Figure 16. First Order Output Buffer Model

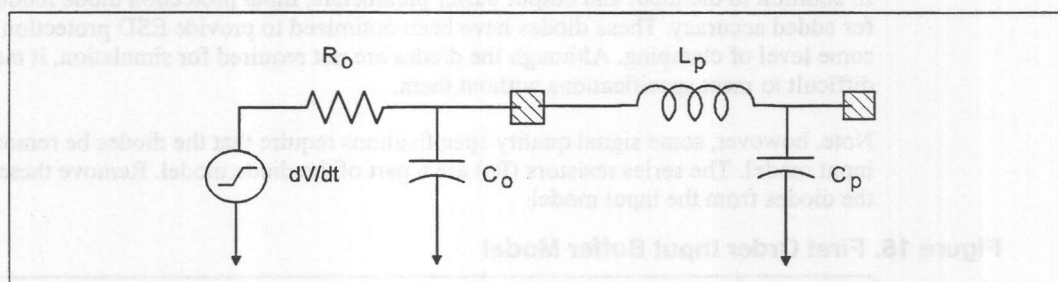


Table 24. Parameters Used in the Specification of the First Order Output Buffer Model

Parameter	Description
dV/dt	Minimum and maximum value of the rate of change of the open circuit voltage source used in the output buffer model
$R_O$	Minimum and maximum value of the output impedance of the output buffer model
$C_O$	Minimum and Maximum value of the capacitance of the output buffer model
$L_P$	Minimum and Maximum value of the package inductance
$C_P$	Minimum and Maximum value of the package capacitance

### 5.4.1 Buffer Model Parameters

This section gives the parameters for each input, output and bidirectional buffers.

The input, output and bidirectional buffer values of the processor are listed in Table 26. These tables contain listings for all three types, do not get them confused during simulation. When a bidirectional pin is operating as an input, use the  $C_{IN}$ ,  $C_P$  and  $L_P$  values; if it is operating as a driver, use all of the data parameters.

Please refer to Table 25 for the groupings of the buffers.

The input, output and bidirectional buffer's values are listed below. These tables contain listings for all three types. When a bidirectional pin is operating as an input, just use the  $C_{IN}$ ,  $C_P$  and  $L_P$  values, if it is operating as a driver use all the data parameters.

**Table 25. Signal to Buffer Type**

Signals	Type	Driver Buffer Type	Receiver Buffer Type
A20M#, AHOLD, BF, BOFF#, BRDY#, BUSCHK#, EADS#, EWBE#, FLUSH#, HOLD, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, PEN#, PICCLK, R/S#, RESET, SMI#, STPCLK#, TCK, TDI, TMS, TRST#, WB/WT#	I		ER1
APCHK#, BE7-BE5#, BP3-BP2, BREQ, FERR#, IERR#, PCD, PCHK#, PM0/BP0, PM1/BP1, PRDY, PWT, SMIACK#, TDO	O	ED1	
A31-A3, AP, BE4#-BE0#, CACHE#, D/C#, D63-D0, DP8-DP0, HLDA, LOCK#, M/IO#, SCYC, ADS#, HITM#, HIT#, W/R#, PICD0, PICD1	I/O	EB1	EB1

**Table 26. Input, Output and Bidirectional Buffer Model Parameters for PPGA Package**

Buffer Type	Transition	dV/dt (V/nsec)		R <sub>O</sub> (Ohms)		C <sub>P</sub> (pF)		L <sub>P</sub> (nH)		C <sub>O</sub> /C <sub>IN</sub> (pF)	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
ER1	Rising					1.1	5.3	7.7	15.3	0.8	1.2
(input)	Falling					1.1	5.3	7.7	15.3	0.8	1.2
ED1	Rising	2.2/2.2	2.7/0.15	21.6	65	1.1	5.8	8.1	16.3	2.0	2.6
(output)	Falling	2.2/2.9	2.7/0.22	17.5	75	1.1	5.8	8.1	16.3	2.0	2.6
EB1	Rising	2.2/2.2	2.7/0.15	21.6	65	1.3	7.0	8.2	18.4	2.0	2.6
(bidir)	Falling	2.2/2.9	2.7/0.22	17.5	75	1.3	7.0	8.2	18.4	2.0	2.6

**Table 27. Preliminary Input, Output and Bidirectional Buffer Model Parameters for HL-PBGA Package**

Buffer Type	Transition	dV/dt (V/nsec)		R <sub>O</sub> (Ohms)		C <sub>P</sub> (pF)		L <sub>P</sub> (nH)		C <sub>O</sub> /C <sub>IN</sub> (pF)	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
ER1	Rising					0.2	0.4	6.4	11.3	0.8	1.2
(input)	Falling					0.2	0.4	6.4	11.3	0.8	1.2
ED1	Rising	2.2/2.2	2.7/0.15	21.6	65	0.2	0.5	5.4	11.7	2.0	2.6
(output)	Falling	2.2/2.9	2.7/0.22	17.5	75	0.2	0.5	5.4	11.7	2.0	2.6
EB1	Rising	2.2/2.2	2.7/0.15	21.6	65	0.2	0.4	5.2	10.3	2.0	2.6
(bidir)	Falling	2.2/2.9	2.7/0.22	17.5	75	0.2	0.4	5.2	10.3	2.0	2.6

**NOTE:** The data in this table is based on preliminary design information. Input, output and bidirectional buffer values are being characterized at this time.



Table 28. Input Buffer Model Parameters: D (Diodes)

Symbol	Parameter	D1	D2
$I_S$	Saturation Current	1.4e-14A	2.78e-16A
N	Emission Coefficient	1.19	1.00
$R_S$	Series Resistance	6.5 $\Omega$	6.5 $\Omega$
$T_T$	Transit Time	3 ns	6 ns
$V_J$	PN Potential	0.983 V	0.967 V
$C_{J0}$	Zero Bias PN Capacitance	0.281 pF	0.365 pF
M	PN Grading Coefficient	0.385	0.376

## 5.5 Signal Quality Specifications

Signals driven by the system into the low-power embedded Pentium processor with MMX technology must meet signal quality specifications to guarantee that the components read data properly and to ensure that incoming signals do not affect the reliability of the component.

### 5.5.1 Overshoot

The maximum overshoot and overshoot threshold duration specifications for inputs to the low-power embedded Pentium processor with MMX technology are described as follows:

- Maximum overshoot specification: The maximum overshoot of the CLK/PICCLK signals should not exceed  $V_{CC2}$ , nominal +0.6 V. The maximum overshoot of all other input signals should not exceed  $V_{CC3}$ , nominal +1.0 V.
- Overshoot threshold duration specification: The overshoot threshold duration is defined as the sum of all time during which the input signal is above  $V_{CC3}$ , nominal +0.3 V, within a single clock period. The overshoot threshold duration must not exceed 20% of the period.

Refer to Table 29 for a summary of the overshoot specifications for the low-power embedded Pentium processor with MMX technology.

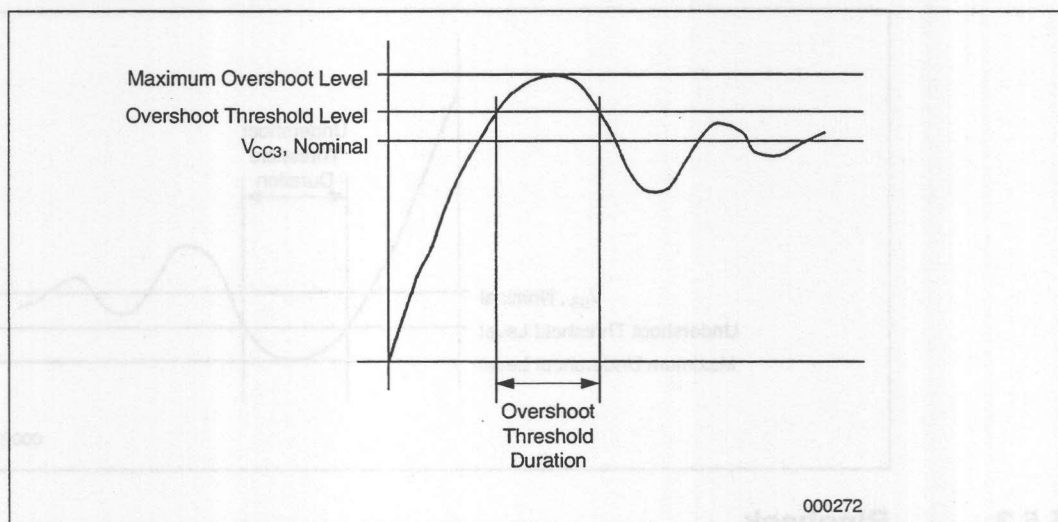
Table 29. Overshoot Specification Summary

Specification Name	Value	Units	Notes
Threshold Level	$V_{CC3}$ , nominal +0.3	V	(1, 2)
Maximum Overshoot Level (CLK and PICCLK)	$V_{CC3}$ , nominal +0.6	V	(1, 2)
Maximum Overshoot Level (all other inputs)	$V_{CC3}$ , nominal +1.0	V	(1, 2)
Maximum Threshold Duration	20% of clock period above threshold voltage	ns	(2)
Maximum Ringback	$V_{CC3}$ , nominal -0.7	V	(1, 2)

#### NOTES:

1.  $V_{CC3}$ , nominal refers to the voltage measured at the  $V_{CC3}$  pins. See "Measurement Methodology" on page 54 for details.
2. See Figure 17 and Figure 19.

Figure 17. Maximum Overshoot Level, Overshoot Threshold Level and Overshoot Threshold Duration



### 5.5.2 Undershoot

The maximum undershoot and undershoot threshold duration specifications for inputs to the low-power embedded Pentium processor with MMX technology are described as follows:

- **Maximum undershoot specification:** The maximum undershoot of the CLK/PICCLK signals must not drop below  $-0.6$  V. The maximum undershoot of all other input signals must not drop below  $-1.0$  V.
- **Undershoot threshold duration specification:** The undershoot threshold duration is defined as the sum of all time during which the input signal is below  $-0.3$  V within a single clock period. The undershoot threshold duration must not exceed 20% of the period.

Refer to Table 30 for a summary of the undershoot specifications for the low-power embedded Pentium processor with MMX technology.

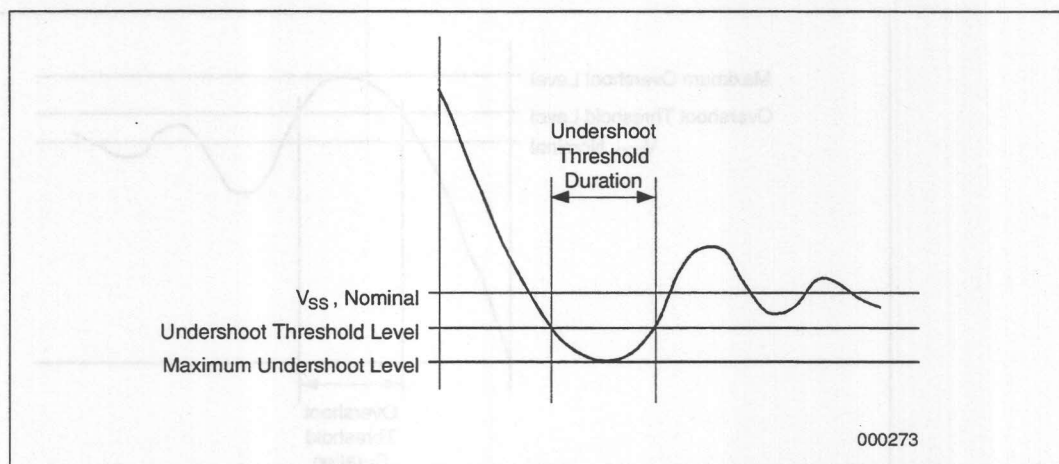
Table 30. Undershoot Specification Summary

Specification Name	Value	Units	Notes
Threshold Level	$-0.3$	V	(1)
Minimum Undershoot Level (CLK and PICCLK)	$-0.6$	V	(1)
Minimum Undershoot Level (all other inputs)	$-1.0$	V	(1)
Maximum Threshold Duration	20% of clock period below threshold voltage	ns	(1)
Maximum Ringback	0.5	V	(1)

**NOTE:**

1. See Figure 18 and Figure 20.

Figure 18. Maximum Undershoot Level, Undershoot Threshold Level and Undershoot Threshold Duration



### 5.5.3 Ringback

Excessive ringback can contribute to long-term reliability degradation of the low-power embedded Pentium processor with MMX technology, and can cause false signal detection. Ringback is simulated at the input pin of a component using the input buffer model. Ringback can be simulated with or without the diodes that are in the input buffer model.

Ringback is the absolute value of the maximum voltage at the receiving pin below  $V_{CC3}$  (or above  $V_{SS}$ ) relative to the  $V_{CC3}$  (or  $V_{SS}$ ) level after the signal has reached its maximum voltage level. The input diodes are assumed present.

If simulated without the input diodes, follow the Maximum Overshoot/Undershoot specifications. By meeting the overshoot/undershoot specifications, the signal is guaranteed not to ringback excessively.

If simulated with the diodes present in the input model, follow the maximum ringback specification. The maximum ringback specification for inputs to the low-power embedded Pentium processor with MMX technology is described as follows:

- Maximum ringback specification: The maximum ringback of inputs associated with their high states (overshoot) must not drop below  $V_{CC3} - 1.0$  V as shown in Figure 19. Similarly, the maximum ringback of inputs associated with their low states (undershoot) must not exceed 0.5 V as shown in Figure 20.
- Overshoot (undershoot) is the absolute value of the maximum voltage above  $V_{CC}$  (below  $V_{SS}$ ). The guideline assumes the absence of diodes on the input.



Figure 19. Maximum Ringback Associated with the Signal High State

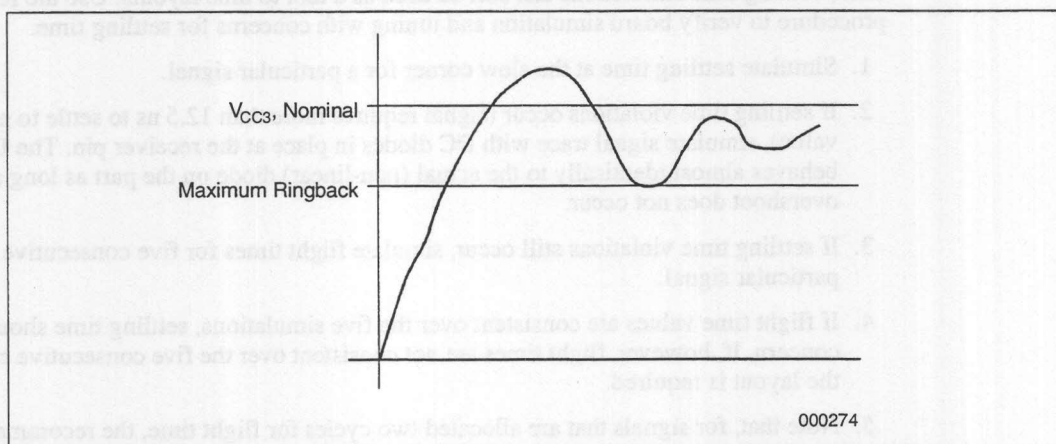
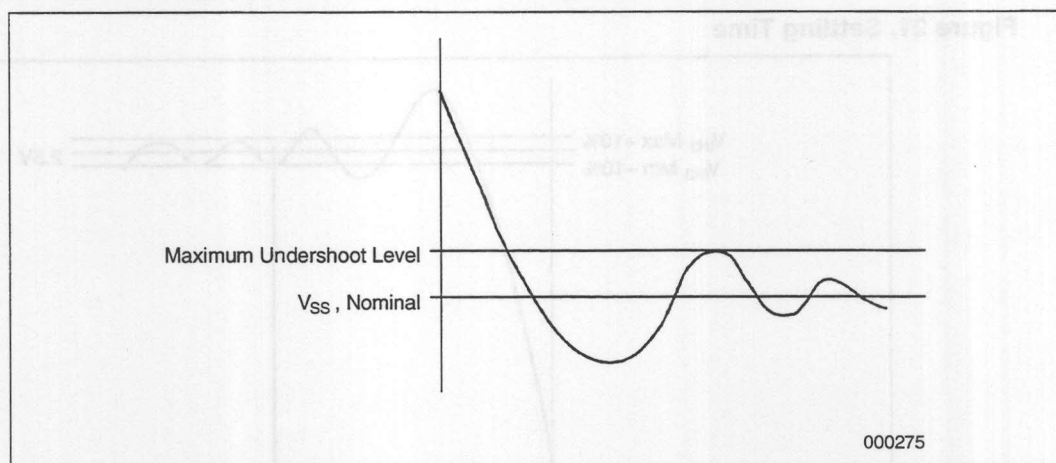


Figure 20. Maximum Ringback Associated with the Signal Low State



#### 5.5.4 Settling Time

The settling time is defined as the time a signal requires the receiver to settle within 10 percent of  $V_{CC3}$  or  $V_{SS}$ . Settling time is the maximum time allowed for a signal to reach within 10 percent of its final value.

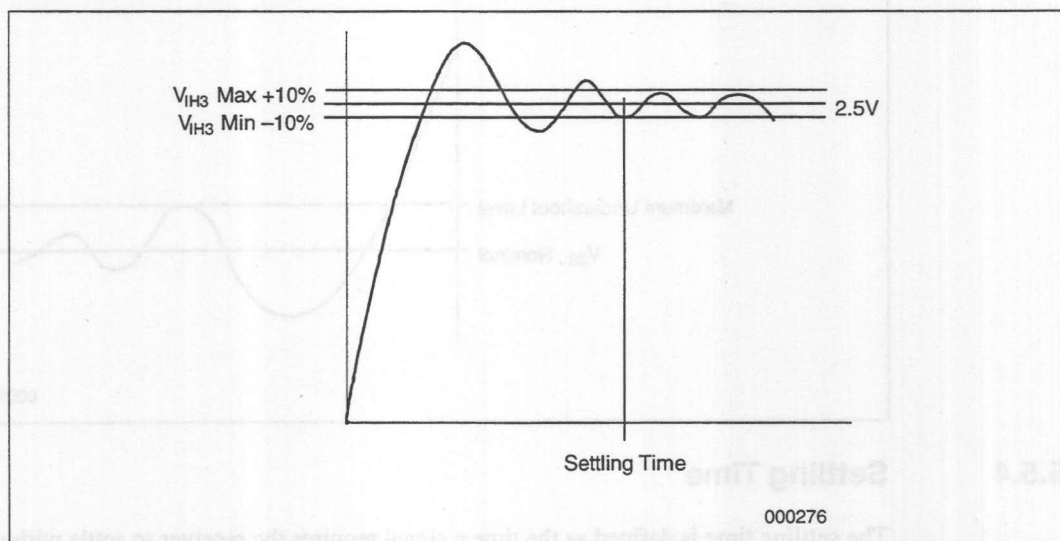
Most available simulation tools are unable to simulate settling time so that it accurately reflects silicon measurements. Second order, and other, effects on a physical board serve to dampen the signal at the receiver. Because of these concerns, settling time is a recommendation or a tool for layout tuning and not a specification.

To make sure that there is no impact on the flight times of the signals if the waveform has not settled, settling time is simulated at the slow corner. Settling time may be simulated with the diodes included or excluded from the input buffer model. If diodes are included, settling time recommendations will be easier to meet.

Although simulated settling time has not shown good correlation with physical, measured settling time, settling time simulations can still be used as a tool to tune layouts. Use the following procedure to verify board simulation and tuning with concerns for settling time:

1. Simulate settling time at the slow corner for a particular signal.
2. If settling time violations occur (signal requires more than 12.5 ns to settle to  $\pm 10\%$  of its final value), simulate signal trace with DC diodes in place at the receiver pin. The DC diode behaves almost identically to the actual (non-linear) diode on the part as long as excessive overshoot does not occur.
3. If settling time violations still occur, simulate flight times for five consecutive cycles for that particular signal.
4. If flight time values are consistent over the five simulations, settling time should not be a concern. If, however, flight times are not consistent over the five consecutive cycles, tuning of the layout is required.
5. Note that, for signals that are allocated two cycles for flight time, the recommended settling time is doubled. Maximum Settling Time to within 10 percent of  $V_{IH}$  or  $V_{IL}$  is 12.5 ns at 66 MHz.

Figure 21. Settling Time



### 5.5.5 Measurement Methodology

The waveform of the input signals should be measured at the processor pins using an oscilloscope with a 3 dB bandwidth of at least 20 MHz (100 ms/s digital sampling rate). There should be a short isolation ground lead attached to a processor pin on the bottom side of the board. A 1-M $\Omega$  probe with loading of less than 1 pF is recommended. The measurement should be taken at the input pins and their nearest  $V_{SS}$  pins.

## 5.6 Measuring Maximum Overshoot, Undershoot and Ringback

The display should show continuous sampling (e.g., infinite persistence) of the waveform at 500 mV/div and 5 ns/div (for CLK) or 20 ns/div (for other inputs) for a recommended duration of approximately five seconds. Adjust the vertical position to measure the maximum overshoot and associated ringback with the largest possible granularity. Similarly, readjust the vertical position to measure the maximum undershoot and associated ringback. There is no allowance for crossing the maximum overshoot, maximum undershoot or maximum ringback specifications.

## 5.7 Measuring Overshoot Threshold Duration

A snapshot of the input signal should be taken at 500 mV/div and 500 ps/div (for CLK) or 2 ns/div (for other inputs). Adjust the vertical position and horizontal offset position to view the threshold duration. The overshoot threshold duration is defined as the sum of all time during which the input signal is above  $V_{CC3}$  nominal + 0.3 V within a single clock period. The overshoot threshold duration must not exceed 20% of the period.

## 5.8 Measuring Undershoot Threshold Duration

A snapshot of the input signal should be taken at 500 mV/div and 500 ps/div (for CLK) or 2 ns/div (for other inputs). Adjust the vertical position and horizontal offset position to view the threshold duration. The undershoot threshold duration is defined as the sum of all time during which the clock signal is below -0.3 V within a single clock period. The undershoot threshold duration must not exceed 20% of the period.



## 6.0 Mechanical Specifications

In mechanical terms, the low-power embedded Pentium processor with MMX technology 296-lead Plastic Staggered Pin Grid Array (PPGA) is completely identical to the Pentium processor with MMX technology PPGA package. The pins are arranged in a 37x37 matrix and the package dimensions are 1.95" x 1.95" (4.95 cm x 4.95 cm). Package summary information for the PPGA device is provided in Table 31. Figure 22 shows the package dimensions.

The HL-PBGA version of the low-power embedded Pentium processor with MMX technology is a new package type for the Pentium processor family. Package summary information for the HL-PBGA device is provided in Table 32. Figure 23 shows the package dimensions.

### 6.1 PPGA Package Mechanical Diagrams

Figure 22. PPGA Package Dimensions

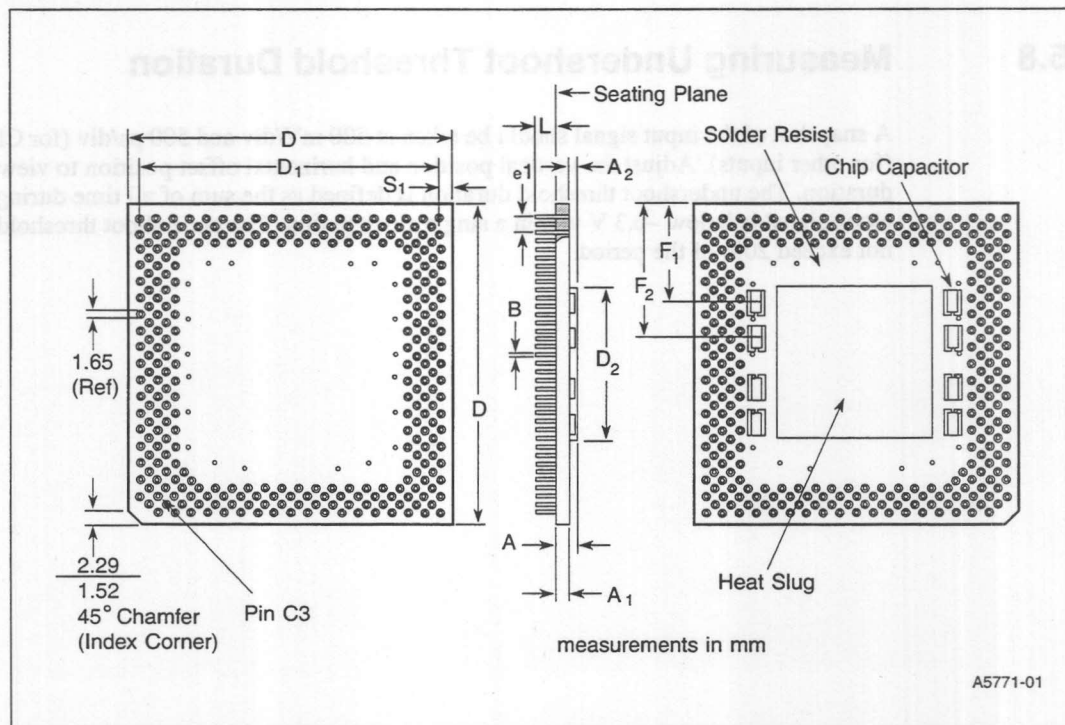




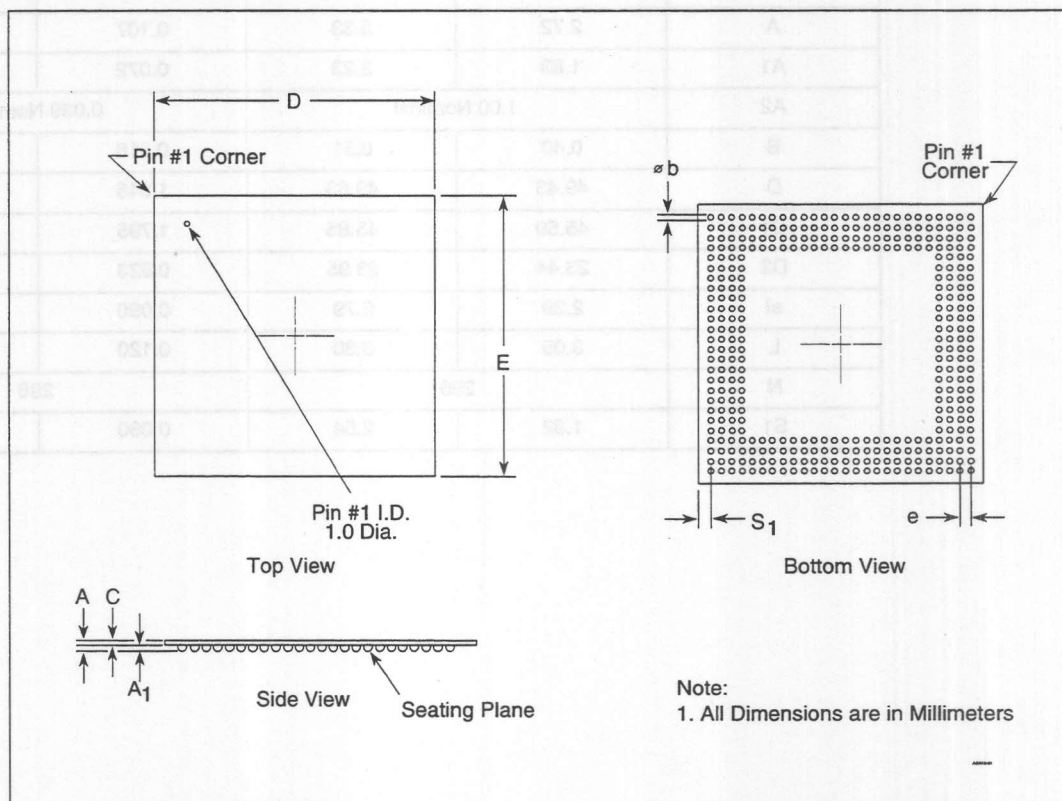
Table 31. PPGA Package Dimensions

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.72	3.33	0.107	0.131
A1	1.83	2.23	0.072	0.088
A2	1.00 Nominal		0.039 Nominal	
B	0.40	0.51	0.016	0.020
D	49.43	49.63	1.946	1.954
D1	45.59	45.85	1.795	1.805
D2	23.44	23.95	0.923	0.943
el	2.29	2.79	0.090	0.110
L	3.05	3.30	0.120	0.130
N	296		296	
S1	1.52	2.54	0.060	0.100

## 6.2 HL-PBGA Package Mechanical Diagrams

Figure 23 shows the ceramic HL-PBGA package. The dimensions are listed in Table 32.

**Figure 23. HL-PBGA Package Dimensions**



**Table 32. HL-PBGA Package Dimensions**

Symbol	Millimeters	
	Min	Max
A	1.41	1.67
A <sub>1</sub>	0.56	0.70
b	0.60	0.90
c	0.85	0.97
D	34.90	35.10
E	34.90	35.10
e	1.27	
S <sub>1</sub>	1.63 REF	



## 7.0 Thermal Specifications

The low-power embedded Pentium processor with MMX technology is specified for proper operation when case temperature,  $T_{CASE}$  ( $T_C$ ), is within the specified range of 0°C to 85°C for the PPGA package, and 0°C to 95°C for the HL-PBGA package.

### 7.1 Measuring Thermal Values

To verify that the proper  $T_C$  is maintained, it should be measured at the center of the package top surface (opposite of the pins). The measurement is made in the same way with or without a heatsink attached. When a heatsink is attached, a hole (smaller than 0.150" diameter) should be drilled through the heatsink to allow probing the center of the package. See Figure 24 for an illustration of how to measure  $T_C$ .

To minimize the measurement errors, it is recommended to use the following approach:

- Use 36-gauge or finer diameter K, T, or J type thermocouples. The laboratory testing was done using a thermocouple made by Omega\* (part number 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the package top surface using high thermal conductivity cements. The laboratory testing was done by using Omega Bond (part number OB-101).
- The thermocouple should be attached at a 90-degree angle as shown in Figure 24.
- The hole size should be smaller than 0.150" in diameter.
- Make sure there is no contact between thermocouple cement and heatsink base. The contact will affect the thermocouple reading.

#### 7.1.1 Thermal Equations and Data

For the low-power embedded Pentium processor with MMX technology, an ambient temperature,  $T_A$  (air temperature around the processor), is not specified directly. The only restriction is that  $T_C$  is met.

The equation used to calculate  $\theta_{CA}$  is:

$$\theta_{CA} = \frac{T_C - T_A}{P}$$

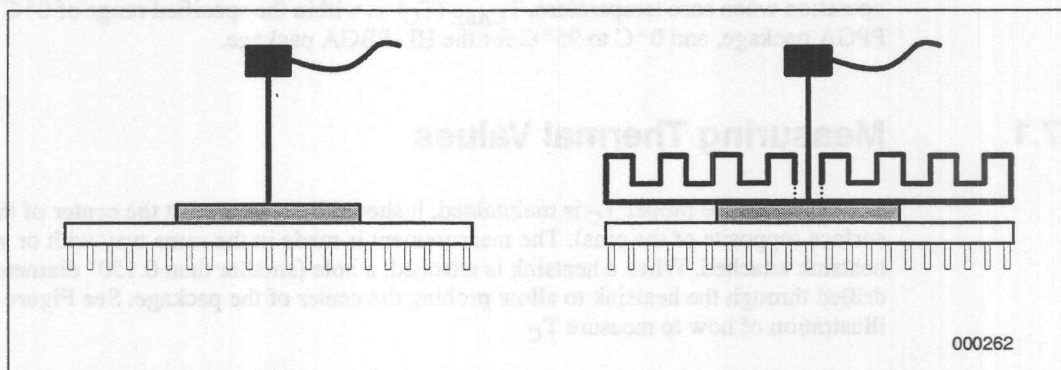
Where:

- |                 |   |  |
|-----------------|---|--|
| $T_A$ and $T_C$ | = | Ambient and case temperature (°C)            |
| $\theta_{CA}$   | = | Case-to-ambient thermal resistance (°C/Watt) |
| $P$             | = | Maximum power consumption (Watt)             |

$\theta_{JC}$  is thermal resistance from die to package case.  $\theta_{JC}$  values shown in Tables 33 and 34 are typical values. The actual  $\theta_{JC}$  values depend on actual thermal conductivity and process of die attach.  $\theta_{CA}$  is thermal resistance from package case to the ambient.  $\theta_{CA}$  values shown in these

tables are typical values. The actual  $\theta_{CA}$  values depend on the heatsink design, interface between heatsink and package, airflow in the system, and thermal interactions between processor and surrounding components through PCB and the ambient.

**Figure 24. Technique for Measuring  $T_C$**



### 7.1.2 Airflow Calculations for Maximum and Typical Power

Below is an example of determining the airflow required during maximum power consumption for the 166 MHz low-power embedded Pentium processor with MMX technology assuming an ambient air temperature of 50° C:

$$T_C (\text{HL-PBGA}) = 95^\circ \text{ C}$$

$$T_A = 50^\circ \text{ C}$$

$$P_{\text{HL-PBGA}} = 4.1 \text{ W}$$

$$\theta_{CA} (\text{HL-PBGA, without heat sink}) = 10.98^\circ \text{ C/W}$$

Figure 26 indicates that this example would require about 175 LFM without a heat sink, and about 25 LFM with a heat sink in the vertical orientation.

Below is an example of determining the airflow required during typical power consumption for the 166 MHz low-power embedded Pentium processor with MMX technology assuming an ambient air temperature of 50° C:

$$T_C (\text{HL-PBGA}) = 95^\circ \text{ C}$$

$$T_A = 50^\circ \text{ C}$$

$$P_{\text{HL-PBGA}} = 2.9 \text{ W}$$

$$\theta_{CA} (\text{HL-PBGA, without heat sink}) = 15.52^\circ \text{ C/W}$$

Figure 26 indicates that this example would require about 0 LFM without a heat sink. A heat sink may not be necessary for typical power and 50° C ambient conditions.

## 7.2 PPGA Package Thermal Resistance Information

Table 33 lists the  $\theta_{JC}$  and  $\theta_{CA}$  values for the low-power embedded Pentium processor with MMX technology in the PPGA package with passive heatsinks.

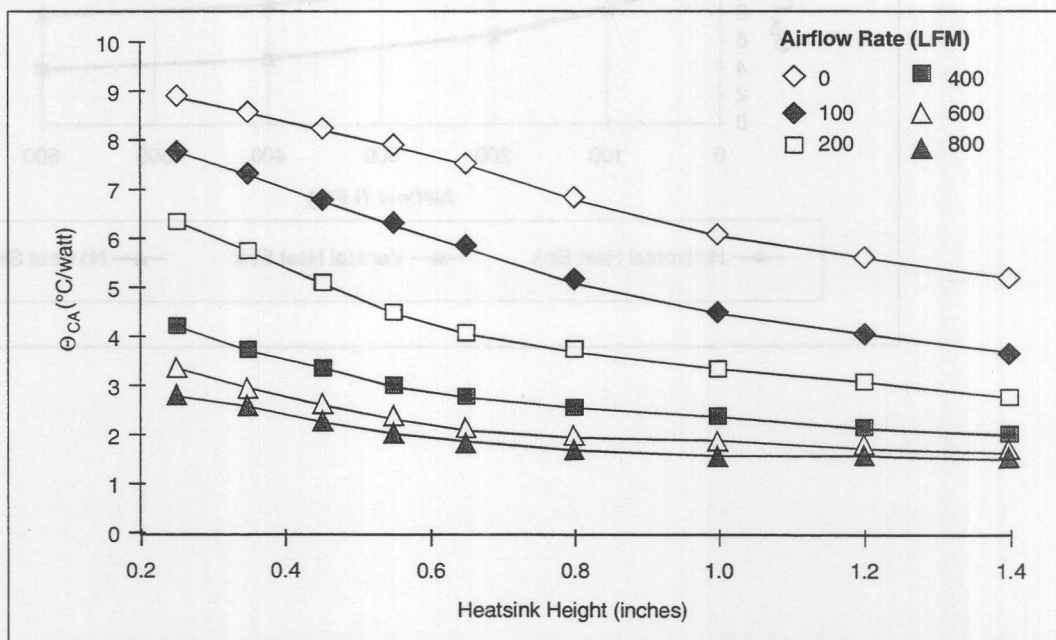
Table 33. Thermal Resistances for PPGA Packages

Heatsink Height	$\theta_{JC}$	$\theta_{CA}$ (°C/watt) vs. Laminar Airflow (linear ft/min)					
(inches)	(°C/watt)	0	100	200	400	600	800
0.25	0.5	8.9	7.8	6.4	4.3	3.4	2.8
0.35	0.5	8.6	7.3	5.8	3.8	3.1	2.6
0.45	0.5	8.2	6.8	5.1	3.4	2.7	2.3
0.55	0.5	7.9	6.3	4.5	3.0	2.4	2.1
0.65	0.5	7.5	5.8	4.1	2.8	2.2	1.9
0.80	0.5	6.8	5.1	3.7	2.6	2.0	1.8
1.00	0.5	6.1	4.5	3.4	2.4	1.9	1.6
1.20	0.5	5.7	4.1	3.1	2.2	1.8	1.6
1.40	0.5	5.2	3.7	2.8	2.0	1.7	1.5
None	1.3	12.9	12.2	11.2	7.7	6.3	5.4

**NOTES:**

1. Heatsinks are omni-directional pin aluminum alloy.
2. Features were based on standard extrusion practices for a given height: pin size ranged from 50 to 129 mils; pin spacing ranged from 93 to 175 mils; base thickness ranged from 79 to 200 mils.
3. Heatsink attach was 0.005" of thermal grease. Attach thickness of 0.002" will improve performance by approximately 0.3 watt.

Figure 25. Thermal Resistance vs. Heatsink Height, PPGA Packages





### 7.3 HL-PBGA Package Thermal Resistance Information

Table 34 lists the  $\theta_{JC}$  values for the low-power embedded Pentium processor with MMX technology in the HL-PBGA package.

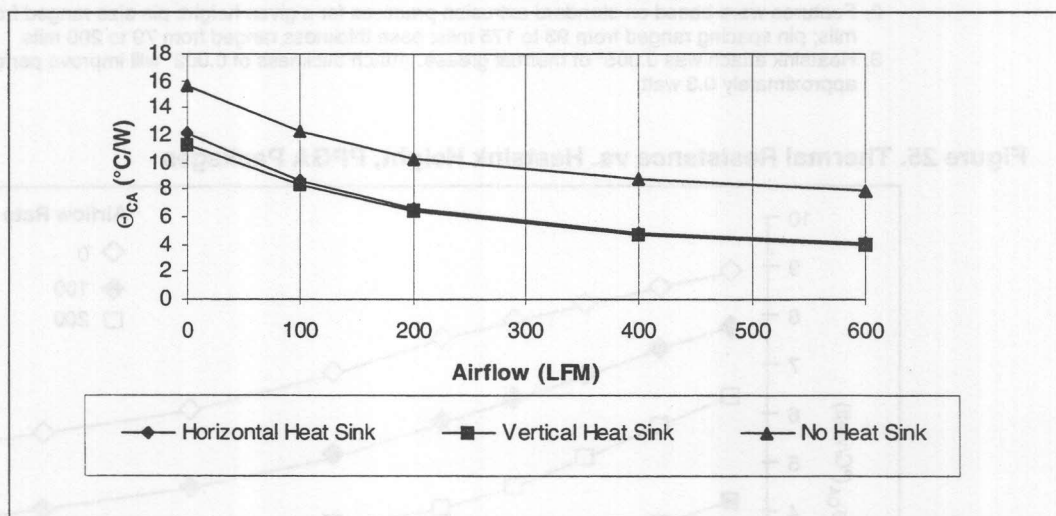
The thermal data collection conditions were:

- A bidirectional anodized aluminum alloy heat sink was used.
- Heat sink height was 7mm.
- In the horizontal orientation the component was mounted flush with the motherboard.
- In the vertical orientation the component was mounted on an add-in card perpendicular to the motherboard.

**Table 34. Thermal Resistances for HL-PBGA Packages**

Heatsink/ Orientation	$\theta_{JC}$ (°C/watt)	$\theta_{CA}$ (°C/watt) vs. Laminar Airflow (linear ft/min)				
		0	100	200	400	600
No Heat Sink	0.76	15.66	12.33	10.3	8.85	7.89
Horizontal	0.76	12.09	8.57	6.52	4.82	4.06
Vertical	0.76	11.33	8.34	6.38	4.69	3.95

**Figure 26. Thermal Resistance vs. Airflow for HL-PBGA Package**



**Low Voltage Embedded Design  
Application Note**





# **Low Voltage Embedded Design**

**JOHN WILLIAMS  
APPLICATIONS ENGINEER**

February 1993



Order Number: 272324-001



## Low Voltage Embedded Design

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# Low Voltage Embedded Design

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## 1.0 INTRODUCTION

Currently, integrated circuit manufacturers are specifying devices for low voltage operation. Most devices are specified for operation around 3V. This can indicate operation centered around 3.0V, 3.3V or other voltages. Many devices are even specified for operation at 2V and below.

In many embedded designs, the designer wants the lowest system power dissipation possible. Embedded, low voltage designs require maximum battery life which is directly proportional to the current consumption of the system. System current consumption is a linear function of operating voltage.

This application note discusses why low voltage devices and systems are beneficial and how to design low voltage systems. Power supplies, mixed voltage systems, single voltage systems and power management schemes are all discussed. Although 3V systems are specifically discussed, the concepts apply to all low voltage designs.

### 1.1 What is 3V?

The term "3V" usually refers to  $3.3V \pm 0.3V$ . This is the JEDEC standard for regulated supplies. The majority of devices are specified for 3.3V operation, the standard being used for portable PC's. JEDEC Standard 8 defines LVC MOS (Low Voltage CMOS) operating voltages and interface levels for low voltages. JEDEC Standard 8.1 defines LVTTL (Low Voltage TTL) compatibility. The LVTTL standard defines specifications for low voltage devices that operate in 5V TTL systems without interface logic.

There is also a standard for unregulated supplies, 2.7V to 3.6V (battery operated systems). Few devices are currently specified for operation in the unregulated region. Many devices used in embedded applications have a wider  $V_{CC}$  range and do not conform to this standard. A  $V_{CC}$  specification from 2.7V to 5.5V allows operation from an unregulated alkaline battery supply (3 x AA). Older 5V devices derated for 3V operation (specified for 3V operation at a reduced frequency) typically can operate in this region.

## 2.0 REASONS FOR 3V OPERATION

Components are being specified to operate at 3V for two reasons. First, advanced fabrication technologies incorporating smaller device geometries require lower operating voltages. Second, there are a number of advantages to operating a system at low voltage.

### 2.1 Device Geometries

One of the driving factors to reduce component operating voltages is technology. As device channel lengths and oxide thicknesses decrease (Figure 2-1), lower operating voltages are required to maintain component reliability. Three main reliability concerns are: oxide breakdown, punch-through, and hot-electron effects.

As feature length and width in a component decrease, depth also decreases. With thinner gate oxides, lower gate voltages are required to avoid dielectric breakdown in the oxide. If oxide breakdown occurs, the gate of the device begins to draw current.

As the channel lengths shorten, lower source and drain voltages are required to keep the depletion regions around the wells from meeting, at this point, the current through the device is no longer controlled by the voltage on the gate.

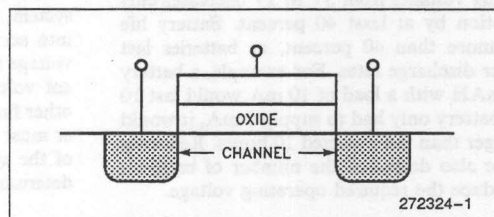


Figure 2-1. Basic Transistor Structure

Finally, lower voltages are required to avoid hot-electron effects. Electrons can lodge in the gate oxide, altering the charge in the oxide. When charge is added to the gate oxide, the turn-on voltage of the device is altered, degrading performance.

### 2.2 System Benefits

Presently, not all devices are being designed to operate specifically at low voltages. Many devices are 5V designs with their performance derated for low voltage operation. These devices are only rated for low voltage operation because of the benefits it has for system designs. Operating parts at lower voltages has some significant advantages at a system level.

Battery powered systems operate significantly longer at 3V. Battery life, rated in Amp-hours, is a function of the current a system draws. The current consumption of a system varies linearly with the operating voltages of the devices. Equation 2.1 expresses this relationship.

$$\text{Equation 2.1: } I_{CC} = C \int V \cdot dt \approx \Delta V \cdot C \cdot F$$

where

- $I_{CC}$  = Device current consumption
- $\Delta V$  = Switching voltage
- $C$  = Device capacitance and output capacitive loading
- $F$  = Device operating frequency

Determining the current consumption of an entire system is not quite this straightforward, but this topic will be examined in more detail later. The point is, lowering device operating voltages from 5V to 3V decreases current consumption by at least 40 percent. Battery life increases by more than 40 percent, as batteries last longer at lower discharge rates. For example, a battery rated at 100 mAH with a load of 10 mA would last 10 hours. If the battery only had to supply 5 mA, it would have a life longer than the expected 20 hours. Reducing system voltage also decreases the number of batteries needed to produce the required operating voltage.

Heat generated by a device is proportional to the power it consumes. The formula for power consumption of a device is the current (Equation 1) multiplied by the operating voltage (V). Power consumption varies as the square of the operating voltage. Reducing the operating voltage of a device from 5V to 3V decreases power consumption by 64 percent. Heat dissipation is reduced by the same amount. This has a couple of important implications. On a device level, parts that generate less heat do not have as many constraints placed on packaging. Packages with much smaller footprints can be created and plastic packages can be offered for devices previously only offered in ceramic packages. On a system level, if parts produce less heat, they can be placed closer together. These advantages allow reduction of the overall form factor and weight of a system. Additionally, many device failure mechanisms are heat related. Systems producing less heat have higher reliability.

Noise generated by devices is a concern for all system designers. The effects of noise: overshoot, undershoot, ground bounce, etc., are a function of  $dV/dt$ . On low voltage devices,  $dV/dt$  is lower. This is discussed in more detail in a later section. Decreased noise generation by low voltage systems simplifies design and makes meeting maximum noise limits easier.

The move to lower operating voltages has a number of benefits to the system designer. Smaller, lighter, less noisy systems and longer battery life all contribute to better designs. Low voltage designs also enable older designs to become mobile/portable.

### 3.0 LOW VOLTAGE SYSTEM DESIGN

Low voltage systems have many aspects in common with standard 5V designs. In addition to the normal design considerations made in any 5V system, low voltage designs have some areas that need specific attention. System power supply, mixed voltage interfaces, and complete low voltage designs all need to be considered.

#### 3.1 Power Supply Design

When designing the power supply for a low voltage system, the characteristics of that system must be taken into account. A supply must exist for each operating voltage on a board. This could mean a number of different voltages for logic, communications, displays, and other functions. For each voltage generated, the designer must determine the worst-case current consumption of the system. Number of supplies and their capacity determine the power supply design.

##### 3.1.1 BATTERIES

A major application of low voltage devices in embedded systems is in portable systems that require battery operation. The type of battery the designer chooses affects the power supply design. Batteries are characterized by two general discharge curves. Alkaline batteries have a constantly decreasing voltage output (Figure 3-1a). Ni-Cad batteries (as well as Nickel-Hydride, Lithium and others) have a relatively constant voltage through the majority of their life (Figure 3-1b). Internal chemical reactions and the number of cells inside each battery determine the output voltage.

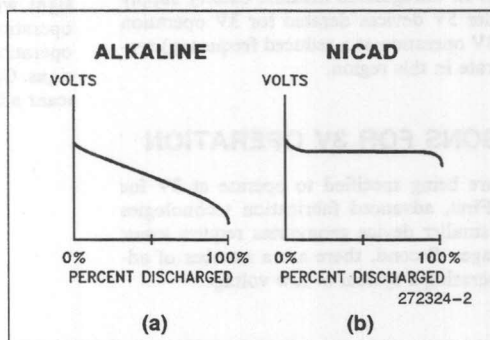


Figure 3-1. Typical Battery Discharge Curves



The battery discharge curve and voltage requirements of the system components determine whether voltage regulation is required. A system utilizing components with narrow voltage specifications ( $3.3V \pm 10\%$ , for example) using Alkaline batteries, would require a voltage regulator to translate the battery output voltage to something usable by the system. NiCad batteries, on the other hand, provide a stable enough voltage over their lifetime that the designer could avoid using a regulator.

Although the constant voltage type of batteries may appear to be the most efficient choice, a number of other tradeoffs exist such as overall capacity, rechargeability, temperature sensitivity, safety, volume, weight and cost. When deciding on a battery, these characteristics, or combinations of these characteristics should be considered. For example, an application may require maximum capacity, but minimum weight, so capacity per unit weight may be the most important combination. Also, rechargeability may or may not be important to the design. Secondary batteries, such as NiCad may be recharged, while primary batteries such as alkaline may not.

### 3.1.2 VOLTAGE REGULATION

Voltage regulators may be required in systems where battery output voltage and system  $V_{CC}$  requirements do not match. For example, three Alkaline AA batteries would discharge from about 4.5V to about 2.7V over their lifetime. A device specified for operation from 3V to 3.6V would require this supply to be regulated. Voltage regulated systems have the advantage of having a stable, constant  $V_{CC}$  for the life of the batteries. The disadvantages include extra board space needed for the regulator(s) and decreased battery life due to regulator efficiency losses. Most regulator efficiencies run from the mid-80 percent to low-90 percent range.

In low power designs, voltage regulation is usually performed with pulse-skipping regulators, current-mode pulse width modulators (PWM's) or voltage-mode PWM's. Each of these methods has certain advantages and disadvantages. Important regulator characteristics include output ripple amplitude and frequency, efficiency, quiescent current, transient response and physical size requirements. Individual designs will have different requirements, and these issues should be considered when designing the system power supply.

### 3.1.3 CALCULATING SYSTEM POWER CONSUMPTION

When designing a system power supply, it is important to understand system current requirements. Knowing the worst-case current consumption allows the designer to choose the voltage regulation method, estimate system battery life and determine system packaging requirements (heat dissipation, etc.).

Many factors determine total system current. Device current, discrete component current, and leakage current are all factors. The general formula for current consumption,  $I$  is:

$$\text{Equation 3.1: } I = V \cdot C \cdot f = C \cdot dV/dt$$

Where:  $V$  = voltage,  $C$  = capacitance, and  $f$  = frequency. This formula must be used for all components in the system to estimate current consumption. The term "estimate" is used because, until the design is completed, fabricated, and tested, there is no way to know the exact current consumption. Actual current will depend on the way the software controls the hardware in the system, temperature and other factors. To estimate current consumption, some assumptions are required to keep the calculations from becoming too detailed. The various contributors to system current consumption are detailed in the following sections.

#### 3.1.3.1 Device Current

There are two parts to device current consumption: core current and I/O current. Core current is typically a large percentage of the total device current. I/O current is a smaller percentage, but still a major contributor to total system current.

Core current is the current consumed by internal transistors switching and the charging and discharging of internal capacitances. In this situation,  $V$  in Equation 3.1 is equal to  $V_{CC}$ . All of the internal nodes switch between  $V_{CC}$  and ground. The frequency term is the device operating frequency. The Capacitance term, slightly more complicated, is an equivalent capacitance accounting for all internal node and trace capacitances. To determine this value,  $I_{CC}$  is measured at a known frequency and voltage with output pins inactive, Equation 3.2 is then solved for the equivalent capacitance (Equation 3.3). This value applies to all operating frequencies.

$$\text{Equation 3.2: } I_{core} = V_{CC} \cdot C_{eq} \cdot f$$

$$\text{Equation 3.3: } C_{eq} = I_{core} / (V_{CC} \cdot f)$$

I/O current is the current consumed by outputs switching. To determine I/O current,  $V$  in Equation 1 is the voltage swing of the output,  $V_{CC}$  in a normal, CMOS system. The capacitance term is the sum of all input capacitances of devices connected to the output plus the capacitance of the PCB trace (approximately 2 pF/in.). The frequency term is the switching frequency of the output, not necessarily the operating frequency of the system. The frequency term can be determined by approximating how often an output switches during a particular time period. The measure of time in an embedded system is typically a processor bus cycle. Using the 80C186 embedded processor as an example, the major contributors to I/O current are the Address/Data bus, RD#, WR# and ALE outputs. Depending on the application, other outputs may switch frequently enough to be included in current calculations. These signals are used as a simple example.

Because of the multiplexed Address/Data bus on the 186 device, data is written and read on the same pins that drive address information. Thus, read and write cycles need to be treated separately. An analysis of bus cycles for a typical application indicates that about 80 percent are read cycles (data reads and instruction fetches) and the remaining 20 percent are write cycles. Equation 3.4 represents the Address/Data bus current for a write cycle.

$$\text{Equation 3.4: } I_{\text{write}} = (V \cdot C \cdot f) \cdot (1/n) \cdot (x + y)$$

where:

- $V = V_{CC}$
- $C =$  Load capacitance per pin
- $f =$  Processor operating frequency
- $n =$  Number of clocks per bus cycle (4 at zero wait states)
- $x =$  Number of pins switching during the address phase
- $y =$  Number of pins switching during the data phase

Because of the random nature of data being read/written, it is a reasonable assumption that approximately half of the Address/Data pins will switch during each phase of the bus cycle (address and data). For a read cycle, the equation will be identical, with  $y = 0$ , as shown in Equation 3.5.

$$\text{Equation 3.5: } I_{\text{read}} = (V \cdot C \cdot f) \cdot (1/n) \cdot (x)$$

The control signals: RD#, WR# and ALE are driven during each bus cycle. Equation 3.6 shows the current for the combined control signals. Each of these signals switch twice during a bus cycle, once to go active and once to go inactive or vice-versa.

$$\text{Equation 3.6: } I_{\text{control}} = (V \cdot C \cdot f) \cdot (1/n) \cdot (x)$$

- $V = V_{CC}$
- $C =$  Load capacitance on the control signal pin
- $f =$  Processor operating frequency
- $n =$  Number of clocks per bus cycle (4 at zero wait states)
- $x =$  Number of times the control signal switches during a bus cycle
  - ALE:  $x = 2$
  - RD#/WR#:  $x = 2$

Total I/O current, Equation 3.7, is calculated by adding equations 3.4, 3.5 and 3.6.

$$\text{Equation 3.7: } I/O \text{ current} = I_{\text{read}} \cdot (0.8) + I_{\text{write}} \cdot (0.2) + I_{\text{control}}$$

The 0.8 and 0.2 factors come from the percentage of read and write bus cycles in a typical system. A similar analysis is required for all devices within a system. The system processor will usually be the most difficult. Once this is done, many of the approximations made apply to calculations for the rest of the system.

### 3.1.3.2 Discrete Component Current

Current consumed by discrete components must also be factored into total system current. Current consumed by pull-up or pull-down resistors, voltage dividers, transistors or other discrete components must be included. These are relatively straightforward calculations, and do not require elaboration.

### 3.1.3.3 Leakage Current

Leakage currents from devices are typically very small and can usually be ignored when calculating system current consumption. When a CMOS device is in a static condition, all p and n transistors inside the device should have their gates driven to  $V_{CC}$  or Ground, turning them on or off. The equivalent resistance of an "off" transistor is approximately 5 M $\Omega$ , the equivalent resistance of an "on" transistor is typically less than 100 $\Omega$ . Some current flows through this resistive path to ground. Typically, this amount will be in the  $\mu\text{A}$  range.

Leakage current can become more significant. If a device is running at a given  $V_{CC}$ , there may be situations where an input is not driven close to  $V_{CC}$ . The p and n transistors of the device input buffers will not be com-

pletely turned on or off. This lowers the equivalent resistance through the transistors to ground. On some devices (AC logic, as an example), at  $V_{IN} = V_{CC} - 2.1V$ , the device may consume as much as 1.5 mA additional current per input pin. Typically, this value is from 100  $\mu A$  to 200  $\mu A$  per input, but still measurable. This additional current exists unless the input to the device is driven close to  $V_{CC}$ . Most logic data sheets list this specification as  $\Delta I_{CC}$ , given as a maximum current per input pin with the input at  $V_{CC} - 2.1V$ .

### 3.1.4 SUMMARY: CALCULATING POWER CONSUMPTION

For a complete system design, total system current consumption must be calculated. This analysis determines power supply design, product packaging and battery life. Although an exact calculation may not be possible (or practical), a worst-case analysis with reasonable approximations allows a reliable system design.

## 3.2 Mixed Voltage System Design

One of the difficulties in designing a low voltage system is product availability. There are a large number of manufacturers producing low voltage products (3V or lower). Embedded processors, like the Intel 80L186EA, EB and EC have been available at 3V for some time. Memory and logic are also widely available. Some peripheral components are still not available at low voltages. Many of these components require redesign to operate at low voltages. Until these components are replaced with low voltage versions, systems requiring their functionality have to utilize the 5V version. This causes tremendous headaches for system designers. System cost, complexity and power consumption all suffer due to the lack of a complete selection of low voltage devices.

### 3.2.1 INTERFACING 3V AND 5V COMPONENTS

Somewhere within a mixed voltage design, the designer must interface 3V and 5V devices. This can happen in 3V to 5V translation, 5V to 3V translation, bidirectional translation or 3V and 5V devices residing on the same system bus. As simple as these interfaces may seem, there are still problems to be solved.

#### 3.2.1.1 3V to 5V Interface

One way to translate a 3V output to a 5V CMOS level is with ACT/HCT logic. These parts accept a TTL level input and give a CMOS output. When operating at 5V, these parts see a 3V level input the same as they would see a 5V TTL level input. The output will be a 5V CMOS level. This is a relatively straightforward approach, but it does have the problem of additional current consumption ( $\Delta I_{CC}$ ).

The JEDEC standard for 3.3V outputs is compatible with TTL input requirements. If the 5V device connected to the 3V output already has TTL compatible inputs, no interface logic is required.

#### 3.2.1.2 5V to 3V Interface

Unfortunately, a 5V output cannot be connected directly to a 3V input. Maximum operating conditions for most devices specify the maximum voltage on any input pin. This number is typically  $V_{CC} + 0.5V$  (LVTTTL and unregulated LVCMOS), and on some 3V devices is  $V_{CC} + 1.0V$  (regulated LVCMOS). A 5V CMOS output high typically drives close to  $V_{CC}$ . When the maximum input voltage is exceeded, the ESD (Electrostatic Discharge) protection diode on the input of the device forward biases and current flows into the 3V  $V_{CC}$  (Figure 3-2). This causes unacceptably high current consumption. Connecting a 5V output to a 3V input leads to reliability problems. Device manufacturers are developing input buffers for low voltage devices that are 5V tolerant, but until these devices are widely available, other solutions are required.

A 5V bipolar TTL device may be connected directly to a 3V input. Some newer 5V CMOS devices have outputs with reduced voltage swings. These devices have 3V compatible outputs and may be connected directly to 3V inputs. The designer must be careful when regulating the 5V and 3V supplies. If the 5V supply goes to 5.5V and the 3.3V supply goes to 3.0V, the 3V input specification could be violated.

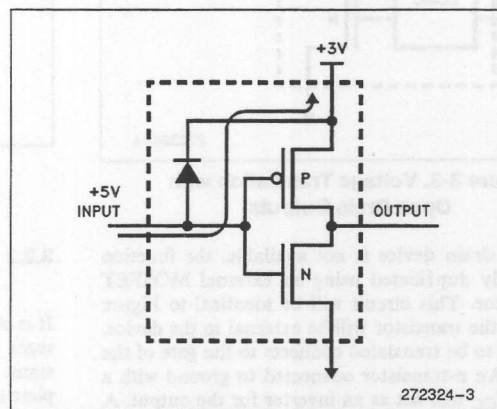


Figure 3-2. 5V Output Driving a 3V Input

There is a way to work around the problem of driving a 3V input with a 5V output. Series resistors can be placed on the outputs of the 5V device. The goal is to drop the voltage to a level acceptable by the 3V device. The value of the resistor must be chosen to limit the



current into the 3V device. The major sacrifice in this solution is speed. If the system can handle the speed degradation, then it is a simple, inexpensive way to translate from 5V to 3V. As a final point on this subject, if this solution is implemented, considerations must be made for system power-up. If the 5V supply ramps much faster than the 3V supply, the substrate diode may still be forward biased temporarily, leading to reliability problems. This situation must be taken into account when determining the resistor value. The designer must either assume the worst case where the 5V part  $V_{CC} = 5.5V$  and the 3V part has  $V_{CC} = 0V$  or the 3V and 5V supplies must be sequenced.

### 3.2.1.3 Voltage Translation with Open Drain Outputs

Open drain output devices provide a simple way to convert from 3V to 5V and vice-versa (Figure 3-3). All that is required is an external pullup resistor to the desired output voltage. If the open drain device outputs a logic "1", there is virtually no current consumption penalty for the conversion. If the output is a logic "0", there is a current path to ground, but a high resistance pullup will limit the amount of current (at the cost of speed).

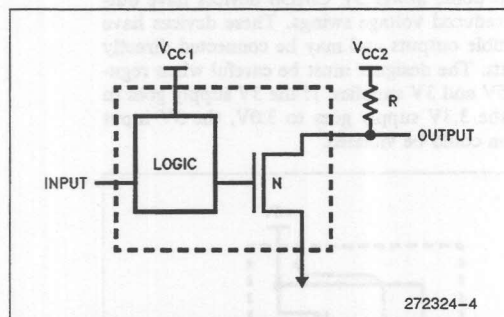


Figure 3-3. Voltage Translation with Open Drain Outputs

If an open drain device is not available, the function can be easily duplicated using an external MOSFET and a resistor. This circuit will be identical to Figure 3-3, except the transistor will be external to the device. The output to be translated connects to the gate of the transistor. An n-transistor connected to ground with a pullup to  $V_{CC}$  will act as an inverter for the output. A p-transistor connected to ground with a pullup resistor will not invert the output. The switching time required by the external MOSFET must be considered when determining system timing.

### 3.2.1.4 Bidirectional Translation

The methods described above all work well for translating unidirectional signals. What happens if a 5V peripheral resides on a 3V bus? Ideally, a designer could place a 5V device and a 3V device on the same system bus. Unfortunately, a floated 3V output will be damaged when a 5V part drives the bus. Depending on the state of the inputs to the 3V device output buffers, it is possible that the p-transistor will turn on (Figure 3-4). If this device turns on, the 5V supply and 3V supply are shorted together. Even if this situation does not occur, the 5V signal still forward biases the ESD protection diodes inside the 3V device, creating a situation similar to a 5V output driving a 3V input. Fortunately, a number of manufacturers are producing buffers with two  $V_{CC}$  pins. The devices translate bidirectionally between the two  $V_{CC}$  values. These are the most practical solution for bidirectional translation between 3V and 5V. System busses must operate at a single voltage with other voltages buffered.

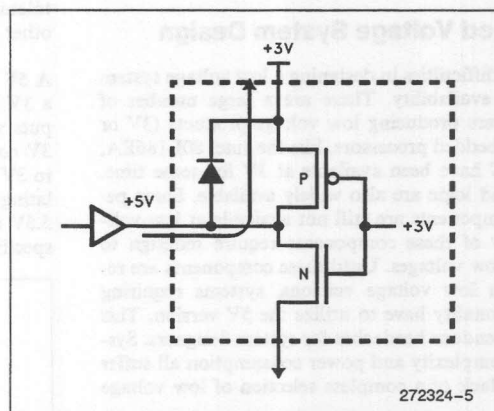


Figure 3-4. 5V Device Driving a Floated 3V Output

### 3.2.2 DISADVANTAGES OF MIXED VOLTAGE SYSTEMS

It is obvious at this point that there really are no advantages to mixed voltage systems over complete 3V designs. They only exist because of the absence of a complete selection of low voltage devices. During the industry's transition to 3V, the objective of designers is to minimize the disadvantages of mixed voltage systems. Two of the drawbacks of mixed voltage systems are voltage supply requirements and additional current consumption.

### 3.2.2.1 Multiple Supplies in Mixed Voltage Systems

A major disadvantage of mixed voltage systems is the requirement of multiple voltage supplies. A typical system may require 3V (major components, memory), 5V (older peripherals, small displays),  $\pm 12V$  (RS-232 communications) and even higher voltages (backlit LCD displays, etc.). One goal in designing a mixed voltage system is to minimize the number of required voltages and the number of devices used to create them. To avoid the extra chip-count associated with creating multiple voltages, some manufacturers, offer one-chip solutions to provide multiple voltages from 2 or 3 cells. The designer can also take advantage of parts with internal charge pumps that take 3V or 5V inputs and create the output voltage levels they require. Although multiple voltages can easily be created with a minimal number of chips, the designer still pays the price for having non-3V parts in the system: battery life. As technology moves forward and 3V designs gain momentum, more components will be available at low voltage (3V or less). This eliminates the requirement for multiple system voltages and the added system cost and complexity associated with creating them.

### 3.2.2.2 Additional Current Consumption in Mixed Voltage Systems

Interfacing 3V and 5V devices in a mixed voltage system is unavoidable. Regardless of how a designer implements these interfaces, they will all have one common characteristic, additional current consumption.

Some devices have an additional specification called  $\Delta I_{CC}$  (or  $I_{CCT}$ ). This specification defines the additional current consumed, per input pin, if an input high voltage is at  $V_{CC} - 2.1V$ . This situation closely resembles using ACT or HCT logic for 3V to 5V translation. This number can be up to 1.5 mA per input pin. Consider a unidirectional, 16-bit bus translated from 3V to 5V using ACT logic. In a worst-case situation, this can be a major source of continuous current consumption. This is a maximum value, typically the extra current amounts to 100  $\mu A$  to 200  $\mu A$  per input pin. Additionally, this specification only applies to a logic "1" input, and typically, only a fraction of the 3V inputs are high at any time.

The reason behind the extra current consumption when using ACT/HCT logic for 3V to 5V translation lies in the input buffers (Figure 3-5). If the input of the device is driven all the way to  $V_{CC}$ , the p-transistor turns completely off and the n-transistor turns completely on. This can be roughly modeled as 5V connected to ground through a 5 M $\Omega$  resistor. As shown by the graph in Figure 3-5, the only current flowing is leakage current, almost nothing.

As the voltage on the input moves farther away from  $V_{CC}$ , the input transistors move closer to their saturation region. The resistance path through the transistors to ground decreases from the initial 5 M $\Omega$ . This increases the current flow through them. The graph shows this current to be on the order of 150  $\mu A$  per input with a 3V input (at room temperature).

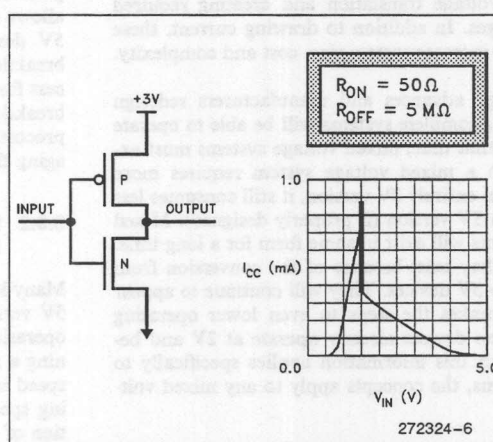


Figure 3-5. Current When Using ACT/HCT Logic for Voltage Conversion

This leads to a valid question. If there is such a penalty for creating mixed voltage systems, is the system better off running at 5V? An analysis of system current consumption must be done for the pure 5V and mixed voltage cases. If only a small part of the system can operate at 3V, the extra power for voltage translation may offset the benefit of using 3V parts. This accents the need to have a complete selection of devices that operate at 3V.

### 3.2.3 SUMMARY: MIXED VOLTAGE SYSTEMS

There are a number of considerations a designer must make when designing a mixed voltage system. Interfacing 3V and 5V logic must be done carefully. There are many solutions to do this, but if done incorrectly, the system eventually fails. Many manufacturers provide simple solutions to do unidirectional and bidirectional transfers. These solutions are probably the easiest to implement and consume a minimal amount of power.

A mixed voltage system, by definition, consumes more current than a pure 3V system. This added current consumption comes from different sources. Any method used to translate from one voltage to another requires additional current. A mixed voltage system also has more devices than a pure 3V system. Extra devices are needed for voltage translation and creating required system voltages. In addition to drawing current, these extra devices increase system size, cost and complexity.

As technology advances and manufacturers redesign current parts, complete systems will be able to operate at 3V. Until that time, mixed voltage systems must exist. Although a mixed voltage system requires more power than an entirely 3V version, it still consumes less power than a 5V version (if properly designed). Mixed voltage systems will exist in some form for a long time. Right now, they exist because of the conversion from 5V devices to 3V devices. They will continue to appear as industry makes the steps to even lower operating voltages. Some devices already operate at 2V and below. Although this information applies specifically to 3V/5V systems, the concepts apply to any mixed voltage system.

### 3.3 Single Voltage System Design

Complete 3V designs have few disadvantages, the exceptions being operating speed and noise immunity. Advantages include: longer battery life, less heat and

lower noise emissions. The advantages of a complete 3V system are significant compared to the minimal design effort required to work around the disadvantages.

#### 3.3.1 DEVICES DESIGNED FOR LOW VOLTAGE OPERATION

Currently, some devices are designed for 3V only operation. Devices optimized for 3V operation are generally specified for operation from 3.0V to 3.6V. These devices exhibit the performance of their 5V counterparts at significantly lower power. The high performance and narrow operating voltages of these parts limits their benefit to embedded, battery operated designs.

If a fabrication process is optimized for 3V operation, gate oxides are thinner. The increased gate capacitance allows a 3V device to function at the same speed as a 5V device produced on a non-3V processes. Oxide breakdown is the major drawback to optimizing a process for 3V. A thinner gate oxide implies a lower oxide breakdown voltage. Devices produced on the optimized process will not be able to operate at 5V without damaging the part.

#### 3.3.2 DEVICES DERATED FOR LOW VOLTAGE OPERATION

Many low voltage products are derated versions of their 5V versions. These devices are specified, typically, for operation from 2.7V to 5.5V. The only sacrifice of running a product designed for 5V at 3V is speed. Device speed is a function of internal switching speeds. Switching speeds are proportional to device current, a function of gate oxide capacitance and gate voltages within a device. A device produced on a process not optimized for 3V will have a thicker gate oxide, decreasing gate capacitance, reducing current. The combination of lower gate voltage and capacitance limits operating speeds for derated 5V devices. For many embedded systems, speed is not critical. Using devices that operate from 2.7V to 5.5V allows the designer to use inexpensive alkaline batteries and avoid the added device count and efficiency losses of voltage regulators.



### 3.3.3 NOISE GENERATION BY LOW VOLTAGE DEVICES

Overshoot, undershoot and ground bounce all relate to  $dV/dt$ ,  $dV$  being the output voltage swing and  $dt$  being the output switching time. In low voltage devices, obviously, voltage levels decrease, lowering the  $dV$  term. This applies to all low voltage devices. Devices designed specifically for low voltage operation, which have smaller geometries and thinner gate oxides, have switching times comparable to the 5V versions. Therefore, the  $dt$  term remains relatively constant. Low voltage devices which are derated versions of 5V parts have slower switching times when operating voltage decreases. The  $dt$  term increases for devices derated for low voltage operation. Derated devices generate very little noise.

Regardless of the exact amount of noise a low voltage device generates (derated or not), any low voltage device will produce less noise than its 5V counterpart.  $dV/dt$  and practicing good PCB design techniques (multi-layer, bypass capacitors, etc.), should eliminate noise as a problem.

### 3.3.4 NOISE MARGINS IN LOW VOLTAGE SYSTEMS

In devices with CMOS compatible inputs, input high ( $V_{IH}$ ) and input low ( $V_{IL}$ ) voltage specifications are a function of operating voltage. The difference between  $V_{IH}$  and  $V_{IL}$  defines the noise margin on the input (Equation 3.8).

$$\text{Equation 3.8: Noise Margin} = V_{IH} - V_{IL}$$

Typically,  $V_{IH}$  is  $0.7 \cdot V_{CC}$  and  $V_{IL}$  is  $0.3 \cdot V_{CC}$  on CMOS compatible inputs. This defines a noise margin of  $0.4 \cdot V_{CC}$ . If operating voltage decreases from 5.0V, noise margins decrease proportionally.

Devices with TTL compatible inputs will not see any change in noise margins when operating at 3V. TTL inputs define  $V_{IH}$  as 2.0V and  $V_{IL}$  as 0.8V. The standards for input levels on 3.3V devices are defined to be compatible with the TTL standard. This is why a 3.3V output can directly interface with a 5V device with TTL inputs.

Noise susceptibility of low voltage systems is not as significant as it may appear. Low voltage systems generate less noise than 5V systems. If a system generates less noise, decreased noise margins on device inputs be-

come less important. Additionally, good Printed Circuit Board layout techniques should eliminate major noise issues.

## 4.0 SYSTEM POWER MANAGEMENT

When creating a battery operated system, the designer is concerned with extending battery life as long as possible. Reducing operating voltages is a relatively simple way to achieve a significant reduction in power consumption. Voltage reduction is an excellent start to increasing battery life, but numerous power management techniques exist to provide even lower power consumption.

### 4.1 Device Power Management

Many Intel embedded processors have modes of operation designed to reduce current consumption. Many static-design embedded processors have Powerdown mode, disabling the clock input to the device. Disabling the clock input eliminates transistor switching within the device, reducing current consumption to leakage current (microamps). Other devices have Idle mode which disables the clock to the CPU, but keeps integrated peripherals active. This decreases current consumption by a smaller amount than Powerdown mode, but is excellent for devices requiring peripherals to remain active at all times. Finally, many embedded processors offer Powersave mode. Powersave mode internally divides the clock input to the device. Because processor current consumption is approximately a linear function of clock frequency, Powersave mode significantly reduces current consumption during execution of non-critical sections of code. Including one or more of these power management functions on silicon reduces board space required to create them separately, if they can be created at all (Idle mode, for example).

Other devices that commonly appear in embedded systems also offer power management features in silicon. Some Intel Flash memory devices offer a powerdown mode, reducing current to leakage levels. Other memories enter a "sleep" mode when not being accessed, reducing current consumption. Even some regulators allow their output to be shut down to decrease current consumption.

Many devices exist offering power management features which enhance low voltage operation. When system designers select components for their systems, parts should be chosen which offer benefits beyond just low voltage operation.

## 4.2 Software Power Management

Power management schemes need to be implemented in software as well as hardware. Software controls power management modes on Intel embedded processors and can be used to control power management on external devices (using port pins, etc.). Software can also be implemented to reduce switching on address and data buses and processor outputs.

### 4.2.1 IMPLEMENTING DELAYS

Many applications require time delays. For example, there may be a minimum time required between successive writes to an LCD display or other peripherals. These delays can be implemented either in hardware (controlled by software) or software. When delay loops are implemented in software, every iteration of that loop will execute a given number of bus cycles. Every bus cycle will drive address information onto the bus and all of the relevant control signals that define a bus cycle and turn on the memory device(s) containing program code. With enough iterations of the loop, a large amount of current is consumed. One solution is to divide the processor clock during these delays. Dividing the clock by a factor of  $x$  reduces the number of bus cycles required by  $x$ , for the same delay.

Implementing a delay with hardware and software is simple. Timers are used to create the delay. A timer can be programmed to cause an interrupt after a set delay. The timer needs to be programmed with the correct count and enabled. If the delay is long enough, it may

even make sense to put the processor into a power management mode (such as Idle mode or Powersave mode). This entire process requires a small number of bus cycles. If the overhead associated with interrupt servicing is a limitation, some processors allow the designer to implement delays without interrupts.

The 80C186, for example, has an input called TEST#. The TEST# pin is sampled during the WAIT instruction. The processor stops execution during a WAIT until the TEST# pin is sampled low. If the output of a timer is connected to the TEST# input, the timer times-out and pulls its output low, causing the processor to continue execution. This solution requires only enough bus cycles to program the timer.

### 4.2.2 CODE OPTIMIZATION

Program code can also be optimized for minimal power consumption. To minimize switching on the address bus, code should be written to reduce the number of jumps that occur. Interrupt driven code is also preferable to code which depends on polling routines. The processor can issue a HLT instruction and wait for an interrupt rather than constantly looping to poll a register bit. The reduction in power consumption by using these methods may be slight but still increases battery life.

Power management is very important to low voltage embedded designs. The effort to add power management is minimal but the benefits are significant. Using hardware and software to minimize power consumption increases battery life with little or no increase in system cost or complexity.

**Intel 430TX PCIset: 82439TX System  
Controller (MTXC)**





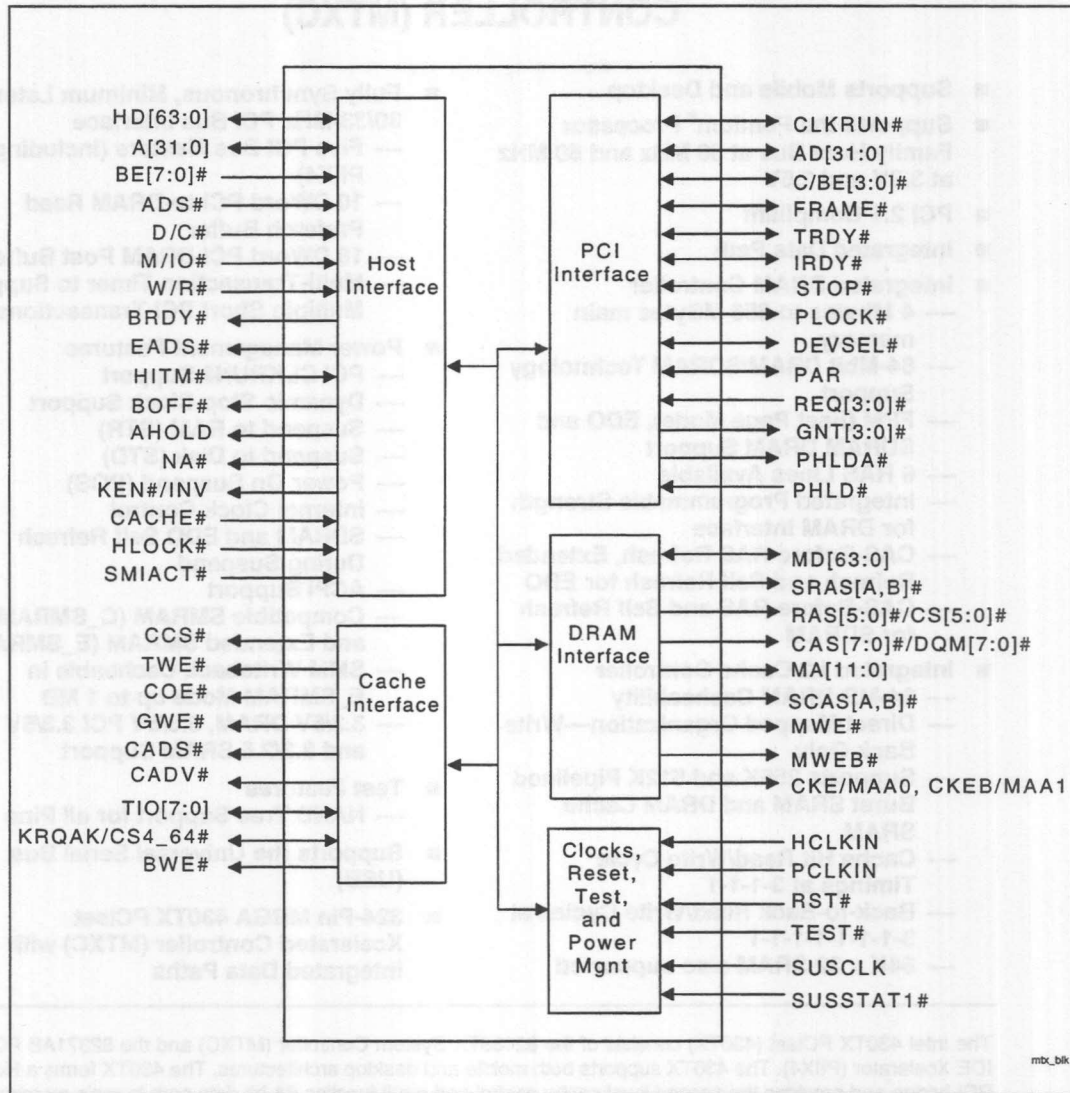


## INTEL 430TX PCISSET: 82439TX SYSTEM CONTROLLER (MTXC)

- Supports Mobile and Desktop
- Supports the Pentium® Processor Family Host Bus at 66 MHz and 60 MHz at 3.3V and 2.5V
- PCI 2.1 Compliant
- Integrated Data Path
- Integrated DRAM Controller
  - 4 Mbytes to 256 MBytes main memory
  - 64-Mbit DRAM/SDRAM Technology Support
  - FPM (Fast Page Mode), EDO and SDRAM DRAM Support
  - 6 RAS Lines Available
  - Integrated Programmable Strength for DRAM Interface
  - CAS-Before-RAS Refresh, Extended Refresh and Self Refresh for EDO
  - CAS-Before-RAS and Self Refresh for SDRAM
- Integrated L2 Cache Controller
  - 64-MB DRAM Cacheability
  - Direct Mapped Organization—Write Back Only
  - Supports 256K and 512K Pipelined Burst SRAM and DRAM Cache SRAM
  - Cache Hit Read/Write Cycle Timings at 3-1-1-1
  - Back-to-Back Read/Write Cycles at 3-1-1-1-1-1-1-1
  - 64K x 32 SRAM also supported
- Fully Synchronous, Minimum Latency 30/33-MHz PCI Bus Interface
  - Five PCI Bus Masters (including PIIX4)
  - 10 DWord PCI-to-DRAM Read Prefetch Buffer
  - 18 DWord PCI-DRAM Post Buffer
  - Multi-Transaction Timer to Support Multiple Short PCI Transactions
- Power Management Features
  - PCI CLKRUN# Support
  - Dynamic Stop Clock Support
  - Suspend to RAM (STR)
  - Suspend to Disk (STD)
  - Power On Suspend (POS)
  - Internal Clock Control
  - SDRAM and EDO Self Refresh During Suspend
  - ACPI Support
  - Compatible SMRAM (C\_SMRAM) and Extended SMRAM (E\_SMRAM)
  - SMM Writeback Cacheable in E\_SMRAM Mode up to 1 MB
  - 3.3/5V DRAM, 3.3/5V PCI 3.3/5V Tag and 3.3/2.5 SRAM Support
- Test Features
  - NAND Tree Support for all Pins
- Supports the Universal Serial Bus (USB)
- 324-Pin MBGA 430TX PCISet Xcelerated Controller (MTXC) with integrated Data Paths

The Intel 430TX PCISet (430TX) consists of the 82439TX System Controller (MTXC) and the 82371AB PCI ISA IDE Xcelerator (PIIX4). The 430TX supports both mobile and desktop architectures. The 430TX forms a Host-to-PCI bridge and provides the second level cache control and a full function 64-bit data path to main memory. The MTXC integrates the cache and main memory DRAM control functions and provides bus control to transfers between the CPU, cache, main memory, and the PCI Bus. The second level (L2) cache controller supports a writeback cache policy for cache sizes of 256 Kbytes and 512 Kbytes. Cacheless designs are also supported. The cache memory can be implemented with pipelined burst SRAMs or DRAM cache SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM for the cache line status bits. For the MTXC DRAM controller, six rows are supported for up to 256 Mbytes of main memory. The MTXC is highly integrated by including the Data Path into the same BGA chip. Using the snoop ahead feature, the MTXC allows PCI masters to achieve full PCI bandwidth. For increased system performance, the MTXC integrates posted write and read prefetch buffers. The 430TX integrates many Power Management features that enable the system to save power when the system resources become idle.

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MTXC Simplified Block Diagram



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The MTXC works with the PCI IDEATA Accelerator 4 (PIA4). The PIA4 provides the PCI-to-SATA bridge functions along with other features such as a fast IDE interface (PIO mode 4 and Ultra DMA/33), Full-Port SATA interface, PCI 3.1 Compliant, SATA interface, and Universal Serial Bus Host Controller functions.

#### DRAM Interface

The DRAM interface is a 64-bit data path that supports Standard for Fast Page Mode (FPM), Extended Data Out (EDO), and Synchronous DRAM (SDRAM) memory. The DRAM controller inside the MTXC is capable of generating 3-1-1-1 for posted writes for any type of DRAM that is used. While read performance is 3-1-1-1 for SDRAM, 3-2-2-2 for EDO, and 3-2-2-2 for FPM.

The DRAM interface supports 4 Mbytes to 512 Mbytes with six CAS lines. The MTXC supports 4-MB, 16-MB, and 32-MB DRAM and SDRAM technology, both synchronous and asynchronous. Parity is not supported, and in testing, errors were not detected. DRAMs should be used.

#### Second Level Cache

The second level cache is a 64-Kbyte cache and supports both 33-MHz and 50-MHz DRAM configurations using Rambus DRAM or DRAM Cache SRAM. The cache performance is 3-1-1-1 for the read/write and 3-1-1-1-1-1-1-1 for back to back reads that are pipelined. Cache write configuration is also supported.

#### PCI Interface

The PCI interface is 3.1 compliant and supports up to four PCI bus masters in addition to the PIA4 bus master.

#### Data Path and Buffers

The MTXC contains three sets of data buffers for processing data flow. A five 64-Kbyte deep DRAM write buffer is provided for CPU-to-DRAM writes, second level cache write buffer, and PCI-to-DRAM transfers. The buffer is used to achieve 3-1-1-1 posted writes to DRAM and also provides 64-Kbyte write buffer and burst merging for CPU-to-DRAM write buffer. In addition, an extra line of buffering is provided that is combined with the DRAM write buffer to supply an 18 64-Kbyte deep buffer for PCI to write memory writes. A five 64-Kbyte buffer is provided for CPU-to-PCI writes to help maintain the bandwidth for posted writes to the PCI bus. Also, five 64-Kbyte of posted buffering has been added to the CPU-to-DRAM read path and allows up to two lines of data to be prefetched at an x-2-2-2 rate. The MTXC interface directly to the host and DRAM data bus.

#### Power Management Features

The MTXC implements extensive power management features. The GUPRIS feature enables controlling of the PCI clock (on/off). The MTXC supports P0S, S1R, S1D, and Soft-off suspend states. SUSCLK and



## 1.0. ARCHITECTURE OVERVIEW

The MTXC host bridge provides a completely integrated solution for the system controller and datapath components in a Pentium processor system. The MTXC Supports all Pentium family processors since P54C, it has 64-bit Host and DRAM Bus Interface, 32-bit PCI Bus Interface, Second level Cache Interface, and it integrates the PCI arbiter.

The MTXC interfaces with the Pentium processor host bus, a dedicated memory data bus, and the PCI bus (see Figure 1).

The MTXC bus interfaces are designed to interface with 2.5V, 3.3V and 5V busses. The MTXC implements 2.5V and 3.3V drivers and 5V tolerant receivers. The MTXC connects directly to the Pentium processor 3.3V or 2.5V host bus, directly to 5V or 3.3V DRAMs, and directly to the 5V or 3.3V PCI bus. The 430TX also interfaces directly to the 3.3V or 5.0V TAGRAM and 3.3V Cache.

The MTXC works with the PCI IDE/ISA Accelerator 4 (PIIX4). The PIIX4 provides the PCI-to-ISA/EIO bridge functions along with other features such as a fast IDE interface (PIO mode 4 and Ultra DMA/33), Plug-n-Play port, APIC interface, PCI 2.1 Compliance, SMBUS interface, and Universal Serial Bus Host Controller functions.

### DRAM Interface

The DRAM interface is a 64-bit data path that supports Standard (or Fast) Page Mode (FPM), Extended Data Out (EDO) and Synchronous DRAM (SDRAM) memory. The DRAM controller inside the MTXC is capable of generating 3-1-1-1 for posted writes for any type of DRAM that is used. While read performance is 6-1-1-1 for SDRAM, 5-2-2-2 for EDO, and 6-3-3-3 for FPM.

The DRAM interface supports 4 Mbytes to 256 Mbytes with six RAS lines. The MTXC supports 4-Mbit, 16-Mbit, and 64-Mbit DRAM and SDRAM technology, both symmetrical and asymmetrical. Parity is not supported, and for loading reasons, x32 and x64 SIMMs/DIMMs/SO-DIMMs should be used.

### Second Level Cache

The second level cache is direct mapped and supports both 256-Kbyte and 512-Kbyte SRAM configuration using Pipeline Burst SRAM or DRAM Cache SRAM. The Cache performance is 3-1-1-1 for line read/write and 3-1-1-1-1-1-1-1 for back to back reads that are pipelined. Cacheless configuration is also supported.

### PCI Interface

The PCI interface is 2.1 compliant and supports up to four PCI bus masters in addition to the PIIX4 bus master requests.

### Datapath and Buffers

The MTXC contains three sets of data buffers for optimizing data flow. A five QWord deep DRAM write buffer is provided for CPU-to-DRAM writes, second level cache write backs, and PCI-to-DRAM transfers. This buffer is used to achieve 3-1-1-1 posted writes to DRAM and also provides DWord merging and burst merging for CPU-to-DRAM write cycles. In addition, an extra line of buffering is provided that is combined with the DRAM Write Buffer to supply an 18 DWord deep buffer for PCI to main memory writes. A five DWord buffer is provided for CPU-to-PCI writes to help maximize the bandwidth for graphic writes to the PCI bus. Also, five QWords of prefetch buffering has been added to the PCI-to-DRAM read path that allows up to two lines of data to be prefetched at an x-2-2-2 rate. The MTXC interfaces directly to the Host and DRAM data bus.

### Power Management Features

The MTXC implements extensive power management features. The CLKRUN# feature enables controlling of the PCI clock (on/off). The MTXC supports POS, STR, STD, and Soft-off suspend states. SUSCLK and

SUSSTAT1# signals are used for implementing Suspend Logic. The MTXC supports two SMRAM modes; Compatible SMRAM (C\_SMRAM) and Extended SMRAM (E\_SMRAM). The C\_SMRAM is the traditional SMRAM feature implemented in Intel PCIsets. The E\_SMRAM is a new feature that supports writeback cacheable SMRAM space up to 1 Mbytes. In order to minimize the idle power, the internal clock in MTXC is turned off (gated off) when there is no activity on the Host and PCI Bus.

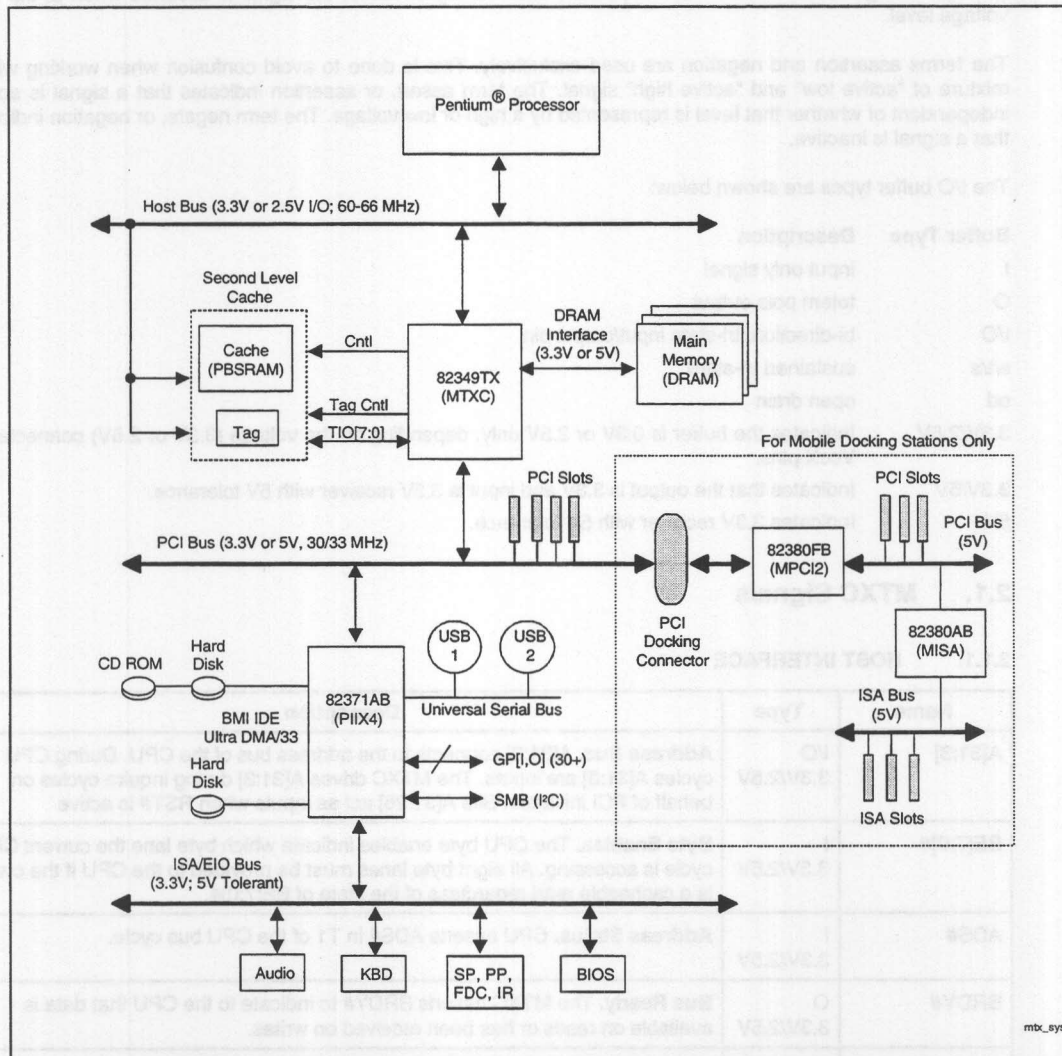


Figure 1. MTXC System Block Diagram

## 2.0. SIGNAL DESCRIPTION

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “#” symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “#” is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signal. The term assert, or assertion indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation indicates that a signal is inactive.

The I/O buffer types are shown below:

Buffer Type	Description
I	input only signal
O	totem pole output
I/O	bi-direction, tri-state input/output pin
s/t/s	sustained tri-state
od	open drain
3.3V/2.5V	Indicates the buffer is 3.3V or 2.5V only, depending on the voltage (3.3V or 2.5V) connected to VccX pins.
3.3V/5V	Indicates that the output is 3.3V and input is 3.3V receiver with 5V tolerance.
5V	Indicates 3.3V receiver with 5V tolerance.

## 2.1. MTXC Signals

### 2.1.1. HOST INTERFACE

Name	Type	Description
A[31:3]	I/O 3.3V/2.5V	<b>Address Bus.</b> A[31:3] connects to the address bus of the CPU. During CPU cycles A[31:3] are inputs. The MTXC drives A[31:3] during inquire cycles on behalf of PCI initiators. Bits A[31:26] act as inputs when RST# is active
BE[7:0]#	I 3.3V/2.5V	<b>Byte Enables.</b> The CPU byte enables indicate which byte lane the current CPU cycle is accessing. All eight byte lanes must be provided to the CPU if the cycle is a cacheable read regardless of the state of BE[7:0]#.
ADS#	I 3.3V/2.5V	<b>Address Status.</b> CPU asserts ADS# in T1 of the CPU bus cycle.
BRDY#	O 3.3V/2.5V	<b>Bus Ready.</b> The MTXC asserts BRDY# to indicate to the CPU that data is available on reads or has been received on writes.
NA#	O 3.3V/2.5V	<b>Next Address.</b> This signal is asserted by the MTXC to indicate to the Processor that it is ready to process a second cycle.



Name	Type	Description
AHOLD	O 3.3V/2.5V	<b>Address Hold.</b> The MTXC asserts AHOLD when a PCI initiator is performing a cycle to DRAM. AHOLD is held for the duration of the PCI burst transfer. The MTXC will negate AHOLD when the completion of the PCI to DRAM read or write cycles complete and during PCI peer transfers. AHOLD is kept asserted while PHLDA# is asserted (i.e., duration of PIIX4 granting).
EADS#	O 3.3V/2.5V	<b>External Address Strobe.</b> Asserted by the MTXC to inquire the first level cache when servicing PCI master references of DRAM.
BOFF#	O 3.3V/2.5V	<b>Back Off.</b> Asserted by the MTXC when required to terminate a CPU cycle that was in progress.
HITM#	I 3.3V/2.5V	<b>Hit Modified.</b> Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the first level cache and needs to be written back.
M/IO#, D/C#, W/R#	I 3.3V/2.5V	<b>Memory/IO; Data/Control; Write/Read.</b> Asserted by the CPU with ADS# to indicate the type of cycle that the system needs to perform.
HLOCK#	I 3.3V/2.5V	<b>Host Lock.</b> All CPU cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no PCI activity to DRAM is allowed.
CACHE#	I 3.3V/2.5V	<b>Cache.</b> Asserted by the CPU during a read cycle to indicate the CPU will perform a burst line fill. Asserted by the CPU during a write cycle to indicate the CPU will perform a burst writeback cycle. If CACHE# is asserted to indicate cacheability, the MTXC will assert KEN# either with the first BRDY#, or with NA# if NA# is asserted before the first BRDY#.
KEN#/INV	O 3.3V/2.5V	<b>Ken/Invalidate.</b> KEN#/INV functions as both the KEN# signal during CPU read cycles, and the INV signal during L1 snoop cycles. During CPU cycles, KEN#/INV is normally low. KEN#/INV is driven high during the 1st BRDY# or NA# assertion of a non-L1-cacheable CPU read cycle.  KEN#/INV is driven high(low) during the EADS# assertion of a PCI master DRAM write(read) snoop cycle. Note that KEN#/INV operation during snoop cycles is independent of the FLCE bit programming.
SMIACT#	I 3.3V/2.5V	<b>System Management Interrupt Active.</b> This is asserted by the CPU when it is in system management mode as a result of an SMI. This signal must be sampled active with ADS# for the processor to access the SMM space of DRAM, located at A0000h, after SMM space has been loaded and locked by BIOS at system boot.
HD[63:0]	I/O 3.3V/2.5V	<b>Host Data.</b> These signals are connected to the CPU data bus. These signals have internal pull-down resistors.

**NOTES:**

All of the signals in the host interface are described in the Pentium Processor data sheet. The preceding table highlights MTXC specific uses of these signals.

## 2.1.2. DRAM INTERFACE

Name	Type	Description
RAS[3:0]# or CS[3:0]#, RAS4#/CS4#/ BA1, RAS5#/CS5#/ MA13	O 3.3 V	<b>Row Address Strobe—RASx# (EDO/FPM).</b> These pins select the DRAM row. <b>Chip Select—CSx# (SDRAM).</b> These pins activate the SDRAMs. SDRAM accepts any command when its CS# pin is active low.  Note: For 64Mbit SDRAM support, BA1/MA12 and MA13 are muxed with the RAS4# and RAS5# signals, respectively. When SDRAMC[bit 1]=1, BA1 and MA13 are driven out on these lines.
CAS[7:0]# or DQM[7:0]	O 3.3 V	<b>Column Address Strobe (EDO/FPM).</b> These pins select the DRAM column. <b>Input/Output Data Mask SDRAM.</b> These pins act as synchronized output enables during a read cycle and a byte mask during a write cycle. The read cycles require Tdqz clock latency before the functions are actually performed. In case of a write cycle, word mask functions are performed in the same cycle (0 cycle latency).
MA[11:0]	O 3.3 V	<b>Memory Address (EDO/FPM/SDRAM).</b> This is the row and column address for DRAM. These buffers now include programmable size selection, as controlled by the DRAMEC[MAD] bit. For 64-Mbit SDRAM support BA1/MA12 and MA13 are muxed with the RAS4# and RAS5# signals, respectively.
MWEB#	O 3.3 V	<b>Memory Write Enable (second copy) (EDO/FPM/SDRAM).</b> MWE# should be used as the write enable for the memory data bus. This signal has programmable buffer size selection.
MWE#	O 3.3 V	<b>Memory Write Enable (EDO/FPM/SDRAM).</b> MWE# should be used as the write enable for the memory data bus. This signal has programmable buffer size selection.
SRAS[A,B]#	O 3.3 V	<b>SDRAM Row Address Strobe (SDRAM).</b> When asserted, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and precharge. Two copies are provided for loading purpose. These signals have programmable buffer size selection.
SCAS[A,B]#	O 3.3 V	<b>SDRAM Column Address Strobe (SDRAM).</b> When asserted, this signal latches Column Address on the positive edge of the clock. This signal also allows Column access. Two copies provided for loading purpose. These signals have programmable buffer size selection.
CKE/MAA0	O 3.3 V	<b>SDRAM Clock Enable (SDRAM).</b> SDRAM clock enable pin. When this signal is negated, SDRAM enters power down mode. This signal is also muxed to provide a second copy of memory address MA0 (MAA0). The MA function is selected via DRT[bit2] (offset 67h).  MTXC negates CKE (and CKEB) when SUSSTAT1# is asserted. Note that MTXC asserts CKE (and CKEB) for all rows (i.e., CKE and CKEB cannot be selectively asserted for certain rows and negated for other rows).

Name	Type	Description
CKEB/MAA1	O 3.3 V	<b>SDRAM Clock Enable (SDRAM) (second copy).</b> SDRAM clock enable pin. When this signal is negated, SDRAM enters into power down mode. Note that this signal is not implemented in the "Suspend Well" and should not be used if suspend to RAM (STR) is implemented. This signal is also muxed to provide a second copy of memory address MA1 (MAA1). The MA function is selected via DRT[bit2] (offset 67h).  MTXC negates CKE (and CKEB) when SUSSTAT1# is asserted. Note that MTXC asserts CKE (and CKEB) for all rows (i.e., CKE and CKEB cannot be selectively asserted for certain rows and negated for other rows).
MD[63:0]	I/O 3.3V/5V	<b>Memory Data.</b> These signals are connected to the DRAM data bus. These signals have internal pull-down resistors



## 2.1.3. SECONDARY CACHE INTERFACE

Name	Type	Description
CADV#	O 3.3V	<b>Cache Advance.</b> Assertion causes the PBSRAM in the secondary cache to advance to the next QWord in the cache line.
CADS#	O 3.3V	<b>Cache Address Strobe.</b> Assertion causes the PBSRAM in the secondary cache to load the PBSRAM address register from the PBSRAM address pins.
CCS#	O 3.3V	<b>Cache Chip Select (CCS#).</b> The second level cache will power up, if necessary, and perform an access if this signal is asserted when CADS# is asserted. The second level cache will power down if this signal is negated when CADS# is asserted. When CCS# is negated the second level cache will ignore ADS#. If CCS# is asserted when ADS# is asserted, the second level cache will power up, if necessary, and perform an access.
COE#	O 3.3V	<b>Cache Output Enable.</b> The secondary cache data RAMs drive the CPUs data bus when COE# is asserted.
GWE#	O 3.3V	<b>Global Write Enable.</b> GWE# assertion causes all the byte lanes to be written into the secondary cache data RAMs, if they are powered up.
BWE#	O 3.3V	<b>Byte Write Enable.</b> Asserted low with GWE#=HIGH to enable using host's BE[7:0]# to be used to control byte lanes to pipeline burst SRAM cache.
TIO[7:0]	I/O 3.3V/5V	<b>Tag Address.</b> These are inputs during CPU accesses and outputs during second level cache line fills and second level cache line invalidates due to inquire cycles. These signals have internal pull-down resistors.
TWE#	O 3.3V	<b>Tag Write Enable.</b> When asserted, new state and tag addresses are written into the external tag.
KRQAK/ CS4_64#	I/O 3.3V	<p><b>KRQAK/Chip Select 4 (for 64-Mb Technology).</b> This pin is a dual-function signal. KRQAK is used in a DRAM Cache L2 implementation and is a bi-directional refresh request/acknowledge. The CS4_64# function is used to generate the fifth chip select line in a SDRAM L2 Cache implementation that supports five rows of 64-Mbit SDRAM.</p> <p>During a hard reset, this signal is sampled to determine if DRAM cache is in the system (see MTXC Strapping options). This signal has a weak internal pull-down.</p> <p>If SDRAMC[bit 1]=1 and DRAM cache is not present in the system (indicated by CEC[bit 5]=0, offset 53h), the CS4_64# function is selected. If DRAM cache is in the system or SDRAMC[bit 1] (offset 54h)=0, then KRQAK is used to drive the KRQAK function.</p>

#### 2.1.4. PCI INTERFACE

Name	Type	Description
AD[31:0]	I/O 3.3/5V	<b>Address/Data.</b> The standard PCI address and data lines. Address is driven with FRAME# assertion, data is driven or received in following clocks.
C/BE[3:0]#	I/O 3.3/5V	<b>Command/Byte Enable.</b> The command is driven with FRAME# assertion, byte enables corresponding to supplied or requested data is driven on following clocks.
FRAME#	I/O 3.3/5V	<b>Frame.</b> Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
DEVSEL#	I/O 3.3/5V	<b>Device Select.</b> This signal is driven by the MTXC when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O 3.3/5V	<b>Initiator Ready.</b> Asserted when the initiator is ready for a data transfer.
TRDY#	I/O 3.3/5V	<b>Target Ready.</b> Asserted when the target is ready for a data transfer.
STOP#	I/O 3.3/5V	<b>Stop.</b> Asserted by the target to request the master to stop the current transaction.
LOCK#	I/O 3.3/5V	<b>Lock.</b> Used to establish, maintain, and release resource locks on PCI.
REQ[3:0]#	I 3.3/5V	<b>PCI Request.</b> PCI master requests for PCI bus.
GNT[3:0]#	O 3.3V	<b>PCI Grant.</b> Permission is given to the master to use PCI.
PHLD#	I 3.3/5V	<b>PCI Hold.</b> This signal comes from the expansion bridge. It is the bridge request for PCI. The MTXC will drain the DRAM write buffers, drain the CPU-to-PCI posting buffers, and acquire the host bus before granting via PHLDA#.
PHLDA#	O 3.3V	<b>PCI Hold Acknowledge.</b> This signal is driven by the MTXC to grant PCI to the expansion bridge. PHLDA# protocol has been modified to include support for passive release.
PAR	I/O 3.3/5V	<b>Parity.</b> A single parity bit is provided over AD[31:0] and C/BE[3:0]. This signal should be pulled high through a weak external pull-up resistor.
CLKRUN#	I/O 3.3/5V	<b>CLOCK RUN.</b> An open drain output and also an input. MTXC requests the central resource (PIIX4) to start, or maintain the PCI clock by the assertion of CLKRUN#. MTXC will tri-state CLKRUN# upon negation of reset (since CLK is running upon negation of reset). External pull-up is required. Note: This signal should be connected to the PIIX4 CLKRUN# pin. However, if it is left as a no connect on the MTXC, it must be pulled low through a 100Ω (pull-down resistor).
RST#	I 3.3/5V	<b>Reset.</b> When asserted this signal asynchronously resets the MTXC. The PCI signals also tri-state compliant to PCI Rev 2.0 and 2.1 specifications.

## 2.1.5. TEST AND CLOCK

Name	Type	Description
TEST#	I 3.3/5V	<b>Test In.</b> NAND tree mode is activated by driving this pin low. The test mode selected depends on the state of REQ[3:0]#. This pin should be pulled high with an external pull-up during normal operation.
HCLKIN	I 3.3/2.5V	<b>Host Clock In.</b> This pin receives a buffered host clock. This clock is used by all of the MTXC logic that is in the Host clock domain.
PCLKIN	I 3.3/5V	<b>PCI Clock In.</b> This pin receives a buffered divide-by-2 host clock. This clock is used by all of the MTXC logic that is in the PCI clock domain.

## 2.1.6. POWER MANAGEMENT

Name	Type	Description
SUSCLK	I 3.3V	<b>Suspend Clock.</b> The signal is a 32 KHz input for DRAM refresh circuitry and clocking events in suspend state. The DRAM refresh during suspend and non-suspend states is performed based on this clock. This signal has an internal pull-down resistor.
SUSSTAT1#	I 3.3V	<b>Suspend Status.</b> SUSSTAT1# indicates MTXC's power plane status during suspend mode. SUSSTAT1#, along with SUSCLK and RST#, define the suspend protocol between MTXC and PIIX4. This signal has an internal pull-up resistor.

## 2.1.7. POWER AND GROUND PINS

Name	Type	Description
Vcc	3.3V	<b>Main voltage supply.</b> These pins are the primary voltage supply for the MTXC core and I/O periphery and must be connected to 3.3V.
Vcc (CPU)	3.3V or 2.5V	<b>CPU Interface Voltage Supply.</b> These pins are the primary voltage supply for the MTXC Host periphery and must be connected to either 2.5V or 3.3V, depending on the voltage level of the CPU interface. Refer to the Power sequencing requirements section for additional details.
Vcc (SUS)	3.3V	<b>Suspend Well Voltage Supply.</b> These pins are the primary voltage supply for the MTXC suspend logic and I/O. If suspend to RAM is supported, these pins should be on an isolated power plane; otherwise, they can be connected to the same 3.3V source used for the Vcc pins.
Vcc5REF	3.3V or 5V	<b>Voltage Reference.</b> This pin is tied to 5V through a small external power sequencing circuit, if MTXC signals are required to be 5V Tolerant. In a non 5V tolerant system (i.e. 3.3V only system), this signal can be tied directly to Vcc. Refer to the Power sequencing requirements section for additional details.
Vss	0V	<b>Ground.</b> These pins are the ground for the MTXC.



## 2.2. MTXC Strapping Options

Name	Type	Description
SCS	A[31:30]	<b>Secondary Cache Size.</b> Described in the Cache Control Register bits 7:6.
L2RAMT	A[29:28]	<b>Initial L2 RAM Type.</b> Described in the Cache Control Register bits 5:4.
DRAM Cache	KRQAK	<b>DRAM Cache L2 Present Upon Reset Negation.</b> This bit is sampled to detect DRAM L2 cache. If sampled high, a DRAM Cache is present. A weak pulldown is provided internally. A DRAM cache module should implement a pull-up on this pin that overrides the weak pulldown. BIOS does not have to be aware of this, this information is used by the MTXC to maintain optimal Pburst timings.
25VD	A26	<b>2.5V Voltage Detection.</b> This bit is used to determine the voltage level (3.3V or 2.5V) of the host clock connected to the host clock pin and the voltage on the Vcc(CPU) pins. An external pull-down or pull-up resistor is required on this pin (pulled down for 2.5V and pulled up for 3.3V).
HFD	A27	<b>Frequency Detection.</b> BIOS can use this bit to determine if the system is 60 MHz (external pull-up) or 66 MHz (no strapping is present) as described in the DRTH Register, bit 7. DRTH[bit 7] register is initialized with the inverted value of pin A27 upon reset negation. The A27 input buffer includes a weak pulldown resistor which will force DRTH[bit 7] to default to 1 if no strapping is present.

## 2.3. Power Planes

The MTXC has three primary internal power planes. These power planes permit parts of the MTXC to power down to conserve battery life. Table 1 shows the internal planes and their uses.

Table 1. MTXC Internal Power Planes

Power Plane	Description	Signals Powered	Vcc Pins	GND Pins
SUSPEND	Contains the logic needed to resume from the Suspend-to-RAM state. This power supply should be capable of providing a "trickle" current.  The input signals attached to the SUSPEND power plane Do Not Support 5V Input Levels. These signals must not exceed Vcc (SUS).	MWE#, MWEB#, CKE, RAS[5:0]# <sup>1</sup> , CAS[7:0]#, SUSCLK, SUSSTAT1#	Vcc (SUS)	Vss
CPU	CPU Interface signals have a separate supply so that the CPU interface can be 3.3V for existing CPUs and can be 2.5V on future CPUs.	A[31:3], BE[7:0]#, ADS#, BRDY#, NA#, AHOLD, EADS#, BOFF#, HITM#, M/IO#, D/C#, W/R#, HLOCK#, CACHE#, KEN#/INV, SMIACK#, HD[63:0], HCLKIN	Vcc (CPU)	Vss
Vcc5REF	The Vcc5REF signal provides protection for the 5V tolerant 3.3V signals.	PCI Bus Input and I/O, MD[63:0], TIO[7:0], PCLKIN, TEST#	Vcc5REF	Vss
MAIN	Contains all the rest of the MTXC logic. This plane is powered by the main system power supply.	All Other Signal Pins	Vcc	Vss

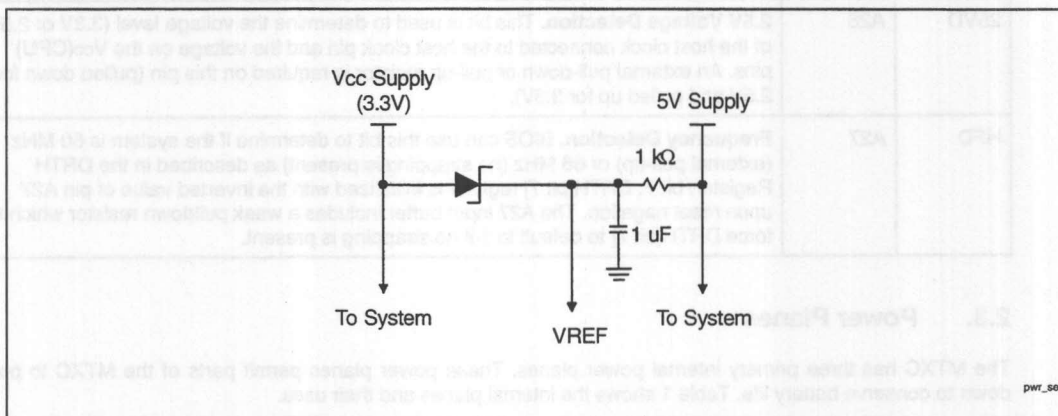
**PRELIMINARY**

**NOTES:**

1. KRQAK is not part of the suspend well. When this pin is used as the 5<sup>th</sup> RAS line (CS4\_64), special considerations must be taken.

**2.4. Power Sequencing Requirements**

The Vcc5REF signal must be tied to 5V in a system requiring 5V tolerance. In a 5V tolerant system, Vcc5REF must power up before or simultaneous to Vcc. It must power down after or simultaneous to Vcc. At any time, Vcc5REF should not be more than 0.6 volts below Vcc. In a non-5V tolerant system (3.3V only), this signal can be tied directly to Vcc. In this case, there are no sequencing requirements. Refer to Figure 2 for an example circuit schematic which may be used to ensure the proper Vcc5REF sequencing.



**Figure 2. Example Vcc5REF Sequencing Circuit**

The Vcc(CPU) power plane is tied to either 2.5 volts or 3.3 volts, depending on the voltage level of the CPU interface. In a system that ties this power plane to 2.5 volts, the Vcc(CPU) pins must power up after or simultaneous to Vcc. It must power down before or simultaneous to Vcc. At any time, Vcc should not be more than 1.2 volts below the Vcc(CPU) plane.

## 2.5. Signal States During And After A Hard Reset

Table 2 shows the state of all the MTCX output and bi-directional signals when RST# is asserted. An undefined state means that the signal is driven either high or low, but not tri-stated.

Table 2. Signal States During/After Reset

Name	State during RST#	State After RST#
A[31:3]	Low	Tri-State
BRDY#	High	High
NA#	High	High
AHOLD	High	Low
EADS#	High	High
BOFF#	High	High
KEN#/INV	Low	Low
HD[63:0]	Tri-State	Tri-State
RAS[5:0]# or CS[5:0]#	Undefined	High
CAS[7:0]# or DQM[7:0]	Undefined	Undefined
MA[11:0], BA1,MA13	Undefined	Undefined
MWE#, MWEB#	High	High
SRAS[A,B]#	High	High
SCAS[A,B]#	High	High
CKE,CKEB	Undefined	High
MD[63:0]	Tri-State	Tri-State
CADV#	High	High
CADS#	High	High

Table 2. Signal States During/After Reset

Name	State during RST#	State After RST#
CCS#	Low	Low
COE#	High	High
GWE#	High	High
BWE#	High	High
TIO[7:0]	Low	Tri-State
TWE#	Low	High
KRQAK	Input	Input
AD[31:0]	Low	Tri-State
C/BE[3:0]#	Low	Tri-State
FRAME#	Tri-State	Tri-State
DEVSEL#	Tri-State	Tri-State
IRDY#	Tri-State	Tri-State
TRDY#	Tri-State	Tri-State
STOP#	Tri-State	Tri-State
LOCK#	Tri-State	Tri-State
GNT[3:0]#	Tri-State	High
PHLDA#	High	High
PAR	Low	Undefined
CLKRUN#	Tri-State	Tri-State



### 3.0. REGISTER DESCRIPTION

The MTXC contains two sets of software accessible registers (I/O Mapped and PCI configuration registers), accessed via the Host CPU I/O address space. The I/O mapped registers control access to PCI configuration space. Configuration registers residing in PCI configuration space used to specify PCI configuration, DRAM configuration, cache configuration, operating parameters and optional system features.

The MTXC internal registers (both I/O Mapped and PCI Configuration registers) are only accessible by the Host CPU and cannot be accessed by PCI masters. The registers can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFADD, which can only be accessed as a DWord. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). The following nomenclature is used for access attributes:

<b>RO</b>	<b>READ ONLY.</b> If a register is read only, writes to this register have no effect.
<b>R/W</b>	<b>READ/WRITE.</b> A register with this attribute can be read and written.
<b>R/WC</b>	<b>READ/WRITE CLEAR.</b> A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.

Some of the MTXC registers described in this section contain reserved bits. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back.

In addition to reserved bits within a register, the MTXC contains address locations in the PCI configuration space that are marked "Reserved" (Table 3). The MTXC responds to accesses to these address locations by completing the Host cycle and returning a value of zero. The registers marked as "Undefined" will return a non-zero value and are defined as read only. Software should not write to reserved or undefined MTXC configuration locations in the device-specific region (above address 3Fh).

Upon RESET, the MTXC sets its internal configuration registers to predetermined **default** states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, cache configuration, operating parameters and optional system features that are applicable, and to program the MTXC registers accordingly.

#### 3.1. I/O Mapped Registers

The MTXC contains three registers that reside in the CPU I/O address space—the Configuration Address (CONFADD) Register, the Configuration Data (CONFDATA) Register, and the PM2 Register Block. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

### 3.1.1. PM2\_CNTRL—PM2 REGISTER BLOCK

I/O Address: 0022h  
Default Value: 00h  
Access: Read/Write

Bit	Descriptions
7:1	<b>Reserved.</b>
0	<b>Arbiter Disable (ARB_DIS).</b> When ARB_DIS=1, the MTXC does not respond to any REQ# signals (including PHOLD#) going active until this bit is set back to 0. This bit is used to disable bus master accesses prior to placing the CPU in a stop clock state. This bit maintains cache coherency by preventing PCI masters from gaining access to the PCI bus and causing snoop cycle activity. MCTL[Bit 6] (offset 79h) must be set to 1 before this register is accessible.

### 3.1.2. CONFADD—CONFIGURATION ADDRESS REGISTER

I/O Address: 0CF8h (Accessed as a DWord)  
Default Value: 00000000h  
Access: Read/Write

CONFADD is a 32-bit register accessed only when referenced as a DWord. A Byte or Word reference will "pass through" the Configuration Address Register onto the PCI bus. The CONFADD register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Descriptions
31	<b>Configuration Enable (CONE).</b> 1=Enable. 0=Disable.
30:24	<b>Reserved.</b>
23:16	<b>Bus Number.</b> When the Bus Number is programmed to 00h the target of the Configuration Cycle is either the MTXC or the PCI Local Bus that is directly connected to the MTXC, depending on the Device Number field. A type 0 Configuration Cycle is generated on PCI if the Bus Number is programmed to 00h and the MTXC is not the target. If the Bus Number is non-zero a type 1 configuration cycle is generated on PCI with the Bus Number mapped to AD[23:16] during the address phase.
15:11	<b>Device Number.</b> This field selects one agent on the PCI bus selected by the Bus Number. During a Type 1 Configuration cycle this field is mapped to AD[15:11]. During a Type 0 Configuration Cycle this field is decoded and one of AD[31:11] is driven to a 1. The MTXC is always Device Number 0.
10:8	<b>Function Number.</b> This field is mapped to AD[10:8] during PCI configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The MTXC responds to configuration cycles with a function number of 000b; all other function number values attempting access to the MTXC (Device Number=0, Bus Number=0) will generate a type 0 configuration cycle onto the PCI bus with no IDSEL asserted, which will result in a master abort.
7:2	<b>Register Number.</b> This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to AD[7:2] during PCI configuration cycles.
1:0	<b>Reserved.</b>

### 3.1.3. CONFDATA—CONFIGURATION DATA REGISTER

I/O Address: 0CFCh  
 Default Value: 00000000h  
 Access: Read/Write

CONFDATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFDATA is determined by the contents of CONFADD.

Bit	Descriptions
31:0	<b>Configuration Data Window (CDW).</b> If bit 31 of CONFADD is 1, any I/O reference that falls in the CONFDATA I/O space is mapped to configuration space using the contents of CONFADD.

## PCI CONFIGURATION SPACE MAPPED REGISTERS

The PCI Bus defines a slot based “configuration space” that allows each device to contain up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space—**Configuration Read** and **Configuration Write**. While memory and I/O spaces are supported by the Pentium microprocessor, configuration space is not supported. The PCI specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The MTCX supports only Mechanism #1. The bus cycles used to access MTCX internal configuration registers are described later in the PCI cycle timings section.

The configuration access mechanism makes use of the CONFADD Register and CONFDATA Register. To reference a configuration register, a DWord I/O write cycle is used to place a value into CONFADD that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFADD[31] must be 1 to enable a configuration cycle. CONFDATA then becomes a window onto four bytes of configuration space specified by the contents of CONFADD. Any read or write to CONFDATA will result in the MTCX translating CONFADD into a PCI configuration cycle.

### Type 0 Access

If the Bus Number field of CONFADD is 0 a Type 0 Configuration cycle is performed on PCI. CONFADD[10:2] is mapped directly to AD[10:2]. The Device Number field of CONFADD is decoded onto AD[31:11]. The MTCX is Device #0 and does not pass its configuration cycles to PCI so AD11 will never be asserted. Device #1 will assert AD12, Device #2 will assert AD13, and so forth up to Device #20 which will assert AD31. Only one AD line is asserted at a time. All device numbers higher than 20 cause a type 0 configuration access with no IDSEL asserted, which will result in a Master Abort.

### Type 1 Access

If the Bus Number field of CONFADD is non-zero a Type 1 Configuration cycle is performed on PCI. CONFADD[23:2] is mapped directly to AD[23:2]. AD[1:0] are driven to 01 to indicate a Type 1 Configuration cycle. All other lines are driven to 0.



Table 3. MTXC Configuration Space

Address Offset	Register Symbol	Register Name	Access
<b>PCI Specific Registers</b>			
00–01h	VID	Vendor Identification	RO
02–03h	DID	Device Identification	RO
04–05h	PCICMD	PCI Command Register	R/W
06–07h	PCISTS	PCI Status Register	RO, R/WC
08	RID	Revision Identification	RO
09–0Bh	CLASSC	Class Code	RO
0Ch	—	Reserved	—
0Dh	MLT	Master Latency Timer	R/W
0Eh	HEDT	Header Type	—
0Fh	BIST	BIST Register	R/W
10–3Fh	—	Reserved	—
<b>MTXC Specific Registers</b>			
40–4Eh	—	Reserved	—
4Fh	ACON	Arbitration Control	R/W
50h	PCON	PCI Control	R/W
51h	—	Reserved	—
52h	CC	Cache Control	R/W
53	CEC	Extended Cache Control	R/W
54–55h	SDRAMC	SDRAM Control	R/W
56h	DRAMEC	DRAM Extended Control	R/W
57h	DRAMC	DRAM Control	R/W
58h	DRAMT	DRAM Timing	R/W
59–5Fh	PAM[6:0]	Programmable Attribute Map (7 registers)	R/W
60–65h	DRB[5:0]	DRAM Row Boundary (6 registers)	R/W
66h	—	Reserved	—
67h	DRTH	DRAM Row Type High	R/W
68h	DRTL	DRAM Row Type Low	R/W

Table 3. MTXC Configuration Space

Address Offset	Register Symbol	Register Name	Access
69–6Ah	—	Undefined	RO
6B–6Fh	—	Reserved	—
70h	MTT	Multi-Transaction Timer	R/W
71h	ESMRAMC	Extended System Management RAM Control	R/W
72h	SMRAMC	System Management RAM Control	R/W
73h	—	Reserved	—
74h	—	Undefined	RO
76–78h	—	Reserved	—
78h	—	Undefined	RO
79	MCTL	Miscellaneous Control Register	R/W
7A–FCh	—	Reserved	—
FDh	—	Undefined	RO
FE–FFh	—	Reserved	—

### 3.1.4. VID—VENDOR IDENTIFICATION REGISTER

Address Offset: 00–01h  
 Default Value: 8086h  
 Attribute: Read Only

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identify any PCI device. Writes to this register have no effect.

Bit	Description
15:0	<b>Vendor Identification Number.</b> This is a 16-bit value assigned to Intel.

### 3.1.5. DID—DEVICE IDENTIFICATION REGISTER

Address Offset: 02–03h  
 Default Value: 7100h  
 Attribute: Read Only

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	<b>Device Identification Number.</b> This is a 16 bit value assigned to the MTXC.

### 3.1.6. PCICMD—PCI COMMAND REGISTER

Address Offset: 04–05h  
 Default: 06h  
 Access: Read/Write

This 16-bit register provides basic control over the MTXC's ability to respond to PCI cycles. The PCICMD Register in the MTXC enables and disables the assertion of SERR# and PCI master accesses to main memory.

Bit	Description
15:10	<b>Reserved.</b>
9	<b>Fast Back-to-Back (FB2B). (Not implemented)</b> This bit is hardwired to 0.
8	<b>SERR# Enable (SERRE). (Not implemented)</b> This bit is hardwired to 0.
7	<b>Address/Data Stepping. (Not implemented)</b> This bit is hardwired to 0.
6	<b>Parity Error Enable (PERRE). (Not implemented)</b> This bit is hardwired to 0.
5	<b>Video Pallet Snooping (VPS). (Not implemented)</b> This bit is hardwired to 0.
4	<b>Memory Write and Invalidate Enable (MWIE). (Not implemented)</b> This bit is hardwired to 0. The MTXC will never use the Memory Write and Invalidate PCI command.
3	<b>Special Cycle Enable (SCE). (Not implemented)</b> This bit is hardwired to 0, as the MTXC does not respond to PCI special cycles.



Bit	Description
2	<b>Bus Master Enable (BME). (Not implemented)</b> This bit is hardwired to 1. The MTXC does not support disabling of its bus master capability on the PCI Bus.
1	<b>Memory Access Enable (MAE).</b> When MAE=1, the MTXC permits PCI masters to access main memory if the PCI address selects enabled DRAM space. When MAE=0, the MTXC does not respond to main memory accesses.
0	<b>I/O Access Enable (IOAE). (Not implemented)</b> The MTXC does not respond to PCI I/O cycles. This bit is hardwired to 0.

### 3.1.7. PCISTS—PCI STATUS REGISTER

Address Offset: 06–07h  
 Default Value: 0200h  
 Access: Read Only, Read/Write Clear

PCISTS is a 16-bit status register that reports the occurrence of a PCI master abort and PCI target abort. PCISTS also indicates the DEVSEL# timing that has been set by the MTXC hardware.

Bit	Description
15	<b>Detected Parity Error (DPE).</b> This bit is hardwired to 0, as PCI received parity checking is not implemented by the MTXC.
14	<b>Signaled System Error (SSE).</b> This bit is hardwired to 0 as MTXC does not support SERR#.
13	<b>Received Master Abort Status (RMAS).</b> When the MTXC terminates a Host-to-PCI transaction (MTXC is a PCI master) with an unexpected master abort, this bit is set to 1. Note that master abort is the normal and expected termination of PCI special cycles. Software resets this bit to 0 by writing a 1 to it.
12	<b>Received Target Abort Status (RTAS).</b> When a MTXC-initiated PCI transaction is terminated with a target abort, RTAS is set to 1. Software resets RTAS to 0 by writing a 1 to it.
11	<b>Signaled Target Abort Status (STAS).</b> This bit is hardwired to 0, as the MTXC never terminates a PCI cycle with a target abort.
10:9	<b>DEVSEL# Timing (DEVT).</b> This 2-bit field indicates the timing of the DEVSEL# signal when the MTXC responds as a target, and is hardwired to the value 01b (medium) to indicate the slowest time that DEVSEL# is generated.
8	<b>Data Parity Detected (DPD).</b> This bit is hardwired to 0, as PERR# is not implemented.
7	<b>Fast Back-to-Back (FB2B).</b> This bit is hardwired to 0, as fast back to back cycle generation is not implemented.
6	<b>User Defined Format (UDF).</b> This bit is hardwired to 0. This is because the MTXC does not contain any configurations that depend on the environment, such as network frequencies.
5	<b>66-MHz PCI Capable (66C).</b> This bit is hardwired to 0. The MTXC does not interface to 66-MHz PCI.
4:0	<b>Reserved.</b>

### 3.1.8. RID—REVISION IDENTIFICATION REGISTER

Address Offset: 08h  
Default Value: 01h  
Access: Read Only

This register contains the revision number of the MTXC. These bits are read only and writes to this register have no effect.

Bit	Description
7:0	<b>Revision Identification Number.</b> This is an 8-bit value that indicates the revision identification number for the MTXC.

### 3.1.9. CLASSC—CLASS CODE REGISTER

Address Offset: 09–0Bh  
Default Value: 00h  
Access: Read Only

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the MTXC. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Description
23:16	<b>Base Class Code (BASEC).</b> 06=Bridge device.
15:8	<b>Sub-Class Code (SCC).</b> 00h=Host Bridge.
7:0	<b>Programming Interface (PI).</b> 00h=Hardwired as a Host-to-PCI Bridge.

### 3.1.10. MLT—MASTER LATENCY TIMER REGISTER

Address Offset: 0Dh  
Default Value: 00h  
Access: Read/Write

MLT is an 8-bit register that controls the amount of time the MTXC, as a bus master, can burst data on the PCI Bus. The Count Value is an 8-bit quantity. However MLT[2:0] are reserved and assumed to 0 when determining the Count Value. MLT is used to guarantee the host CPU a minimum amount of the system resources.

The number of clocks programmed in the MLT represents the guaranteed time slice (measured in PCI clocks) allotted to the MTXC, after which it must surrender the bus as soon as other PCI masters request the bus. The default value of MLT is 00h or 0 PCI clocks.

Bit	Description
7:3	<b>Master Latency Timer Count Value</b>
2:0	<b>Reserved.</b> Read as 0s

### 3.1.11. HEDT—HEADER TYPE REGISTER

Address Offset: 0Eh  
 Default Value: 00h  
 Access: Read Only

This register contains the Header Type of the MTXC. This code is 00h indicating that the MTXC's configuration space map follows the basic format.

Bit	Description
7:0	<b>Device Type (DEVICET).</b> 00h=Indicates a basic configuration space format.

### 3.1.12. BIST—BIST REGISTER

Address Offset: 0Fh  
 Default Value: 00h  
 Access: Read/Write

The Built In Self Test (BIST) function is not supported by the MTXC. Writes to this register have no effect.

Bit	Description
7	<b>BIST Supported.</b> This read only bit is always set to 0, disabling the BIST function. Writes to this bit position have no effect.
6	<b>Start BIST.</b> This function is not supported and writes have no effect.
5:4	<b>Reserved.</b>
3:0	<b>Completion Code.</b> This read only field always returns 0 when read and writes have no effect.

### 3.1.13. ACON—ARBITRATION CONTROL REGISTER

Address Offset: 4Fh  
 Default Value: 00h  
 Access: Read/Write

The ACON Register enables and disables features related to PCI arbitration and PCI 2.1 compliance.

Bit	Description
7	<p><b>Extended CPU-to-PIIX4 PHLDA# Signaling Enable (XPLDE).</b> When XPLDE=1, the MTXC adds the following additional signaling to signal PHLDA# (i.e., in addition to the normal CPU/PIIX4 PHOLD/PHLDA# protocol):</p> <ol style="list-style-type: none"> <li>Whenever the North bridge begins a PCI read/write transaction, it will assert PHLDA# for 1 PCLK within the address phase of the transaction.</li> <li>If the CPU is attempting a LOCKed cycle AND LOCK has been established (i.e. PLOCK# was seen negated in address phase), the PHLDA# remains asserted for one additional clock following the address phase.</li> </ol> <p>This bit should be set to 1 anytime both Passive Release and Delayed Transaction are enabled in the PIIX4. Passive release and delayed transaction are enabled via bits 1 and 0 in PIIX4 register 82h (function 0). When bit 7 in this register is set to 1 (enabled), Bit 7 in PIIX4 Register, 6A (Function 0) must also be set to 1. When enabling these two bits, enable Bit 7 in the PIIX4 first, followed by bit 7 in this register. When disabling these two bits, disable Bit 7 in this register first, followed by bit 7 in the PIIX4.</p>
6:0	<b>Reserved.</b>



### 3.1.14. PCON—PCI CONTROL REGISTER

Address Offset: 50h  
Default Value: 00h  
Access: Read/Write

The PCON Register enables and disables features related to the PCI bus that are not already covered in the required PCI space.

Bit	Description
7:4	Reserved.
3	<b>PCI Concurrency Enable (PCE).</b> 1=CPU can access DRAM and L2 while a non-PIIX4 PCI master is targeting Peer PCI devices. 0 (default)=CPU is held off of the bus during all PCI master cycles. This bit should be set to 1 by BIOS during normal operation.
2:0	Reserved.

### 3.1.15. CC—CACHE CONTROL REGISTER

Address Offset: 52h  
Default Value: SSSS0010 (S=Strapping option)  
Access: Read/Write

This 8-bit register defines the secondary cache operations. The CC register enables and disables the second level cache, adjusts cache size, selects the cache write policy, selects the caching policy when CACHE# is negated on reads, informs the MTXC how the SRAMs are connected, and defines the cache SRAM type. After a hard reset, CC[7:4] reflect the signal levels on the Host address lines A[31:28].

Bit	Description										
7:6	<p><b>Secondary Cache Size (SCS).</b> This field reflects the inverted signal level on the A[31:30] pins at the rising edge of the RESET signal. The options are:</p> <table> <tr> <th>Bits[7:6]</th><th>Secondary Cache Size</th></tr> <tr> <td>00</td><td>Cache not populated</td></tr> <tr> <td>01</td><td>256 Kbytes</td></tr> <tr> <td>10</td><td>512 Kbytes</td></tr> <tr> <td>11</td><td>Reserved</td></tr> </table> <p>The RESET values can be overwritten with subsequent writes to the CC Register.</p> <p style="text-align: center;"><b>NOTE</b></p> <ol style="list-style-type: none"> <li>When bits[7:6]=00, the secondary cache is disabled.</li> <li>When bits[7:6]≠00, the FLCE bit must also be set to 1 (L2 cache cannot be enabled unless the L1 cache is also enabled).</li> </ol>	Bits[7:6]	Secondary Cache Size	00	Cache not populated	01	256 Kbytes	10	512 Kbytes	11	Reserved
Bits[7:6]	Secondary Cache Size										
00	Cache not populated										
01	256 Kbytes										
10	512 Kbytes										
11	Reserved										

Bit	Description															
5:4	<p><b>L2 SRAM Type (L2SRAMT).</b> This field reflects the inverted signal level on the A[29:28] pins at the rising edge of the RESET signal. The RESET values can be overwritten with subsequent writes to the CC Register. The options are:</p> <table><tr><th>Bits[5:4]</th><th>SRAM Type</th></tr><tr><td>00</td><td>Pipelined Burst SRAM</td></tr><tr><td>01</td><td>Reserved</td></tr><tr><td>10</td><td>Reserved</td></tr><tr><td>11</td><td>Two banks of Pipelined Burst</td></tr></table> <p style="text-align: center;"><b>NOTE</b></p> <p>When 512-KB Pipelined Burst SRAM L2 mode is selected (via SCS and SRAMT), CCS# is negated after NA# is asserted, and reasserted after a pipelined ADS# is detected. CADS# is asserted along with the final BRDY# for a cycle if a pipelined cycle is outstanding (i.e., an ADS# was detected).</p>	Bits[5:4]	SRAM Type	00	Pipelined Burst SRAM	01	Reserved	10	Reserved	11	Two banks of Pipelined Burst					
Bits[5:4]	SRAM Type															
00	Pipelined Burst SRAM															
01	Reserved															
10	Reserved															
11	Two banks of Pipelined Burst															
3	<p><b>NA Disable (NAD).</b> 1=Disable. 0=Enable. When disabled, MTXC never asserts the NA# pin. When enabled, NA# assertion is dependent on the cache type and size selected (via SRAMT, SCS). Note that NAD must be set to 1 if the NA# pin of the MTXC is not connected to the processor. This bit should be set to 0 for normal operation in systems that connect NA# to the processor.</p>															
2	<p><b>Reserved.</b></p>															
1	<p><b>Secondary Cache Force Miss or Invalidate (SCFMI).</b> When set to a 1, the L2 hit/miss detection is disabled, and all tag lookups result in a miss. If the L2 is enabled, then the cycle is processed as a miss (as described in Chapter 4.2). If the L2 is populated but disabled (FLCE=0), then when SCFMI is set to a 1, any CPU read cycle will invalidate the selected tag entry. When SCFMI is set to a 0, normal L2 cache hit/miss detection and cycle processing occurs.</p> <p>Software can flush the cache (cause all modified lines to be written back to DRAM) by setting SCFMI to a 1 with the L2 enabled (non-zero SCS, FLCE=1), and reading all L2 cache tag address locations. See FLCE bit description for FLCE/SCFMI interaction.</p>															
0	<p><b>First Level Cache Enable (FLCE).</b> 1=Enable. 0=Disable. When FLCE=1, the MTXC responds to CPU cycles with KEN# asserted for cacheable memory cycles. When FLCE=0, KEN# is always negated. This prevents new cache line fills to either the first level or second level cache.</p> <p>The FLCE/SCFMI interaction is summarized below. Note that “Normal L2 operation” is further dependent on the SCS field programming.</p> <table><tr><th>FLCE</th><th>SCFMI</th><th>L2 Result</th></tr><tr><td>0</td><td>0</td><td>L2 disabled</td></tr><tr><td>0</td><td>1</td><td>L2 disabled, MTXC tag invalidate on reads</td></tr><tr><td>1</td><td>0</td><td>Normal L2 operation (dependent on SCS)</td></tr><tr><td>1</td><td>1</td><td>L2 enabled, MTXC miss forced on reads/writes (Note that writes to the cache are also forced as misses, making it possible to create incoherent DRAM/L2 data.)</td></tr></table>	FLCE	SCFMI	L2 Result	0	0	L2 disabled	0	1	L2 disabled, MTXC tag invalidate on reads	1	0	Normal L2 operation (dependent on SCS)	1	1	L2 enabled, MTXC miss forced on reads/writes (Note that writes to the cache are also forced as misses, making it possible to create incoherent DRAM/L2 data.)
FLCE	SCFMI	L2 Result														
0	0	L2 disabled														
0	1	L2 disabled, MTXC tag invalidate on reads														
1	0	Normal L2 operation (dependent on SCS)														
1	1	L2 enabled, MTXC miss forced on reads/writes (Note that writes to the cache are also forced as misses, making it possible to create incoherent DRAM/L2 data.)														

### 3.1.16. CEC—EXTENDED CACHE CONTROL REGISTER

Address Offset: 53h  
Default Value: 14h  
Access: Read/Write, Read Only

This 8-bit register defines the refresh rate (in HCLKs) for a DRAM CACHE L2 cache implementation, if enabled.

Bit	Description
7:6	<b>Reserved</b>
5	<b>DRAM CACHE L2 Present (ML2)—RO.</b> When ML2=1, an L2 DRAM CACHE is present.
4:0	<b>DRAM Cache L2 Refresh Timer (MCRT)—R/W.</b> These bits determine the time the MTXC remains idle during a DRAM cache refresh sequence. The smallest value for the MCRT must be 04h; otherwise, the MTXC will not function properly. The default value sets the timer refresh to 20 HCLKs.

### 3.1.17. SDRAMC—SDRAM CONTROL REGISTER

Address Offset: 54–55h  
Default Value: 0000h  
Access: Read/Write

Bit	Description
15:9	<b>Reserved.</b>
8:6	<p><b>Special SDRAM Mode Select (SSMS).</b> These bits select 1 of 4 special SDRAM modes for testing and initialization. Note that the NOP command must be programmed first before any other command can be issued. After the DRAM detection process has completed, bits[7:5] must remain at “000” during normal DRAM operation.</p> <p><b>Bits[8:6] Mode</b></p> <p>000 <b>Normal SDRAM mode (default).</b></p> <p>001 <b>NOP Command Enable (NOPCE).</b> This mode forces all CPU cycles to DRAM to generate a SDRAM NOP command on the memory interface.</p> <p>010 <b>All Banks Precharge Command Enable (ABPCE).</b> This setting enables a mode where all CPU cycles to DRAM are converted to an all banks precharge command on the memory interface. Used for BIOS Detection algorithm.</p> <p>011 <b>Mode Register Command Enable (MRCE).</b> This setting enables a mode where all CPU cycles to DRAM are converted into MRS commands to the memory interface. The command is driven on the MA[11:0] lines. MA[2:0] needs to be always driven to 010 for burst of 4 mode. MA3 needs to be always driven to 1 for interleave wrap type mode. MA4 needs to be driven to the value in the CAS# Latency bit. MA[6:5] needs to be always driven to 01. MA[11:7] needs to be always driven to 00000.</p> <p>The BIOS will select an appropriate host address for each Row of memory such that the right commands are generated on the Memory Address MA[11:0] lines. The BIOS needs to be cognizant of the mapping of the Host addresses to Memory addresses. e.g. A Host address of 1D0h will set up the Mode registers in Row 0 of SDRAM with Burst length of 4, Wrap type of interleaved, and CAS latency of 3.</p> <p>100 <b>CBR Cycle Enable (CBRC).</b> This setting enables a mode where all CPU cycles to DRAM are converted to SDRAM CBR refresh cycles on the memory interface.</p> <p>101 <b>Reserved</b></p> <p>11X <b>Reserved</b></p>



Bit	Description												
5	<b>RAS# to CAS# Override (RCO).</b> When set to 1, and the CL bit (CAS Latency) is 0 (CAS Latency=3), then a RAS# to CAS# delay of 2 HCLKs is provided for SDRAM. When set to 0, a RAS# to CAS# delay for SDRAM is determined by the CL bit.												
4	<b>CAS# Latency (CL).</b> When set to 1, a CAS# latency of 2 is used for all SDRAM cycles. When reset to 0, CAS# latency of 3 is used for all SDRAM cycles.												
3	<b>RAS# Timing (RT).</b> This bit controls RAS# precharge, RAS# active to precharge time and Refresh to RAS# active delay (in HCLKs): <table><tr><th>Bit 3</th><th>RAS# Precharge</th><th>RAS# act. to Precharge</th><th>Refresh to RAS# act.</th></tr><tr><td>0</td><td>3</td><td>5</td><td>8</td></tr><tr><td>1</td><td>3</td><td>4</td><td>7</td></tr></table>	Bit 3	RAS# Precharge	RAS# act. to Precharge	Refresh to RAS# act.	0	3	5	8	1	3	4	7
Bit 3	RAS# Precharge	RAS# act. to Precharge	Refresh to RAS# act.										
0	3	5	8										
1	3	4	7										
2	<b>Reserved.</b>												
1	<b>64-Mbit Technology Enable (64MTEN).</b> 1=Enable. 0=Disable. When set to 0, the MTXC does not support 64-Mbit SDRAM devices. In this mode, the MTXC supports 4-Mbit, 16-Mbit, and 64-Mbit technology for EDO/FPM systems and 4 Mbit and 16 Mbit for SDRAM systems (i.e., 64 Mbit not supported in SDRAM systems). When set to 1, the MTXC supports 4 Mbit, 16 Mbit, and 64 Mbit for both SDRAM and EDO/FPM devices. In this mode, the RAS#/CS5# signal becomes RAS#/CS5#/MA13, RAS4#/CS4# becomes RAS4#/CS4#/BA1, and KRQAK/CS4_64# becomes CS4_64#. CS4_64# (fifth row) function is provided if this signal is set to 1 and DRAM Cache is not present in the system (indicated by a 0 in bit 5, register 53h).												
0	<b>Reserved.</b>												

Table 4 lists the CAS# Latency, RAS# to CAS#, RAS# Precharge, RAS# Active to Precharge and Refresh to RAS# active programmable timings.

Table 4. Programming Timings

Operating Frequency	CAS Latency (CL)	RAS# to CAS# (Trcd)	RAS# Precharge (Trp)	RAS# active to Precharge (Tras)	Refresh to RAS# (Trc)	Register 54h Bits[5:3]
60/66 MHz	3 HCLKs	3 HCLKs	3 HCLKs	5 HCLKs	8 HCLKs	000
60/66 MHz	3 HCLKs	2 HCLKs	3 HCLKs	5 HCLKs	8 HCLKs	100
60/66 MHz	2 HCLKs	2 HCLKs	3 HCLKs	4 HCLKs	7 HCLKs	011

### 3.1.18. DRAMEC—DRAM EXTENDED CONTROL REGISTER

Address Offset: 56h  
Default Value: 52h  
Access: Read/Write

This 8-bit register contains additional controls for main memory DRAM operating modes and features.

Bit	Description																											
7	Reserved.																											
6	<b>Refresh RAS# Assertion(RRA).</b> 1=5 clocks (RAS# asserted for Refresh cycles). 0=4 clocks.																											
5	<b>Fast EDO Lead Off (FELO).</b> 1=Enables fast timing EDO read cycles. 0=Disable. This is valid for EDO DRAMs only (in both a synchronous cache and a Cacheless system). This results in a 1 HCLK pull-in for all read leadoff latencies for EDO DRAMs. (i.e., Page hits, Page misses, and Row Misses). This bit must be 0 if any of the DRAM rows is populated with FPM DRAMs.																											
4	<b>Speculative Lead Off (SLD).</b> If set to 0, the DRAM Controller read request is presented before the final memory target (Cache/DRAM/PCI) has been decoded by the MTXC. This results in a 1 HCLK pull-in for all read leadoff latencies. Note that if the cycle does not actually target DRAM, the DRAM cycle is later terminated. The SLD bit applies to EDO/FPM and SDRAM. This bit should be set to 1 in systems with a L2 cache and to 0 for systems without a L2 cache																											
3	Reserved.																											
2:1	<p><b>Memory Address Drive Strength (MAD).</b> This field controls the strength of the output buffers driving the MA, SRASx#, SCASx#, MWEx# and CKEx pins. It is recommended that series termination or undershoot and overshoot diodes be used on these lines.</p> <table><tr><th>Bit[2:1]</th><th>MA[13,11:0], BA1</th><th>SRAS[A,B],SCAS[A,B], MWEx#, CKEx</th></tr><tr><td>00</td><td>10 mA</td><td>10 mA</td></tr><tr><td>01</td><td>10 mA</td><td>16 mA</td></tr><tr><td>10</td><td>16 mA</td><td>10 mA</td></tr><tr><td>11</td><td>16 mA</td><td>16 mA</td></tr></table> <p>Setting Memory Address Drive Strength:</p> <table><tr><th>1 Row</th><th>2 Row</th><th>3 Row</th><th>4 Row</th><th>5 Row</th><th>6 Row</th></tr><tr><td>00</td><td>00</td><td>11</td><td>11</td><td>11</td><td>01*</td></tr></table> <p>* Assuming All Rows are buffered</p>	Bit[2:1]	MA[13,11:0], BA1	SRAS[A,B],SCAS[A,B], MWEx#, CKEx	00	10 mA	10 mA	01	10 mA	16 mA	10	16 mA	10 mA	11	16 mA	16 mA	1 Row	2 Row	3 Row	4 Row	5 Row	6 Row	00	00	11	11	11	01*
Bit[2:1]	MA[13,11:0], BA1	SRAS[A,B],SCAS[A,B], MWEx#, CKEx																										
00	10 mA	10 mA																										
01	10 mA	16 mA																										
10	16 mA	10 mA																										
11	16 mA	16 mA																										
1 Row	2 Row	3 Row	4 Row	5 Row	6 Row																							
00	00	11	11	11	01*																							
0	Reserved.																											

## 3.1.19. DRAMC—DRAM CONTROL REGISTER

Address Offset: 57h  
 Default Value: 01h  
 Access: Read/Write

This 8-bit register controls main memory DRAM operating modes and features.

Bit	Description																
7:6	<p><b>Hole Enable (HEN).</b> This field enables a memory hole in DRAM space. CPU cycles matching an enabled hole are passed on to PCI. PCI cycles matching an enabled hole will be ignored by the MTXC (no DEVSEL#). Note that a selected hole is not remapped.</p> <p><b>Bits[7:6] Hole Enabled</b></p> <table> <tr> <td>00</td><td>None</td></tr> <tr> <td>01</td><td>512 KB–640 KB (128 Kbytes)</td></tr> <tr> <td>10</td><td>15 MB–16 MB (1 Mbyte)</td></tr> <tr> <td>11</td><td>14 MB–16 MB (2 Mbytes)</td></tr> </table>	00	None	01	512 KB–640 KB (128 Kbytes)	10	15 MB–16 MB (1 Mbyte)	11	14 MB–16 MB (2 Mbytes)								
00	None																
01	512 KB–640 KB (128 Kbytes)																
10	15 MB–16 MB (1 Mbyte)																
11	14 MB–16 MB (2 Mbytes)																
5	<b>Reserved.</b>																
4	<p><b>Enhanced Paging Disable (EPD).</b> 1=MTXC keeps page open until a page/row miss. When EPD=0, the MTXC uses additional information to keep the DRAM page open when the host may be “right back”. See DRAM section for additional information. This bit should be set to 0 for normal operation.</p>																
3	<p><b>EDO Detect Mode Enable (EDME).</b> 1=Enables a special timing mode for BIOS to detect EDO DRAM type on a bank-by-bank basis. Once all DRAM row banks have been tested for EDO, the EDME bit should be set to 0. Otherwise, performance will be seriously impacted.</p>																
2:0	<p><b>DRAM Refresh Rate (DRR).</b> The DRAM refresh rate for “FPM/EDO only” DRAM subsystem is adjusted according to the value selected by this field. DRAM refresh is implemented using SUSCLK.</p> <p><b>Bits[2:0] DRAM Refresh Rate</b></p> <table> <tr> <td>000</td><td>Refresh Disabled (results in the eventual loss of DRAM data)</td></tr> <tr> <td>001</td><td>15.6 <math>\mu</math>s</td></tr> <tr> <td>010</td><td>31.2 <math>\mu</math>s (for EDO/FPM only memory subsystem)</td></tr> <tr> <td>011</td><td>64.4 <math>\mu</math>s (for EDO/FPM only memory subsystem)</td></tr> <tr> <td>100</td><td>125 <math>\mu</math>s (for EDO/FPM only memory subsystem)</td></tr> <tr> <td>101</td><td>256 <math>\mu</math>s (for EDO/FPM only memory subsystem)</td></tr> <tr> <td>110</td><td>Reserved</td></tr> <tr> <td>111</td><td>Reserved</td></tr> </table> <p style="text-align: center;"><b>NOTES</b></p> <ol style="list-style-type: none"> <li>1. If any of the row is populated with SDRAMs, this field must be set to 15.6 <math>\mu</math>s refresh rate.</li> <li>2. Selecting refresh rate of 125 <math>\mu</math>s or 256 <math>\mu</math>s may violate the max RAS# active time DRAM specification. It is up to the system designer to make sure this does not happen.</li> </ol>	000	Refresh Disabled (results in the eventual loss of DRAM data)	001	15.6 $\mu$ s	010	31.2 $\mu$ s (for EDO/FPM only memory subsystem)	011	64.4 $\mu$ s (for EDO/FPM only memory subsystem)	100	125 $\mu$ s (for EDO/FPM only memory subsystem)	101	256 $\mu$ s (for EDO/FPM only memory subsystem)	110	Reserved	111	Reserved
000	Refresh Disabled (results in the eventual loss of DRAM data)																
001	15.6 $\mu$ s																
010	31.2 $\mu$ s (for EDO/FPM only memory subsystem)																
011	64.4 $\mu$ s (for EDO/FPM only memory subsystem)																
100	125 $\mu$ s (for EDO/FPM only memory subsystem)																
101	256 $\mu$ s (for EDO/FPM only memory subsystem)																
110	Reserved																
111	Reserved																



### 3.1.20. DRAMT—DRAM TIMING REGISTER

Address Offset: 58h  
Default Value: 00h  
Access: Read/Write

This 8-bit register controls main memory DRAM timings. For SDRAM specific timing control, see the SDRAMC timing register definition.

Bit	Description															
7	<b>Reserved.</b>															
6:5	<p><b>DRAM Read Burst Timing (DRBT).</b> The DRAM read burst timings are controlled by the DRBT field. Slower rates may be required in certain system designs to support loose layouts or slower memories. Most system designs will be able to use one of the faster burst mode timings. The timing used depends on the type of DRAM on a per-bank basis, as indicated by the DRT register.</p> <p>The x322 timings for EDO Burst rate should be used only when the Fast EDO Path Select (FEPS) bit is set to 1 and the timings for the EDO Burst rate for X222 have a negative margin. This forces the MXS to be negated after the leadoff; thus, selecting the fast path for the leadoff and the slow path for the burst cycles.</p> <p>When FEPS=1 and the EDO Burst rate is set to x222, the EDO read cycle is selected through the fast path for both leadoff and the burst cycles.</p> <p>When FEPS=0 and the EDO Burst rate is set to x222, the EDO read cycle is selected through the slow path for both leadoff and the burst cycles.</p> <table><tr><th>DRBT</th><th>EDO Burst Rate</th><th>FPM Burst Rate</th></tr><tr><td>00</td><td>x444</td><td>x444</td></tr><tr><td>01</td><td>x333</td><td>x444</td></tr><tr><td>10</td><td>x222</td><td>x333</td></tr><tr><td>11</td><td>Reserved</td><td>Reserved</td></tr></table>	DRBT	EDO Burst Rate	FPM Burst Rate	00	x444	x444	01	x333	x444	10	x222	x333	11	Reserved	Reserved
DRBT	EDO Burst Rate	FPM Burst Rate														
00	x444	x444														
01	x333	x444														
10	x222	x333														
11	Reserved	Reserved														
4:3	<p><b>DRAM Write Burst Timing (DWBT).</b> The DRAM write burst timings are controlled by the DWBT field. Slower rates may be required in certain system designs to support loose layouts or slower memories. Most system designs will be able to use one of the faster burst mode timings.</p> <table><tr><th>DWBT</th><th>EDO/FPM Burst Rate</th><th>DWBT</th><th>EDO/FPM Burst Rate</th></tr><tr><td>00</td><td>x444</td><td>10</td><td>x222</td></tr><tr><td>01</td><td>x333</td><td>11</td><td>Reserved</td></tr></table>	DWBT	EDO/FPM Burst Rate	DWBT	EDO/FPM Burst Rate	00	x444	10	x222	01	x333	11	Reserved			
DWBT	EDO/FPM Burst Rate	DWBT	EDO/FPM Burst Rate													
00	x444	10	x222													
01	x333	11	Reserved													
2	<b>Reserved.</b>															

Bit	Description																												
1:0	<p><b>DRAM Leadoff Timing (DLT).</b> The DRAM leadoff timings are controlled by the DLT bits. Slower leadoffs may be required in certain system designs to support loose layouts or slower memories. The Row Miss leadoff timings are summarized below for EDO/FPM reads and writes.</p> <p>Changing DLT affects the Row Miss and Page Miss timings only (e.g., DLT=01 is one clock faster than DLT=00 on Row Miss and Page Miss timings). These bit control MA setup to CAS# assertion.</p> <p>DLT does not affect page hit timings. Thus, DLT=00 or DLT=01 has same page hit timings for reads and writes (e.g., for reads, it would be 10-3=7 clocks for DLT=00 or DLT=01)</p> <table> <tr> <th>DLT</th><th>Read Leadoff</th><th>Write Leadoff</th><th>RAS# Precharge</th><th>RAS-to-CAS Delay</th></tr> <tr> <td>00</td><td>11</td><td>7</td><td>3</td><td>4</td></tr> <tr> <td>01</td><td>10</td><td>6</td><td>3</td><td>3</td></tr> <tr> <td>10</td><td>11</td><td>7</td><td>4</td><td>4</td></tr> <tr> <td>11</td><td>10</td><td>6</td><td>4</td><td>3</td></tr> </table> <p>SLD and FELO bits have cumulative effect on the leadoff timings. The above leadoff represent timings with SLD=1 and FELO=0.</p>				DLT	Read Leadoff	Write Leadoff	RAS# Precharge	RAS-to-CAS Delay	00	11	7	3	4	01	10	6	3	3	10	11	7	4	4	11	10	6	4	3
DLT	Read Leadoff	Write Leadoff	RAS# Precharge	RAS-to-CAS Delay																									
00	11	7	3	4																									
01	10	6	3	3																									
10	11	7	4	4																									
11	10	6	4	3																									

### 3.1.21. PAM—PROGRAMMABLE ATTRIBUTE MAP REGISTERS (PAM[6:0])

Address Offset: 59h (PAM0) (5Fh (PAM6))  
 Default Value: 00h  
 Attribute: Read/Write  
 Size: 8 bits (each register)

The MTCX allows programmable memory and cacheability attributes on 14 memory segments of various sizes in the 640-Kbytes to 1-Mbyte address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Three bits are used to specify L1 cacheability and memory attributes for each memory segment. These attributes are:

- RE Read Enable.** When RE=1, the CPU read accesses to the corresponding memory segment are directed to main memory. Conversely, when RE=0, the CPU read accesses are directed to PCI.
- WE Write Enable.** When WE=1, the CPU write accesses to the corresponding memory segment are directed to main memory. Conversely, when WE=0, the CPU write accesses are directed to PCI.
- CE Cache Enable.** When CE=1, the corresponding memory segment is L1 cacheable. CE must not be set to 1 when RE is reset to 0 for any particular memory segment. When CE=1 and WE=0, the corresponding memory segment is cached in the first level cache only on CPU code read cycles.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only. The characteristics for memory segments with these read/write attributes are described in Table 5.

Table 5. Attribute Definition

Read/Write Attribute	Definition
Read Only	Read cycles: CPU cycles are serviced by the DRAM in a normal manner. Write cycles: CPU initiated write cycles are ignored by the DRAM interface as well as the cache. Instead, the cycles are passed to PCI for termination. Areas marked as Read Only are L1 cacheable for Code accesses only. These regions are not cached in the second level cache.
Write Only	Read cycles: All read cycles are ignored by the DRAM interface as well as the second level cache. CPU-initiated read cycles are passed onto PCI for termination. The write only state can be used while copying the contents of a ROM, accessible on PCI, to main memory for shadowing, as in the case of BIOS shadowing. Write cycles: CPU write cycles are serviced by the DRAM and L2 cache in a normal manner.
Read/Write	This is the normal operating mode of main memory. Both read and write cycles from the CPU and PCI are serviced by the DRAM and L2 cache interface.
Disabled	All read and write cycles to this area are ignored by the DRAM and cache interface. These cycles are forwarded to PCI for termination.

Each PAM Register controls two regions, typically 16 Kbytes in size. Each of these regions has a 4-bit field. The four bits that control each region have the same encoding and are defined in Table 6.

PCI master access to DRAM space is also controlled by the PAM Registers. If the PAM programming indicates a region is writeable, then PCI master writes will be accepted (DEVSEL# generated). If the PAM programming indicates a region is readable, PCI master reads will be accepted. If a PCI write to a non-writeable DRAM region, or a PCI read to a non-readable DRAM region is seen, the MTXC will not accept the cycle (DEVSEL# will not be asserted). PCI master accesses to enable memory hole regions will not be accepted.

Table 6. Attribute Bit Assignment

Bits [7, 3] Reserved	Bits [6, 2] Cache Enable	Bits [5, 1] Write Enable	Bits [4, 0] Read Enable	Description
x	x	0	0	DRAM disabled, accesses directed to PCI
x	0	0	1	read only, DRAM write protected, non-cacheable
x	1	0	1	read only, DRAM write protected, L1 cacheable for code accesses only
x	0	1	0	write only
x	0	1	1	read/write, non-cacheable
x	1	1	1	read/write, cacheable

As an example, consider a BIOS that is implemented on the expansion bus. During the initialization process the BIOS can be shadowed in main memory to increase the system performance. When a BIOS is shadowed in main memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The CPU then does a write of the same address, which is directed to main



memory. After the BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus.

**Table 7. PAM Register and Associated Memory Segments**

PAM Reg.	Attribute Bits				Memory Segment	Comments	Offset
PAM0[3:0]	Reserved						59h
PAM0[7:4]	R	CE	WE	RE	0F0000h – 0FFFFFFh	BIOS Area	59h
PAM1[3:0]	R	CE	WE	RE	0C0000h – 0C3FFFh	ISA Add-on BIOS	5Ah
PAM1[7:4]	R	CE	WE	RE	0C4000h – 0C7FFFh	ISA Add-on BIOS	5Ah
PAM2[3:0]	R	CE	WE	RE	0C8000h – 0CBFFFh	ISA Add-on BIOS	5Bh
PAM2[7:4]	R	CE	WE	RE	0CC000h – 0CFFFFh	ISA Add-on BIOS	5Bh
PAM3[3:0]	R	CE	WE	RE	0D0000h – 0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	CE	WE	RE	0D4000h – 0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	CE	WE	RE	0D8000h – 0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	CE	WE	RE	0DC000h – 0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	CE	WE	RE	0E0000h – 0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	CE	WE	RE	0E4000h – 0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	CE	WE	RE	0E8000h – 0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	CE	WE	RE	0EC000h – 0EFFFFh	BIOS Extension	5Fh

**NOTES:**

The CE bit should not be changed while the L2 cache is enabled.

Attribute	Bit (0)	Bit (1)	Bit (2)	Bit (3)
Read-only, non-cacheable	0	0	0	0
Read-only, cacheable	1	0	0	0
Write-only, non-cacheable	0	1	0	0
Write-only, cacheable	1	1	0	0
Read/write, non-cacheable	0	0	1	0
Read/write, cacheable	1	0	1	0

#### DOS Application Area (00000h–9FFFh)

Read, write, and cacheability attributes are always enabled and are not programmable for the 0–640-Kbytes DOS application region.

#### Video Buffer Area (A0000h–BFFFFh)

This 128-Kbytes area is not controlled by attribute bits. CPU-initiated cycles in this region are always forwarded to PCI for termination. This area is not cacheable.

#### Expansion Area (C0000h–DFFFFh)

This 128-Kbytes area is divided into eight 16-Kbytes segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled Memory that is disabled is not remapped. Cacheability status can also be specified for each segment.

#### Extended System BIOS Area (E0000h–EFFFFh)

This 64-Kbytes area is divided into four 16-Kbytes segments. Each segment can be assigned independent cacheability, read, and write attributes. Memory segments that are disabled are not remapped elsewhere.

#### System BIOS Area (F0000h–FFFFFh)

This area is a single 64-Kbytes segment. This segment can be assigned cacheability, read, and write attributes. When disabled, this segment is not remapped.

#### Extended Memory Area (100000h–FFFFFFFh)

The extended memory area can be split into several parts:

- Flash BIOS area from 4 Gbytes to 4 Gbytes–512 Kbytes (aliased on ISA at 16 Mbytes–15.5 Mbytes)
- DRAM Memory from 1 Mbytes to a maximum of 512 Mbytes
- PCI Memory space from the top of DRAM to 4 Gbytes–512 Kbytes

On power-up or reset the CPU vectors to the Flash BIOS area, mapped in the range of 4 Gbytes to 4 Gbytes–512 Kbytes. This area is physically mapped on the expansion bus. Since these addresses are in the upper 4-Gbytes range, the request is directed to PCI.

The DRAM memory space can occupy extended memory from a minimum of 1 Mbytes up to 256 Mbytes. This memory is cacheable.

PCI memory space from the top of main memory to 4 Gbytes is always non-cacheable.

### 3.1.22. DRB—DRAM ROW BOUNDARY REGISTERS

Address Offset: 60–65h  
 Default Value: 02h  
 Access: Read/Write

The MTXC supports 6 rows of DRAM. Each row is 64-bits wide. The DRAM Row Boundary Registers define upper and lower addresses for each DRAM row. Contents of these 8-bit registers represent the boundary addresses in 4-Mbytes granularity.

DRB0=Total amount of memory in row 0 (in 4 Mbytes)  
 DRB1=Total amount of memory in row 0 + row 1 (in 4 Mbytes)  
 DRB2=Total amount of memory in row 0 + row 1 + row 2 (in 4 Mbytes)  
 DRB3=Total amount of memory in row 0 + row 1 + row 2 + row 3 (in 4 Mbytes)  
 DRB4=Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 (in 4 Mbytes)  
 DRB5=Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 (in 4 Mbytes)

The DRAM array can be configured with 512-KB, 1-MB, 4-MB, or 16-MB deep by 32- or 36-bit wide SIMMs. Each register defines an address range that will cause a particular RAS# line to be asserted (e.g., if the first DRAM row is 8 Mbytes, accesses within the 0 to 8-Mbytes range will cause RAS0# to be asserted).

#### NOTE

When programming the DRB registers, the following programming consideration must be followed: When DRB3 is written, DRB4 and DRB5 are also modified with the value written into DRB3. When DRB4 is written, DRB5 is also modified with the value written into DRB4. To avoid data corruption in the DRB4 and DRB5 registers, program DRB3 first, followed by DRB4 and then DRB5. If either DRB3 or DRB4 are written, this sequence should be followed.

Bit	Description
7	Reserved.
6:0	<b>Row Boundary Address.</b> This 7-bit value is compared against the address lines A[28:22] to determine the upper address limit of a particular row (i.e., DRB minus previous DRB=row size).

#### Row Boundary Address

These 8 bit values represent the upper address limits of the 6 rows (i.e., this row minus previous row=row size). Unpopulated rows have a value equal to the previous row (row size=0). DRB5 reflects the maximum amount of DRAM in the system. The top of memory is determined by the value written into DRB5. If DRB5 is greater than 256 Mbytes, then 256 Mbytes of DRAM are available. BIOS must make sure that the DRB registers do not reflect more than 256M of Main memory.

As an example of a general purpose configuration where 3 physical rows are configured for either single-sided or double-sided SIMMs, the memory array would be configured like the one shown in Figure 3. In this configuration, the MTXC drives two RAS# signals directly to the SIMM rows. If single-sided SIMMs are populated, the even RAS# signal is used and the odd RAS# is not connected. If double-sided SIMMs are used, both RAS# signals are used.



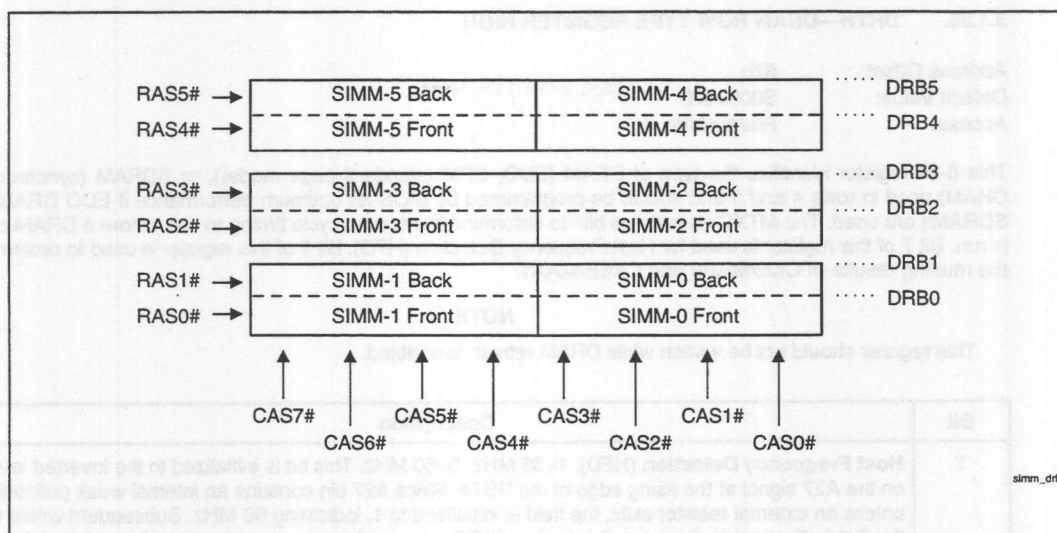


Figure 3. SIMMs and Corresponding DRB Registers

The following 2 examples describe how the DRB Registers are programmed for cases of single-sided and double-sided SIMMs on a motherboard having a total of four 8-byte or eight 4-byte SIMM sockets.

#### Example #1

The memory array is populated with four single-sided 1 MB x 32 SIMMs, a total of 16 MBytes of DRAM. Two SIMMs are required for each populated row making each populated row 8 Mbytes in size.

DRB0=02h	populated (2 SIMMs, 8 Mbytes this row)
DRB1=04h	populated (2 SIMMs, 8 Mbytes this row)
DRB2=04h	empty row
DRB3=04h	empty row
DRB4=04h	empty row
DRB5=04h	empty row

#### Example #2

As an another example, the memory array is populated with two 2 Mbytes x 32 double-sided SIMMs (one row), and four 4 Mbytes x 32 single-sided SIMMs (two rows), yielding a total of 96 Mbytes of DRAM. The DRB Registers are programmed as follows:

DRB0=04h	populated with 16 Mbytes, 1/2 of double-sided SIMMs
DRB1=08h	the other 16 Mbytes of the double-sided SIMMs
DRB2=10h	populated with 32 Mbytes, one of the sided SIMMs
DRB3=18h	the other 32 Mbytes of single-sided SIMMs
DRB4=18h	empty row
DRB5=18h	empty row

**3.1.23. DRTH—DRAM ROW TYPE REGISTER HIGH**

Address Offset: 67h  
 Default Value: S0000000  
 Access: Read/Write

This 8-bit register identifies the type of DRAM (EDO, SPM (standard page mode)), or SDRAM (synchronous DRAM) used in rows 4 and 5 and should be programmed by BIOS for optimum performance if EDO DRAMs or SDRAMs are used. The MTXC uses these bits to determine the correct cycle timing to use before a DRAM cycle is run. Bit 7 of this register is used for Host Frequency Detection (HFD). Bit 2 of this register is used to determine the muxing results of CKE/MAA0 and CKEB/MAA1.

**NOTE**

This register should not be written while DRAM refresh is enabled.

Bit	Description																
7	<b>Host Frequency Detection (HFD).</b> 1=66 MHz. 0=60 MHz. This bit is initialized to the inverted level on the A27 signal at the rising edge of the RST#. Since A27 pin contains an internal weak pulldown, unless an external resistor exists, the field is initialized to 1, indicating 66 MHz. Subsequent writes to this field will override the reset strap value. BIOS can use the value to determine if the system is 60 MHz (external pull-up) or 66 MHz (no strapping).																
5:4, 1:0	<p><b>DRAM Row Type (DRT).</b> The DRT bits select the DRAM type installed in each physical DRAM Row. Each one-of-four bit pairs in this register corresponds to the DRAM row identified by the corresponding DRB register.</p> <table> <tr> <th>DRT Bits</th><th>DRAM Row</th></tr> <tr> <td>5,1</td><td>5</td></tr> <tr> <td>4,0</td><td>4</td></tr> </table> <table> <tr> <th>DRT</th><th>DRAM Type value definitions</th></tr> <tr> <td>0,0</td><td>SPM DRAM</td></tr> <tr> <td>0,1</td><td>EDO DRAM</td></tr> <tr> <td>1,0</td><td>SDRAM</td></tr> <tr> <td>1,1</td><td>Reserved</td></tr> </table>	DRT Bits	DRAM Row	5,1	5	4,0	4	DRT	DRAM Type value definitions	0,0	SPM DRAM	0,1	EDO DRAM	1,0	SDRAM	1,1	Reserved
DRT Bits	DRAM Row																
5,1	5																
4,0	4																
DRT	DRAM Type value definitions																
0,0	SPM DRAM																
0,1	EDO DRAM																
1,0	SDRAM																
1,1	Reserved																
6,3	<b>Reserved.</b>																
2	<b>Memory Address Select Enable (MASELEN).</b> When this bit is set to 1, CKE and CKEB are used to propagate the second copy of the MA0 and MA1 lines. CKE is muxed with MAA0 and CKEB is muxed with MAA1. When this bit is set to 0, the CKE and CKEB functionality is propagated across these lines. This bit defaults to 0 and BIOS must set it to 1 to take advantage of the second copy of the MA0 and MA1 lines.																

### 3.1.24. DRTL—DRAM ROW TYPE REGISTER LOW

Address Offset: 68h  
 Default Value: 00h  
 Access: Read/Write

This 8-bit register identifies the type of DRAM (EDO, SPM (standard page mode)), or SDRAM (synchronous DRAM) used in rows 0 to 3 and should be programmed by BIOS for optimum performance if EDO DRAM's or SDRAMs are used. The hardware uses these bits to determine the correct cycle timing to use before a DRAM cycle is run.

Bit	Description																				
7:0	<p><b>DRAM Row Type (DRT).</b> The DRT bits select the DRAM type installed in each physical DRAM Row. Each one-of-four bit pairs in this register corresponds to the DRAM row identified by the corresponding DRB register.</p> <table> <tr> <th>DRT Bits</th><th>DRAM Row</th></tr> <tr> <td>7,3</td><td>3</td></tr> <tr> <td>6,2</td><td>2</td></tr> <tr> <td>5,1</td><td>1</td></tr> <tr> <td>4,0</td><td>0</td></tr> </table> <table> <tr> <th>DRT</th><th>DRAM Type value definitions</th></tr> <tr> <td>0,0</td><td>SPM DRAM</td></tr> <tr> <td>0,1</td><td>EDO DRAM</td></tr> <tr> <td>1,0</td><td>SDRAM</td></tr> <tr> <td>1,1</td><td>reserved</td></tr> </table>	DRT Bits	DRAM Row	7,3	3	6,2	2	5,1	1	4,0	0	DRT	DRAM Type value definitions	0,0	SPM DRAM	0,1	EDO DRAM	1,0	SDRAM	1,1	reserved
DRT Bits	DRAM Row																				
7,3	3																				
6,2	2																				
5,1	1																				
4,0	0																				
DRT	DRAM Type value definitions																				
0,0	SPM DRAM																				
0,1	EDO DRAM																				
1,0	SDRAM																				
1,1	reserved																				

### 3.1.25. MTT—MULTI-TRANSACTION TIMER REGISTER (RESERVED TEST MODE REGISTER)

Address Offset: 70h  
 Default Value: 20h  
 Access: Read/Write

MTT is an 8-bit register that controls the amount of time that the MTXC's arbiter allows a PCI initiator to perform multiple transactions on the PCI bus. The MTT guarantees the minimum time, measured in PCLKs, that the PCI agent retains the ownership of the PCI bus from the initial assertion of grant.

Bit	Description
7:2	<p><b>MTT Count value.</b> The number of clocks programmed in the MTT represents the guaranteed time slice (in PCLKs) allotted to the current agent, after which the MTXC will grant the bus as soon as another PCI agent requests the bus. The value of 00h disables this function. The count value should be set to multiples of 4 (i.e., 2 lsbs are ignored).</p>
1:0	<p><b>Reserved.</b> Hardwired to 0. (i.e., counter has a resolution of 4 PCLKs)</p>



### 3.1.26. ESMRAM—EXTENDED SYSTEM MANAGEMENT RAM CONTROL REGISTER

Address Offset: 71h  
 Default Value: 00h  
 Access: Read/Write

The Extended SMRAM register controls the configuration of Extended SMRAM space. MTXC supports two types of SMRAM memory: Compatible and Extended. The Compatible SMRAM (C\_SMRAM) memory provides an uncacheable SMRAM memory space below 1 Mbytes in the A and B segments. The Extended SMRAM (E\_SMRAM) memory provides a writeback cacheable SMRAM memory space that is above 1 Mbytes. This register provides the following types of control over SMRAM space:

- Where the memory space is located (above 1 Mbytes, below 1 Mbytes)
- Enabling of SMRAM memory (TSEG, 128 Kbytes, 256 Kbytes, 512 Kbytes or 1 Mbytes of additional SMRAM memory) for Extended SMRAM space only.
- Cacheability control (for the Extended SMRAM space only)
- Protection of SMRAM space for non-SMM accesses

Bit	Description										
7	<b>High SMRAM Enable (H_SMRAME).</b> 1=Enable. 0=Disable. This bit enables the high SMRAM memory space to appear in the appropriate physical address locations between 100A0000h and 100F0000h.										
6	<b>Extended SMRAM Error (E_SMERR).</b> This bit is set when CPU accesses the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit=0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.										
5	<b>SMRAM Cache Strategy (SM_CACHE).</b> Hardwired to 0. This bit determines how Extended SMRAM space is cached (writethru or writeback). Since the MTXC supports only writeback for extended SMRAM space, this bit is hardwired to 0.										
4	<b>SMRAM_L1_EN (SM_L1).</b> This bit should be set to 1 if Extended SMRAM is being used and the system wishes to L1 writeback cache this memory space. Default value for this bit is 0.										
3	<b>SMRAM_L2_EN (SM_L2).</b> This bit should be set to 1 if Extended SMRAM is being used, and there is less than 32 Mbytes of DRAM in the system. Setting of this bit when SM_L1 bit=1 allows the Extended SMRAM to be writeback cached in the L2. Default value for this bit is 0.										
2:1	<p><b>TSEG_SZ[1:0] (T_SZ).</b> Selects the size of the TSEG memory block, if enabled. This memory is taken from the top of DRAM space, which is no longer claimed by the memory controller (all accesses to this space are sent to the PCI bus if TSEG_EN is set). This memory appears at the physical memory space of 256 Mbytes plus the top of memory (TOM) minus the size of TSEG. This field decodes as follows:</p> <table> <tr> <th>Bits[1,0]</th><th>Description</th></tr> <tr> <td>00</td><td>(TOM-128 KB) to TOM</td></tr> <tr> <td>01</td><td>(TOM-256 KB) to TOM</td></tr> <tr> <td>10</td><td>(TOM-512 KB) to TOM</td></tr> <tr> <td>11</td><td>(TOM-1 MB) to TOM</td></tr> </table>	Bits[1,0]	Description	00	(TOM-128 KB) to TOM	01	(TOM-256 KB) to TOM	10	(TOM-512 KB) to TOM	11	(TOM-1 MB) to TOM
Bits[1,0]	Description										
00	(TOM-128 KB) to TOM										
01	(TOM-256 KB) to TOM										
10	(TOM-512 KB) to TOM										
11	(TOM-1 MB) to TOM										
0	<b>TSEG_EN (T_EN).</b> When G_SMRAME=1 and T_EN=1, the TSEG is enabled to appear in the appropriate physical address space.										

### 3.1.27. SMRAMC—SYSTEM MANAGEMENT RAM CONTROL REGISTER

Address Offset: 72h  
Default Value: 02h  
Access: Read/Write

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. MTXC supports two types of SMRAM memory: Compatible and Extended. The Open, Close, and Lock bits function only when G\_SMFRAME bit is set to a 1. Also, the OPEN bit be reset before the LOCK bit is set.

Bit	Description
7	<b>Reserved.</b>
6	<b>SMM Space Open (D_OPEN).</b> When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMIACK# is negated. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 is mutually exclusive with D_CLS=1. When D_LCK is set to a 1, D_OPEN is reset to 0 and becomes read only.
5	<b>SMM Space Closed (D_CLS).</b> When D_CLS=1, SMM space DRAM is not accessible to data references, even if SMIACK# is asserted. Code references may still access SMM space DRAM. This will allow SMM software to reference “through” SMM space to update the display, even when SMM space is mapped over the VGA range. Software should ensure that D_OPEN=1 is mutually exclusive with D_CLS=1.
4	<b>SMM Space Locked (D_LCK).</b> When D_LCK is set to 1, D_OPEN is reset to 0 and both D_LCK and D_OPEN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a power-on reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to “lock down” SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	<b>Global SMRAM Enable (G_SMFRAME).</b> If set to a 1, then Compatible SMRAM functions is enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADS# with SMIACK#). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details.
2:0	<b>Compatible SMM Space Base Segment (C_BASE_SEG).</b> This field programs the location of SMM space. SMM DRAM is not remapped. It is simply “made visible” if the conditions are right to access SMM space; otherwise, the access is forwarded to PCI. C_BASE_SEG=010 selects the SMM space as A0000–BFFFFh. All other values are reserved. PCI initiators are not allowed to access to SMM space. These bits are hardwired to 010.

Table 8 summarizes the operation of SMRAM space cycles targeting the SMI space addresses.

Table 8. SMRAM Space Cycles

G_S M_R A_M E	D_L C_K	D_C L_S	D_O P_E_N	S_M I_A C_T#	H_S M_R A_M E	T_S E_G E_N	Code Fetch			Data Access		
							A→PCI	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
0	x	x	x	x	x	x	A→PCI	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	0	0	0	0	0	0	A→DRAM	S→PCI	T→PCI	A→DRAM	S→PCI	T→PCI
1	0	0	0	0	0	1	A→DRAM	S→PCI	T→DRAM	A→DRAM	S→PCI	T→DRAM
1	0	0	0	0	1	0	A→PCI	S→DRAM	T→PCI	A→PCI	S→DRAM	T→PCI
1	0	0	0	0	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→DRAM	T→DRAM
1	0	x	0	1	x	x	A→PCI	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	0	0	1	x	0	0	A→DRAM	S→PCI	T→PCI	A→DRAM	S→PCI	T→PCI
1	0	0	1	x	0	1	A→DRAM	S→PCI	T→DRAM	A→DRAM	S→PCI	T→DRAM
1	0	0	1	x	1	0	A→PCI	S→DRAM	T→PCI	A→PCI	S→DRAM	T→PCI
1	0	0	1	x	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→DRAM	T→DRAM
1	0	1	0	0	0	0	A→DRAM	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	0	1	0	0	0	1	A→DRAM	S→PCI	T→DRAM	A→PCI	S→PCI	T→PCI
1	0	1	0	0	1	0	A→DRAM	S→DRAM	T→PCI	A→PCI	S→PCI	T→PCI
1	0	1	0	0	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→PCI	T→PCI
1	0	1	1	x	x	x	Invalid			Invalid		
1	1	0	0	0	0	0	A→DRAM	S→PCI	T→PCI	A→DRAM	S→PCI	T→PCI
1	1	0	0	0	0	1	A→DRAM	S→PCI	T→DRAM	A→DRAM	S→PCI	T→DRAM
1	1	0	0	0	1	0	A→PCI	S→DRAM	T→PCI	A→PCI	S→DRAM	T→PCI
1	1	0	0	0	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→DRAM	T→DRAM
1	1	x	0	1	x	x	A→PCI	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	1	1	0	0	0	0	A→DRAM	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	1	1	0	0	0	1	A→DRAM	S→PCI	T→DRAM	A→PCI	S→PCI	T→PCI
1	1	1	0	0	1	0	A→PCI	S→DRAM	T→PCI	A→PCI	S→PCI	T→PCI
1	1	1	0	0	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→PCI	T→PCI

**NOTES:**

1. A=A Segment, S=100A0000h to 100FFFFFFh, and T=T Segment. The Code Fetch and Data Access columns indicate whether the access is to the PCI bus or to main memory DRAM.



### 3.1.28. MCTL—MISCELLANEOUS CONTROL REGISTER

Address Offset: 79h  
Default Value: 00h  
Access: Read/Write

Bit	Description
7	Reserved.
6	<b>ACPI Control Register Enable (ACRE).</b> 0=Any CPU access to I/O address 0022h is passed on to the PCI bus. 1=Any CPU access to I/O address 0022h is processed internally in the MTXC. This bit must be set to 1 before accessing the "Arbiter Disable" bit in the PM2_CNTRL Register (0022h).
5	<b>Suspend Refresh Type (SRT).</b> 0=CBR refresh. 1=Self refresh. This bit determines what type of DRAM refresh is used during Power On Suspend (POS) or Suspend to DRAM modes. This bit applies to EDO/FPM DRAM only. SDRAM always uses self refresh, regardless of the state of this bit.
4	<b>Normal Refresh Enable (NREF_EN).</b> Setting this bit to 1 switches MTXC from suspend refresh to normal refresh. After the reset, this bit must be set by software executing out of EPROM. MTXC waits for this bit to be set before exiting out of suspend refresh mode.
3	Reserved.
2	<b>Internal Clock Control (Gated Clock) Disable (lcc).</b> 1=Disable. 0=Enable. This bit, when set to 0, allows the MTXC to reduce its power consumption (via turning off its internal clocks, to specific interfaces) when in chip standby mode. This bit defaults to 0.
1:0	Reserved.

## 4.0. FUNCTIONAL DESCRIPTION

### 4.1. Host Interface

The Host Interface of the MTCX is designed to support the Pentium microprocessor. The host interface of the MTCX supports 60-, and 66-MHz bus speeds. The Intel 430TX PCIs set supports the Pentium microprocessor with a full 64-bit data bus, 32-bit address bus, and associated internal writeback cache logic. Host bus addresses are decoded by the MTCX for accesses to main memory, PCI memory, and PCI I/O. The MTCX also supports the pipelined addressing capability of the Pentium microprocessor.

### 4.2. Secondary Cache Interface

The MTCX integrates a high performance writeback second level cache controller using internal/external tags and provides a full first level and second level cache coherency mechanism. The second level cache is direct mapped, nonsectored, and supports a writeback, no write allocate (lines are not allocated on write misses) write policy.

The second level cache can be configured to support either a 256-KB or 512-KB cache using synchronous pipelined burst SRAM or DRAM Cache. One additional PCIs set signal (KRQAK) is required to support DRAM Cache. 64-Mbytes cacheability coverage is obtained with 8Kx8 standard SRAM to store the tags for 256-KB configuration. For the 512-KB configurations, a 16Kx8 standard SRAM is used to store the tags and the valid bits for 64-MB cacheability.

A second level cache line is 32-bytes wide. In the 256-KB configurations, the second level cache contains 8K lines, while the 512-KB configurations contain 16K lines. Valid and modified status bits are kept on a per line basis. Cacheability of the entire memory space in first level cache is supported, while only the lower 64 MB of main memory is cacheable in the second level cache. Table 9 shows the tag sizes needed to support different sizes of cacheability. Only main memory controlled by the MTCX DRAM interface is cached. PCI memory is not cached.

**Table 9. Cacheability**

Cache Size	Tag Size	Cacheability
256 Kbytes	8K by 8 bits	64 Mbytes
512 Kbytes	16K by 8 bits (including valid bit)	64 Mbytes

The following table shows the different standard SRAM access time requirements for different host clock frequencies.

**Table 10. SRAM Access Time Requirements**

Host Clock Frequency (MHz)	Pipelined Burst Clock-to-Output Access Time (ns)	Tag RAM Cycle Time (ns)
60	10	15
66	8.5	15

Figure 4 and Figure 5 show the connections between the MTXC and the external tag RAM and data SRAM.

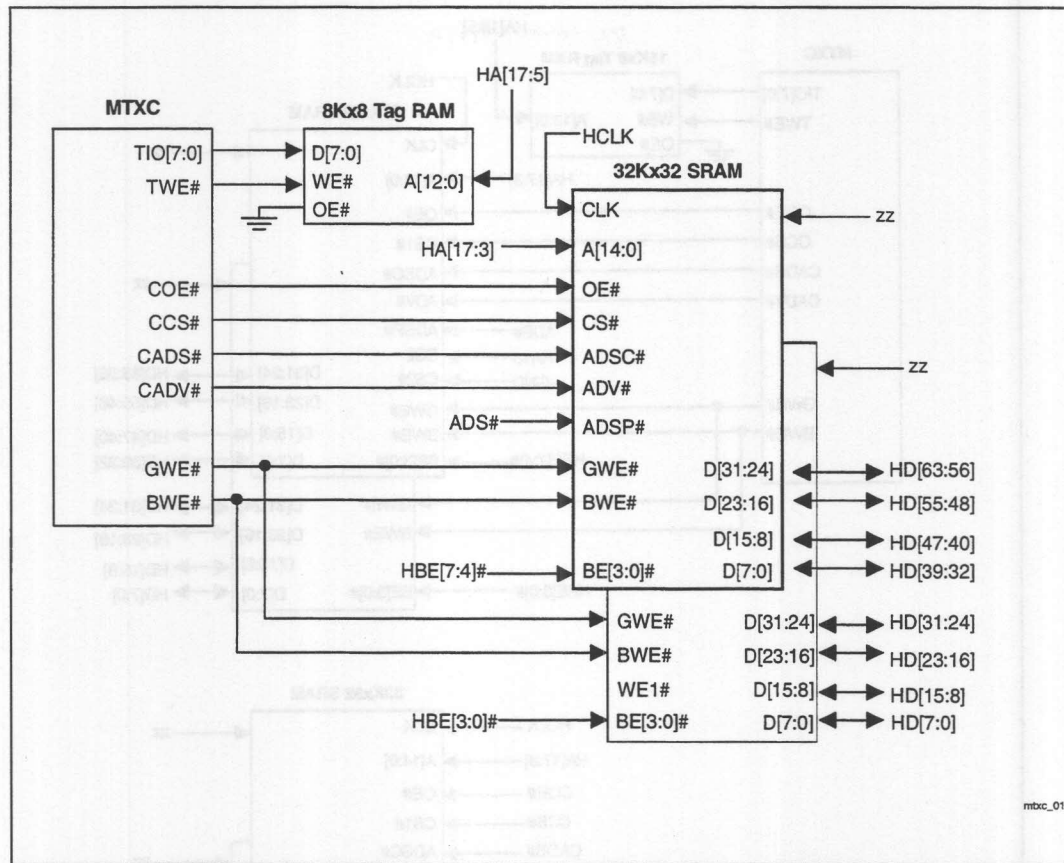


Figure 4. MTXC Connections for 256K Second Level Cache with PBSRAM

Figure 5 shows a 512-KB implementation using four 32Kx32 SRAM. Two 64Kx32 devices could also be used. In this case, HA18 would not be connected to CS2# (i.e., CS2 and CS2# should be connected to an active state). HA18 should be connected to one of the address lines on the 64Kx32 SRAM and is still required for the TAG RAM.



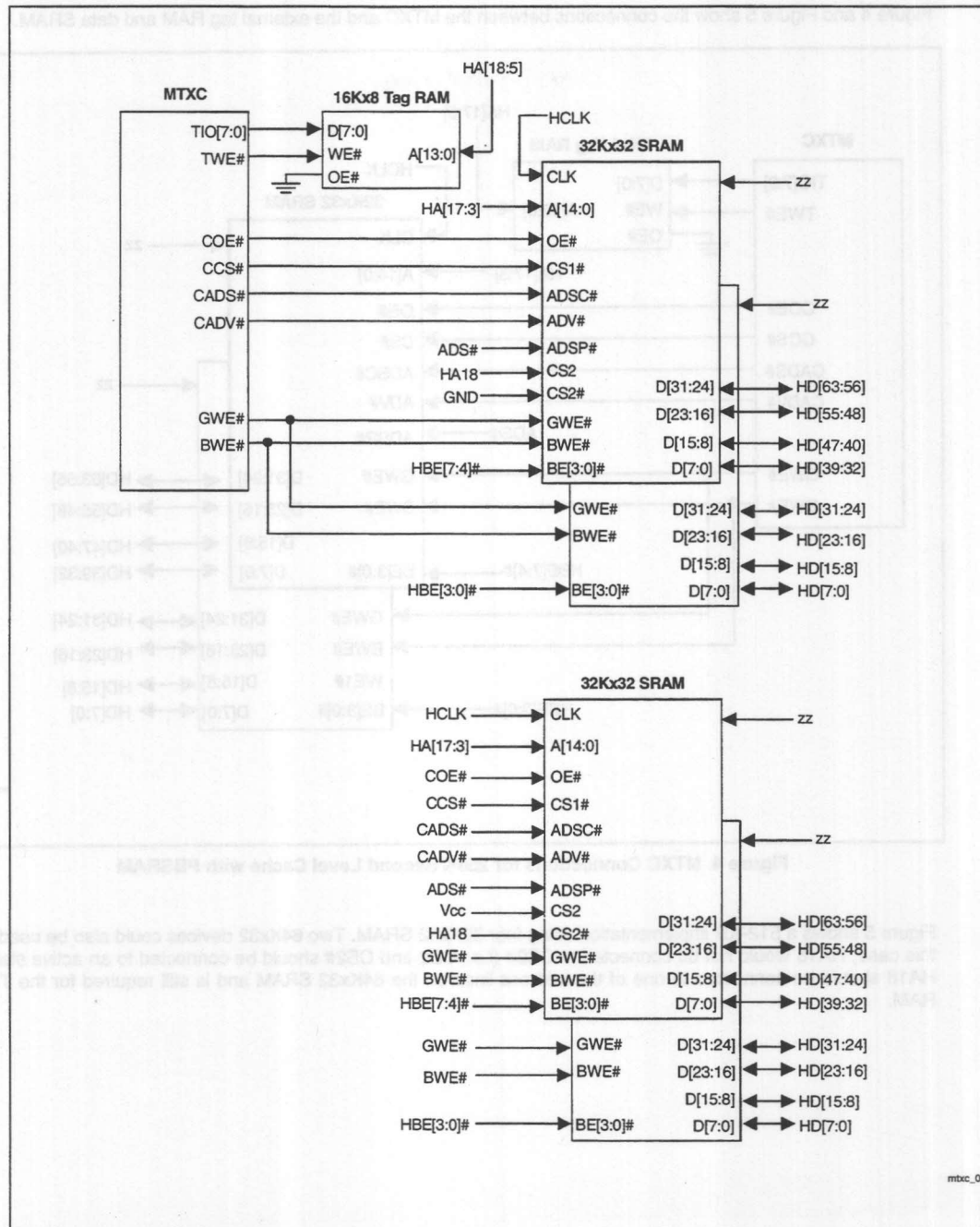


Figure 5. MTXC Connections for 512K Second Level Cache with PBSRAM

#### 4.2.1. CLOCK LATENCIES

Table 11 lists the latencies for various processor transfers to and from the second level cache.

**Table 11. Second Level Cache Latencies with Pipelined Burst SRAM**

Cycle Type	HCLK Count
Burst Read	3-1-1-1
Burst Write (write back)	3-1-1-1
Single Read	3
Single Write	3
Pipelined Back-to-Back Burst Reads	3-1-1-1,1-1-1-1 (note 1)

#### NOTES:

1. The back to back cycles do not account for CPU idle clocks between cycles.

#### 4.2.2. SNOOP CYCLES

The snoop (or inquire) cycle is used to probe the first level and second level caches when a PCI master attempts to access main memory. This is done in order to maintain coherency between the first and second level caches and main memory.

To maintain optimum PCI bandwidth to DRAM, the MTXC utilizes a snoop ahead algorithm. Once the snoop for the first cache line of a transfer has completed, the MTXC automatically snoops the next sequential cache line. This algorithm enables the MTXC to continue burst transfers across cache line boundaries.

#### Reads

Snoop cycles are performed by driving the PCI master address onto the host address bus and asserting EADS#. The processor then performs a tag lookup to determine whether the addressed memory is in the first level cache. If the snoop hit is to a Modified Line in the first level cache (HITM# asserted), then the line in the first level cache is posted to the DRAM Posted Write buffers. The line in the second level cache (if it exists) is invalidated. The line in the first level cache is not invalidated if the INV pin on the CPU is tied to the KEN# signal from the MTXC. KEN#/INV will be driven low by the MTXC with EADS# assertion during PCI master read cycles.

At the same time as the first level snoop cycle, the MTXC performs a tag lookup to determine whether the addressed memory is in the second level cache. A hit to a modified line in the second level cache also results in a writeback to DRAM posted write buffers if HITM# is not asserted. The PCI data is serviced from the DRAM after the line has been retired to DRAM.

#### Writes

PCI Master write cycles never result in a write directly into the second level cache. A snoop hit to a modified line in either the first or second caches results in a writeback of that line to main memory. If both the first and second level caches have modified lines, then the line is written back from the first level cache. In all cases lines in the first and second level caches are invalidated and the PCI write to main memory occurs after the writeback completes. A PCI master write snoop hit to an unmodified line in either the first or second level caches results in the line being invalidated. KEN#/INV will be driven high by the MTXC with EADS# assertion during PCI master write cycles.

#### 4.2.3. DRAM CACHE SECOND LEVEL CACHE MODE

DRAM Cache L2 cache implementation is similar to Pipelined Burst SRAM, except for the addition of the KRQAK bi-direct refresh handshake signal between the MTXC and L2 SRAM. A DRAM Cache type L2 is assumed present when the KRQAK pin is sampled high during the negation of the reset signal. An internal weak pull-down is used on the MTXC KRQAK pin to default to a non DRAM Cache L2 mode, if this pin is left unconnected. An external pull-up (10 k $\Omega$ ) must be used on KRQAK when DRAM Cache SRAM is used. Note that there is no configuration bit associated with the L2 Pseudo SRAM mode.

The SRAM can operate in either master or slave mode via the M/S# strapping bit. In master mode, the SRAM drives the KRQAK pin to request a refresh. A slave device never drives KRQAK, but only monitors it to determine when a refresh period begins. Only one SRAM device within the L2 cache is master enabled. The other SRAM devices must be slaves.

During reset, the master SRAM and MTXC tri-state their KRQAK outputs. After the SRAM RESET pin is negated, KRQAK remains tri-stated for one whole refresh interval and is then driven high by the master SRAM. The SRAM signals a refresh request by driving KRQAK low for 1 clock, high the next clock, and then tri-states on the following clock and waits, sampling the KRQAK pin. The MTXC after sampling the SRAM's request on KRQAK and after the SRAM has tri-stated its KRQAK output, waits for a host bus dead clock and grants an L2 refresh by driving its KRQAK pin in an identical fashion to the SRAM's request signaling. When all SRAM's see the refresh grant from the MTXC, they begin their internal refresh cycle for a period of 20 clocks.

#### 4.3. DRAM Interface

The MTXC integrates a DRAM controller that supports a 64-bit memory array from 4 Mbytes to 256 Mbytes of main memory. The MTXC supports Standard Page Mode (FPM), Extended Data Out (EDO) and Synchronous DRAM (SDRAM) memories using 32-bit wide SIMM modules, 64-bit wide unbuffered DIMM modules and 64-bit wide unbuffered SO-DIMM modules. DRAM parity is not supported, and for loading reasons, parity modules should not be used. All three memory types can be mixed and matched. The MTXC generates all DRAM control signals and multiplexed addresses for the DRAM array. The address and data flows through the MTXC for all DRAM accesses. The DRAM controller interface is fully configurable through a set of control registers. Complete descriptions of these registers are given in the MTXC configuration register description. A brief overview of these registers is provided in this section.

The MTXC supports page mode DRAMs and EDO (Extended Data Out) DRAMs; otherwise known as Hyper Page mode. The twelve multiplexed address lines, MA[11:0], allow the MTXC to support 4-Mbit, 16-Mbit, and 64-Mbit memory, both symmetrical and asymmetrical addressing. The MTXC has six RAS# lines enabling the support of up to six rows of DRAM. Eight CAS# lines allow byte control over the array during write operations. The MTXC targets 60 ns (also supports 50 ns and 70 ns) DRAMs, and supports both single- and double-sided DRAM modules. The MTXC provides CBR refresh and extended CBR refresh in the normal mode and self refresh or CBR (for EDOs only) during suspend mode.

The MTXC also supports SDRAMs. The fourteen multiplexed address lines, MA[13:0], allow the MTXC to support 16-Mbit and 64-Mbit SDRAM devices. The MTXC has six CS# lines (i.e. muxed onto RAS#[5:0]). Although six CS# signals are provided, due to loading concerns, 5 rows of SDRAM maximum is recommended. Eight DQM lines (i.e., muxed with CAS#[7:0]) allow byte control over the array during the write operation. Two copies of SRAS# and SCAS# signals are provided for encoded SDRAM commands. The MTXC targets 60- and 66-MHz SDRAMs and supports both single- and double-sided SDRAM modules.

The DRAM interface of the MTXC is configured by the DRAM Control Mode Register (DRAMC), DRAM Extended Control Register (Dramec), DRAM Timing Register (DRAMT), SDRAM Control Register (SDRAMC), six DRAM Row Boundary (DRB) Registers, and the DRAM Row Type (DRT) Registers. The DRB registers define the size of each row in the memory array.



Seven Programmable Attribute Map (PAM) Registers are used to specify the cacheability, PCI enable, and read/write status of the memory space between 640 Kbytes and 1 Mbytes. Each PAM Register defines a specific address area enabling the system to selectively mark specific memory ranges as cacheable, read only, write only, read/write, or disabled. When a memory range is disabled, all CPU accesses to that range are forwarded to PCI.

The MTXC also supports one of two memory holes, either from 512 KB–640 KB or from 14/15 MB–16 MB in main memory. Accesses to the memory holes are forwarded to PCI. The memory hole can be enabled/disabled through the DRAM Control register. All other memory from 1M to 256 MB is read/write L1 cacheable, and is L2 cacheable up to 64 MB.

An optional Extended SMRAM DRAM memory space is also supported in the 256-MB to 512-MB address range. It consists of the 640-KB–1-MB DRAM area aliased at the 256-MB memory segment, and also an optional 128K/256K/512K/1M DRAM area chopped from the Top-of-DRAM memory and aliased above 256 MB in a similar manner.

#### 4.3.1. DRAM ORGANIZATION

The MTXC integrates a DRAM controller that supports EDO, FPM, and SDRAM. SDRAM, EDO and FPM DRAM's can be mixed between rows, however, a given row must contain only one type of DRAM. When DRAM types are mixed (EDO, FPM and SDRAM) each row will run optimized for that particular type of DRAM.

The MTXC supports six rows of memory (six RAS#/CS# lines). For maximum memory flexibility and performance, it is recommended that a DRAM configuration of four rows be used. This allows 64-Mbit DRAM devices to be used as well as the mixing of SDRAM and EDO/FPM. Figure 6 shows an EDO/FPM configuration using x32 SIMM modules and Figure 7 shows a four row EDO/FPM/SDRAM configuration using x64 DIMM modules (or x64 SO-DIMM).

#### NOTE

It is not recommended to mix SDRAM (which are 3V devices) with 5V EDO/FPM SIMMs, unless the SDRAM and EDO/FPM are properly isolated (e.g., isolate the memory data lines with Qswitches). Mixing 5V and 3V memory is not recommended for reliability reasons. Not all SDRAMs are 5V tolerant.

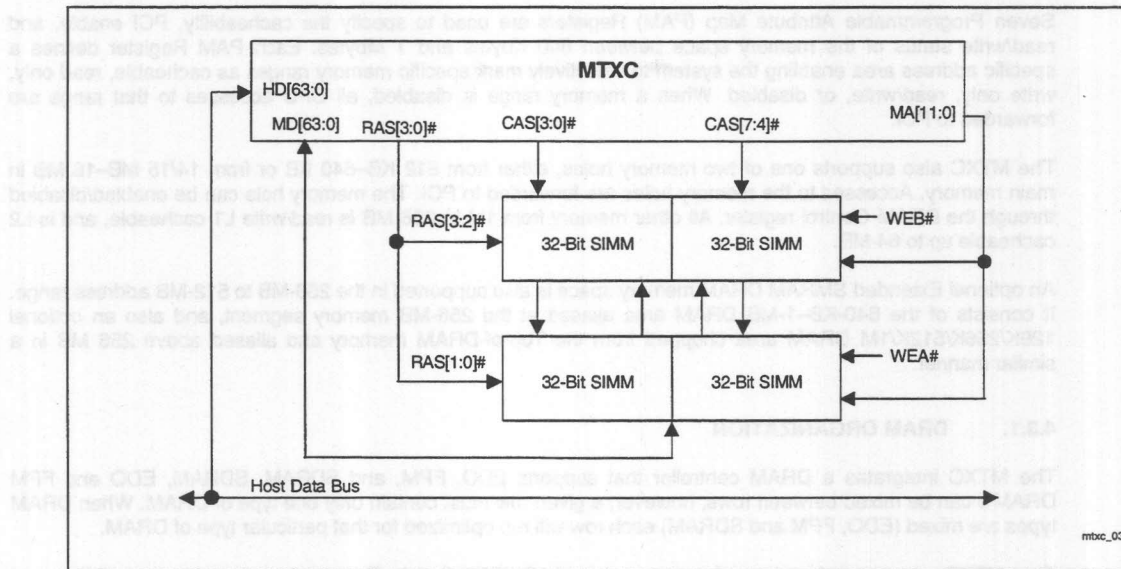


Figure 6. FPM/EDO Four Row SIMM Configuration

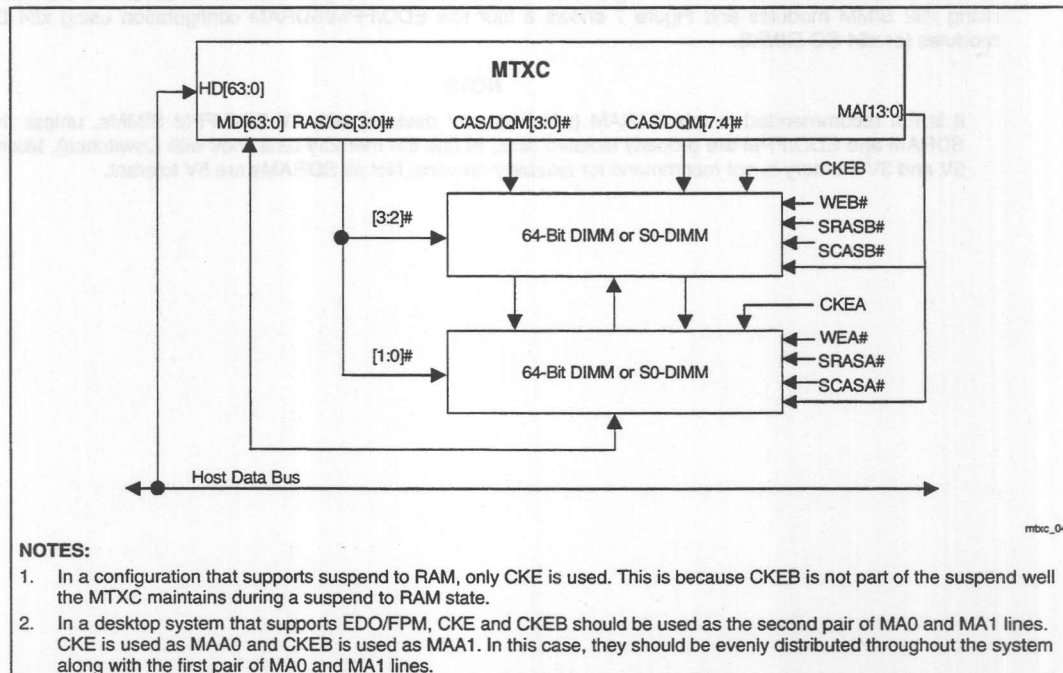


Figure 7. FPM/EDO/SDRAM Four Row DIMM or SO-DIMM Configuration

#### Rules for Populating SIMM Modules (or x32 SO-DIMM modules)

- SIMM sockets can be populated in any order (i.e., memory for RAS0# does not have to be populated before memory for RAS[2:1]# or RAS[4:3]# are used).
- SIMM socket pairs (i.e., two, 32-bit wide SIMMs) need to be populated with the same densities. For example, SIMM sockets for RAS0# should be populated with identical densities. However, SIMM sockets for RAS[2:1]# can be populated with different densities than the SIMM socket pair for RAS0#.
- EDOs and standard page mode can both be used; however, only one type should be used per SIMM socket pair. For example, in the table shown below SIMM sockets for RAS[2:1]# can be populated with EDOs while SIMM sockets for RAS[4:3]# can be populated with standard page mode. If different memory is used for different rows, each row will be optimized for that type of memory.
- The DRAM Timing Register which provides the DRAM speed grade control for the entire memory array must be programmed to use the timings of the slowest DRAMs installed.

#### Rules for Populating DIMM or SO-DIMM modules

- DIMM or SO-DIMM sockets can be populated in any order (i.e., memory for RAS0# does not have to be populated before memory for RAS[2:1]# or RAS[4:3]# are used).

### 4.3.2. CONFIGURATION REQUIREMENTS

#### General Configuration Requirements

- In a system that uses 64-Mbit SDRAM, the RAS4#/CS4#/BA1 and RAS5#/CS5#/MA13 signals are used to provide two additional address lines (BA1 and MA13), and KRQAK/CS4\_64# is used to provide the 5th CS# line, if required. To enable 64-Mbit support for four rows of SDRAM, set SDRAMC[bit 1] to 1 (offset 54h). To enable 64-Mbit support for five rows of SDRAM, SDRAMC[bit 1] must be set to 1, and DRAM cache must **not** be present in the system (indicated by CEC[bit 5]=0, offset 53h). In a five row SDRAM system that supports 64-Mbit SDRAM devices, the KRQAK/CS4\_64# signal provides the fifth CS# (or CS4\_64#) function. This means that a system that supports DRAM Cache, can not support five rows of 64-Mbit SDRAM. However, four rows of 64-Mbit SDRAM with DRAM Cache is supported. In a FPM/EDO only configuration, there are no restrictions on using 64-Mbit devices (i.e., all six rows can support 64-Mbit DRAM devices. However, SDRAMC[bit 1] must be set to 1 if more than four rows of EDO/FPM are used. This allows the RAS4# and RAS5# functions to be used.

	Driven on RAS5#/CS5#/ MA13	Driven on RAS4#/CS4#/ MA13	Driven on KRQAK/ CS4_64#	64-Mbit (SDRAM)	64-Mbit (EDO/FPM)
Bit 1, reg 54h=0	RAS5#/CS5#	RAS4#/CS4#	KRQAK	no	yes (6 rows)
Bit 1, reg 54h=1 and DRAM Cache is present*	MA13	BA1 (Bank Select)	KRQAK	Yes (4 rows)	Yes (4 rows)
Bit 1, reg 54h=1 and DRAM Cache is not present <sup>1</sup>	MA13	BA1 (Bank Select)	RAS4#/ CS4_64#	Yes (5 rows)	Yes (5 rows)

#### NOTES:

1. The presence of DRAM cache is indicated by the value in bit 5, register 53h.
- Due to loading, using SDRAM x4 devices is not recommended.
  - Buffering of SDRAM Rows is not supported
  - In a five row system, the 5th row is intended to be implemented with DRAM devices that are soldered down on the motherboard. If a DIMM or a SIMM is used in the 5th row, it should **not** be used as an upgrade path



by the end user; the size and type of DRAM that can be implemented in the 5th row is limited (see the bullets below).

- The total memory supported is 256 MB, even though it is possible to populate the six rows with more than 256 MB. This limit must be ensured by the system BIOS.

#### EDO/FPM only configuration Requirements

- If more than four rows of x4 DRAM devices + one row of x8 DRAM devices of memory is supported, it is recommended that all six rows be buffered. MA and MWE# enable signals should be buffered. In a system that only supports x8 or x16 devices (i.e., x4 devices not supported), six rows of memory can be supported without buffering.
- Maximum load supported without buffers: Four rows of x4 DRAM devices + one row of x8 DRAM devices.
- A second pair of MA0 and MA1 signals are provided by muxing CKE with MAA0 and CKEB with MAA1. In a desktop system, it is required that the second pair of MA lines be used to support 5-2-2-2 EDO performance in more than two rows of memory. The second pair of MA lines are not required in a mobile system, assuming x4 devices are not used. The MA functionality is selected via DRAMC[bit 2] (67h).

#### SDRAM only configuration Requirements

- Maximum rows supported; Five rows of x8 devices.

#### SDRAM/EDO/FPM mixing configuration Requirements

- If SDRAM and EDO/FPM are mixed in a system, the configuration is limited to a maximum of four rows (two rows of x4 EDO/FPM and two rows of x8 or x16 SDRAM). If only x8 or x16 EDO/FPM and SDRAM devices are used (i.e., not x4's), five rows can be supported.
- SDRAMs can be mixed with EDO/FPM on a row by row basis (e.g., row 0 can be populated with SDRAMs while row 3 is populated with EDO/FPM).
- A second pair of MA0 and MA1 signals are provided by muxing CKE with MAA0 and CKEB with MAA1. In a desktop system, it is required that the second pair of MA lines be used to support 5-2-2-2 EDO performance in more than two rows of memory. The second pair of MA lines are not required in a mobile system, assuming x4 devices are not used. The MA functionality is selected via DRAMC[bit 2] (67h).

Table 12 provides a summary of the characteristics of memory configurations supported by the MTXC. Minimum values listed are obtained with single-sided SIMMs or DIMMs. Maximum values are obtained with double-sided SIMMs or DIMMs. Note that, for a 64-bit wide memory array, a minimum of two 32-bit wide DRAM SIMMs are required in any specific row. The minimum values used are also the smallest upgradeable memory size. Please note that EDO/FPM can also come on x64 DIMM modules.

Row	Max. # of DRAMs	Max. # of Banks	Max. # of Banks per Row	Max. # of Banks per Row (if 64-bit)	Max. # of Banks per Row (if 32-bit)
0	16	4	4	4	4
1	16	4	4	4	4
2	16	4	4	4	4
3	16	4	4	4	4
4	16	4	4	4	4
5	16	4	4	4	4

Table 12. Minimum (Upgradeable) and Maximum Memory Size for each configuration (DRAM)

DRAM Tech.	DRAM Density	DRAM Width	DRAM SIMM		DRAM Addressing	Address Size		DRAM Size	
			SS x32	DS x32		Row	Col	Min. (UP) (1 row)	Max. (6 rows)
4M	512K	8	512K	1M	Asymmetric	10	9	4 MB	24 MB
	1M	4	1M	2M	Symmetric	10	10	8 MB	48 MB
16M	1M	16	1M	2M	Symmetric	10	10	8 MB	48 MB
	1M	16	1M	2M	Asymmetric	12	8	8 MB	48 MB
	2M	8	2M	4M	Asymmetric	11	10	16 MB	96 MB
	4M	4	4M	8M	Symmetric	11	11	32 MB	192 MB
	4M	4	4M	8M	Asymmetric	12	10	32 MB	192 MB
64M	2M	32	2M	4M	Asymmetric	12	9	16 MB	96 MB
	4M	16	4M	8M	Symmetric	11	11	32 MB	192 MB
	4M	16	4M	8M	Asymmetric	12	10	32 MB	192 MB
	8M	8	8M	16M	Asymmetric	12	11	64 MB	256 MB
	16M	4	16M	32M	Symmetric	12	12	128 MB	256 MB

Table 13. Minimum (Upgradeable) and Maximum Memory Size for each configuration (SDRAM)

SDRAM Tech.	SDRAM Density	SDRAM Width	SDRAM DIMM		SDRAM Addressing	Address Size		SDRAM Size	
			SS x64	DS x64		Row	Column	Min. (UP) (1 row)	Max. (6 rows)
16M	1M	16	1M	2M	Asymmetric	12	8	8 MB	48 MB
	2M	8	2M	4M	Asymmetric	12	9	16 MB	96 MB
	4M	4 <sup>1</sup>	4M	8M	Asymmetric	12	10	32 MB	192 MB
64M	2M	32	2M	4M	Asymmetric	12	9	16 MB	96 MB
	2M	32	2M	4M	Asymmetric	13	8	16 MB	96 MB
	4M	16	4M	8M	Asymmetric	14	8	32 MB	192 MB
	8M	8	8M	16M	Asymmetric	14	9	64 MB	256 MB
	16M	4 <sup>1</sup>	16M	32M	Asymmetric	14	10	128 MB	256 MB

**NOTES:**

- Functionally the 430TX supports x4 SDRAM devices. However, due to loading reasons, it is not recommended that x4 devices be used in 60-MHz and 66-MHz designs.

The memory organization shown below represents the maximum 256 MB of address space. Accesses to memory space above Top-of-DRAM (< 256 MB), video buffer, or the memory gaps (if enabled) are forwarded to PCI, and these regions are not cacheable. Below 1 MB, there are several memory segments which have selectable cacheability. None of the DRAM space occupied by the video buffer (except for SMM usage) or the memory space gaps is remapped (and is therefore "lost").

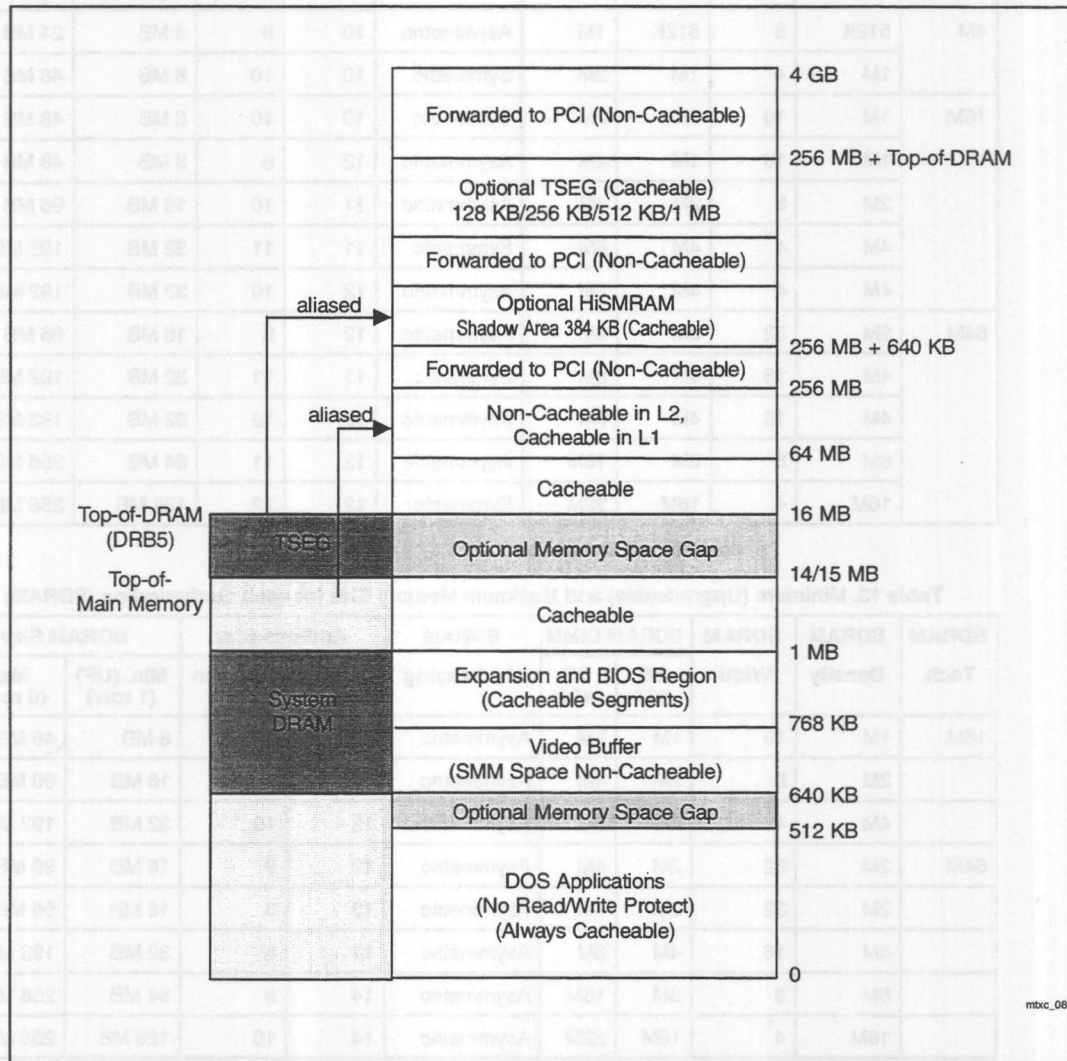


Figure 8. Memory Space Organization



### 4.3.3. DRAM ADDRESS TRANSLATION

The multiplexed row/column address to the DRAM memory array is provided by the MA[11:0] signals (MA[13:0] for SDRAM 64-Mbit support). The MA bits are derived from the host or PCI address bus as defined by the Table 14. The MTXC supports a 2K byte page size only. The MA lines are translated from the address lines A[26:3] for all memory accesses.

Table 14. MTXC DRAM Address Map Summary

ADDR	MA13	MA12/ BA1	MA11/ BA0	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row	A24	A23	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col		A23	A26/ A11	A11/ A25 "V"	A11/ A24/ A26	A11/ A22/ A23/ A25	A10	A9	A8	A7	A6	A5	A4	A3

#### NOTES:

1. V=Valid level (either 0 or 1) used for SDRAMs. It is 1 during the initialization sequence. It is 0 during normal mode of operation.
2. BA0 and BA1 are the muxed bank selects for SDRAM. Bank select BA1 is required for 64-Mbit SDRAM support.

### 4.3.4. DRAM PAGING

If DRAMC[bit 4]=1, the MTXC keeps the page open until a page or row miss occurs. If DRAMC[bit 4]=0 (default), the DRAM page is kept open when:

- CPU host bus is non-idle, or
- PCI interface owns the bus.

### 4.3.5. DRAM TYPES

#### 4.3.5.1. FPM Mode

The MTXC, as a default, supports the standard fast page mode (FPM) DRAM.

#### 4.3.5.2. EDO Mode

Extended Data Out (or Hyper Page Mode) DRAM is designed to improve the DRAM read performance. EDO DRAM holds the memory data valid until the next CAS# falling edge. Compared to standard page mode DRAM which tri-states the memory data when CAS# negates to precharge. With EDO, the CAS# precharge overlaps the memory data valid time. This allows CAS# to negate earlier while still satisfying the memory data valid window time.

#### 4.3.5.3. SDRAM Mode

Synchronous DRAM (SDRAM) implements a fully synchronous interface as compared to a conventional DRAM whose timing delays are related to the rising and falling edges of the RAS#, CAS#, and WE# input signals. The 430TX supports all of the features and timings as shown in the "SDRAM PC" specification. The objective of the SDRAM PC Specification is to enable low cost and easily manufactureable SDRAMs for the main stream volume

desktop and Mobile PC's. There are three grade parts defined for the 430TX. All of the speed grade conform to the *SDRAM PC Specification*. For information on the performance of each of the Speed grade parts, refer to the DRAM performance section. The Three speed grade parts are shown in Table 15.

Table 15. SDRAM Speed Grade Parts

Speed Grade	CAS latency (CL)	RAS to CAS (Trcd)	System Frequency
66.67 MHz	3	3	60/66 MHz
66.67 MHz	3	2	60/66 MHz
66.67 MHz	2	2	60/66 MHz

#### SDRAM Command Reference

The 430TX supports the following commands:

Command	Command
Mode Register Set (MRS)	No Operation (NOP)
Activate Bank (ACT)	Auto Refresh CBR (REFR)
Read Bank (RD)	Data Write/Output Enable
Write Bank (WR)	Data Mask/Output Disable
Precharge All Banks (PALL)	Self Refresh Entry
Deselect Device	Self Refresh Exit

Table 16 MRS command (Mode Register Set) Supported by the MTXC.

Table 16. Command Fields

A11	A10	A9	A8	A7	A[6:4]	A3	A[2:0]
0	0	0	0	0	CL	WT	BL

CAS Latency Field (CL)		Wrap Type Field (WT)		Burst Length Field (BL)	
Bits[6:4]	CAS Latency	Bit 3	Type	Bits[2:0]	Burst Length
010	2	0	X	010	4
011	3	1	Interleave	All Other	X
All Other	X	The linear order addressing is not supported.			

#### NOTES:

1. X=Don't Care. These Modes are Don't Care for MTXC specific implementation.

#### 4.3.6. AUTO DETECTION

#### 4.3.7. DRAM PERFORMANCE

For write cycles, the measurement is broken up into two parts. The first part consists of the rate of posting data in to the CPU to DRAM posted write buffers. This is measured from ADS# to BRDY#. The second part consists of the retire rate from posted write buffers to the DRAM. The leadoff for retiring is measured from the clock after BRDY# assertion to the CAS# assertion.

Table 17 lists the performance summary for 60 ns EDO/FPM DRAMs. The four row column is assuming each row is populated with a maximum of 16, x4 devices=64 DRAM devices. The five row column is assuming each of the first four rows is populated with a maximum of 16, x4 devices and the fifth row is populated with a maximum of eight, x8 devices=72 DRAM devices. The six row column assumes that each of the six rows can be populated with a maximum of 16, x4 devices.

The FELO and SLD bits are used to control the leadoff for read cycles (page hit, row miss, and page miss). Each bit removes one clock from the leadoff, when enabled. Note that FELO impacts EDO only and must be disabled for FPM. The DLT bits are used to control the base starting point for the leadoff for read/write cycles (page miss and row miss, only).



Table 17. EDO/ Standard Page Mode Performance Summary (60 ns DRAMs)

Processor Cycle Type (pipelined)	60/66 MHz w/ four rows	60/66 MHz w/ five rows	60/66 MHz w/ six rows Buffered	DRAM Type
Burst Read Page Hit	5-2-2-2	6-3-3-3	6-3-3-3	EDO
Read Row Miss <sup>1</sup>	8-2-2-2	9-3-3-3	10-3-3-3	EDO
Read Page Miss	11-2-2-2	12-3-3-3	13-3-3-3	EDO
Back-to-Back Burst Reads Page Hit	5-2-2-2-3-2-2-2	6-3-3-3-4-3-3-3	6-3-3-3-4-3-3-3	EDO
Burst Read Page Hit	6-3-3-3	7-4-4-4	7-4-4-4	FPM
Burst Read Row Miss <sup>1</sup>	9-3-3-3	9-4-4-4	9-4-4-4	FPM
Burst Read Page Miss	12-3-3-3	12-4-4-4	12-4-4-4	FPM
Back-to-Back Burst Read Page Hit	6-3-3-3-3-3-3-3	7-4-4-4-4-4-4-4	7-4-4-4-4-4-4-4	FPM
Write Page Hit <sup>2,3,4</sup>	3	3	3	EDO/FPM
Write Row Miss <sup>2,3,4</sup>	6	6	7	EDO/FPM
Write Page Miss <sup>2,3,4</sup>	9	9	10	EDO/FPM
Posted Write <sup>3,4</sup>	3-1-1-1	3-1-1-1	3-1-1-1	EDO/FPM
Write retire rate from Posted Write Buffer	-2-2-2	-3-3-3	-3-3-3	EDO/FPM
Single writes	2	2	3	EDO/FPM
Reg 56h, Bit 4 (SLD) <sup>5</sup>	0	0	0	EDO/FPM
Reg 56h, Bit 5 (FELO) <sup>6</sup>	1	1	1	EDO
Reg 56h, Bit 5 (FELO) <sup>6</sup>	0	0	0	FPM
Reg 58h, Bits[6:5] (DRBT)	2	1	1	EDO/FPM
Reg 58h, Bits[4:3] (DWBT)	2	1	1	EDO/FPM
Reg 58h, Bits[1:0] (DLT)	1	1	0	EDO/FPM
Reg 56h, Bit 6 (RRA)	0	0	0	EDO/FPM

**NOTES:**

1. The row miss cycles assume that the new page is closed from the prior cycle. Due to the MA[13:0] to RAS# setup requirements, if the page is open, 2 clocks are added to the leadoff.
2. This cycle timing assumes the write buffer(DWB) is empty.
3. Write timing is measured from the clock after BRDY# is returned to the CPU up to CAS# assertion for that cycle.
4. Write data is always posted as 3-1-1-1 (ADS# to BRDY#), if write buffers is available.
5. This bit (SLD) should be set to a 1 (speculative leadoff disable) in systems with cache and to 0 in systems without cache.
6. When set to 1, enables fast timing for EDO timing only. Enables one HCLK pull in for page hit, page miss, and row miss cycles.

Table 18 lists the performance summary for SDRAM. The CL=3 column represents a CAS latency of 3 part with a RAS to CAS (Trcd) of two clocks. The CL=2 column represents a CAS latency of two part. The performance numbers in Table 18 assume each row is populated with a maximum of eight, x8 devices=40 SDRAM devices.

The SLD bit (page hit, row miss, and page miss) is used to control the leadoff for read cycles. This bit removes one clock from the leadoff, when enabled.

**Table 18. SDRAM Performance Summary**

Processor Cycle Type	60/66 MHz CL=3 Five Rows (Max)	60/66 MHz CL=2 Five Rows (Max)
Burst Read Page Hit	7-1-1-1	6-1-1-1
Read row Miss <sup>1</sup>	9-1-1-16	8-1-1-1
Read Page Miss	12-1-1-16	11-1-1-1
Back-to-Back Burst Reads Page Hit	7-1-1-1 2-1-1-1	6-1-1-1 2-1-1-1
Write Page Hit <sup>2,3</sup>	3	3
Write Row Miss <sup>2,3</sup>	6	5
Write Page Miss <sup>2,3</sup>	9	8
Posted Write <sup>2,3</sup>	3-1-1-1	3-1-1-1
Write retire rate from Posted Write Buffer	-1-1-1	-1-1-1
Reg 54h, Bit 5 (RCO) <sup>5</sup>	1	0
Reg 54h, Bit 4 (CL)	0	1
Reg 54h, Bit 3 (RT)	0	1
Reg 56h, Bit 4 (SLD) <sup>4</sup>	0	0

**NOTES:**

1. The row miss cycle assumes that the new page is closed from the prior cycle.
2. This cycle timing assumes the write buffer(DWB) is empty.
3. Write data is always posted as 3-1-1-1 (ADS# to BRDY#), if write buffers is available.
4. This bit (SLD) must be set to a 1 (speculative leadoff disable) in systems with cache and to 0 in systems without cache.
5. For a CL=3 part that can not meet a RAS to CAS timing (Trcd) of two HCLKs, RCO can be set to 0. This will add an HCLK to the leadoff cycle for Row miss and Page miss cycles.

#### 4.3.8. DRAM REFRESH

MTXC supports CAS-before-RAS# (CBR) refresh and Self refresh. The refresh rate is controlled via the DRAM Refresh Rate field in the DRAM Control Register (DRAMC). When a refresh request is generated, it is placed in a four entry queue. The DRAM controller services a refresh request when the refresh queue is not empty and the controller has no other requests pending. When the refresh queue is full, refresh becomes the highest priority request and will be serviced next by the controller.

Refresh is only performed on rows that are populated (i.e., "smart refresh"). The controller determines which rows are populated by looking at the DRB registers. Note that Refresh has to be disabled before the refresh rate is changed.

Refer to bit 5 in the MCTL register (offset 79h) for suspend refresh information.

### 4.4. PCI CLK Control (CLKRUN#)

#### 4.4.1. CLOCKING STATES

There are three main states in the clocking protocol:

- **Clock Running:** The clock is running and the bus is operational.
- **About to Stop:** The central resource has indicated on the CLKRUN# line that the clock is about to stop.
- **Clock Stopped:** The clock is stopped with CLKRUN# being monitored for a restart

#### 4.4.2. OPERATION

The MTXC is a CLKRUN# Master device and behaves according to the rules for a master device. The PIIX4 companion chip controls the clocks in the system and is the CLKRUN# Central Resource. Please refer to the latest "PCI Mobile Design Guide" for more information.

### 4.5. SMRAM Memory Space

The MTXC supports the use of main memory as System Management RAM (SMRAM), enabling the use of System Management Mode. The MTXC supports two SMRAM options; Compatible SMRAM (C\_SMRAM) and Extended SMRAM (E\_SMRAM).

#### 4.5.1. COMPATIBLE SMRAM (C\_SMRAM)

This is the traditional SMRAM feature supported in Intel PCIs. When this function is enabled via C\_BASE\_SEG[2:0]=010 and G\_SMRAME=1 of the SMRAMC register, the MTXC reserves 000A0000h through 000BFFFFh (A and B segments) of the main memory for use as Noncacheable SMRAM. CPU accesses to segments A and B while not in SMM (i.e., SMIACK# is negated) are always forwarded to the PCI bus. CPU accesses to segments A and B while in SMM (i.e., SMIACK# is asserted) are forwarded to either DRAM or PCI bus, depending on the value of bits[6:0] of the SMRAMC register. PCI masters cannot access the SMRAM area of the main memory. When a PCI master tries to access the SMRAM space, the MTXC does not respond to the PCI cycle (i.e., DEVSEL# is not asserted).

#### 4.5.2. EXTENDED SMRAM (E\_SMRAM)

This feature in the MTXC extends the SMRAM space up to 1 Mbytes and provide writeback cacheability. This feature requires that SMI handlers execute above 1 Mbytes which will require rewriting the existing code to

**PRELIMINARY**



operate properly above 1 Mbytes. However once this is done, then SMI handlers execute at full processor performance.

An error status bit is set in the Extended SMRAM Control register if the CPU tries to access the extended SMRAM space while SMI $\overline{ACT}\#$  is negated and D\_OPEN bit is 0. This access is forwarded to PCI bus and may result in a Master Abort condition.

Extended SMRAM feature allows up to 1 Mbyte of SMRAM space to be writeback cacheable. This memory space consists of any DRAM not used by the system (as shadow space etc.) between 640 Kbytes and 1 Mbyte (this memory space is referred to as High Memory in this document), and an optional block of memory referred to as the "TSEG". The TSEG is either a 128 Kbyte, 256 Kbyte, 512 Kbytes, or 1 Mbytes block of memory, as defined by TSEG\_SZ[1:0] of the SMRAMC register. When TSEG is enabled, the TSEG block of memory is disabled from the top of memory and the system BIOS should report a main memory size of (memorize - TSEG) to the OS.

The two areas of memory available for SMRAM when Extended SMRAM is enabled are:

Physical Address	DRAM Address
100A0000h to 100FFFFFFh	000A0000h to 000FFFFFFh (High Mem)
10000000h plus TOM minus TSEG_SZ to 10000000h plus TOM	TOM minus TSEG_SZ to TOM (TSEG)

Extended SMRAM option has the following DRAM memory available to it:

**Table 19. Extended SMRAM DRAM memory regions**

DRAM Area	Size/Availability
A Segment	64 Kbytes always available if enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
B Segment	64 Kbytes always available if enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
C Segment	64 Kbytes available if not used for shadowing (as defined by PAM register) and enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
D Segment	64 Kbytes available if not used for shadowing (as defined by PAM register) and enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
E Segment	64 Kbytes available if not used for shadowing (as defined by PAM register) and enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
F Segment	64 Kbytes only available for suspend/resume (as defined by PAM register) if enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
TSEG	128K, 256K, 512K or 1M bytes available if enabled (i.e., TSEG_EN=1 and G_SMRAME=1)

As with the Compatible SMRAM solution, MTXC does not claim any bus master access to the Extended SMRAM memory ranges defined above. The CPU can access these memory ranges by one of the following mechanisms:

- The processor generating an access to one of the defined memory ranges while in the SMM (SMIACK# is active). A processor access to any of the defined ranges while not in SMM (SMIACK# is inactive) and with the D\_OPN bit reset will be forwarded to PCI bus and a status bit is set in the SMRAMC register.
- The processor generating an access to one of the defined memory ranges while the D\_OPN bit is set.
- Any modified write access of the processor is allowed to write into the SMRAM space, regardless of the state of the D\_OPN, D\_CLS, or SMIACK# signals.

The cacheability of SMRAM space is dependent on how much physical DRAM is available in the system. If the system has less than 32 Mbytes of DRAM, the SMRAM is cached in both the L1 and L2. If the system has more than 32 Mbytes of DRAM, the SMRAM is cached in only the L1.

#### 4.5.3. SMRAM PROGRAMMING CONSIDERATIONS

When using the Extended SMRAM configuration, the SMI handler software must be extremely careful when accessing DRAM memory in the 100A0000h to 100FFFFFFh memory range. First, if this area of memory is accessed while the CPU is not in SMM mode and the D\_OPN bit is not set, the MTXC will forward the cycle to PCI bus which may cause a fatal system error and system shutdown. Second, only areas within the 100A0000h to 100FFFFFFh region that have been selected as SMRAM space should be accessed; otherwise, the L1 and L2 caches will become incoherent, which will cause a future system error. Any memory in normal DRAM space that is not used in OS or application space can be used as SMRAM memory.

#### 4.6. Low Power States

MTXC supports five types of low power states: Chip Standby, Power On Suspend (POS), Suspend to RAM (STR), Suspend to Disk (STD), and dynamic stop clock. The Table 20 summarizes the various MTXC's Low power states.

Table 20. 430TX Low Power State Summary

PM Mode	Description	Exit Latency Target
Chip Standby	When MTXC's CPU and PCI busses are both idle, MTXC enters this state.	No delay
Dynamic Stop Clock	MTXC provides provisions that enable transitioning the CPU in and out of the stop clock state in an active system. This includes the ability to disable the system arbiter and transition the memory controller in and out of the suspend refresh state.	<10 ms
Powered On Suspend (POS)	System PLLs are powered down, only running clock is the RTC clock and the SUSCLK. MTXC maintains DRAM refresh using SUSCLK.	<10 ms
Suspend to RAM (STR)	CPU complex (CPU and L2) and PCI interface are powered off. Only the RTC clock and SUSCLK are running. MTXC maintains DRAM refresh using SUSCLK.	~1 sec
Suspend to Disk(STD)	CPU complex (CPU and L2), DRAM and PCI interface are powered off.	~30 sec

The 430TX system maintains a very low power CPU complex by utilizing the different power down features available from the CPU, cache data RAMs and utilizing leading edge low power design techniques in the 430TX system components. The 430TX components work in unison to dynamically control the CPU complexes power state without adversely affecting performance. The following gives a brief description of how the 430TX system components achieve these low power states.

The MTXC and PIIX4 work in unison to maintain a very low power L2 subsystem without adversely affecting peak performance.

#### NOTE

There are some system restrictions when DRAM Cache is implemented in a system that supports STP\_CLK, POS, and STR power management modes. Since KRQAK is not implemented in the "Suspend Well," the correct operation of KRQAK is not guaranteed when the system enters the above mentioned power management modes. To avoid data corruption in the L2 cache, a system that implements the STP\_CLK, POS, and STR modes must abide by the following rules:

1. Before entering these power management modes, the DRAM cache must be flushed so that all modified lines end up in system memory.
2. After exiting these power management modes, the DRAM Cache must be reinitialized.

#### 4.6.1. CHIP STANDBY

The MTXC also supports a chip standby mode. When the MTXC determines that both its CPU interface and PCI interface are idle, it will dynamically place itself into a very low power state. While in chip standby state the MTXC is able to respond to new CPU or PCI bus master accesses with no performance penalty. This provides very optimized power/performance characteristics because the CPU interface are idle for large periods of time. The MTXC enters Chip Standby mode when the following conditions are true:

- Host Bus idle
- PCI bus Idle
- Normal Mode (i.e., not Test Mode)
- Not in RESET state
- Internal operations idle

Entering the Chip Standby state is not dependent on any timer expiration. When the above conditions are met, the MTXC can enter the chip standby state as soon as it can.

#### 4.6.2. SUSPEND/RESUME

The MTXC supports POS, STR, STD and SOFF (Soft Off) suspend states. The MTXC supports the POS mode by maintaining all of its power planes when in the suspend state. The MTXC supports the STR modes by isolating its CPU and PCI interfaces, and only maintaining the DRAM refresh off the SUSCLK signal. When exiting the STR modes, the MTXC's core well is reset and its context is lost (the power management context is not lost however). The MTXC supports the STD and SOFF modes by being totally powered off.



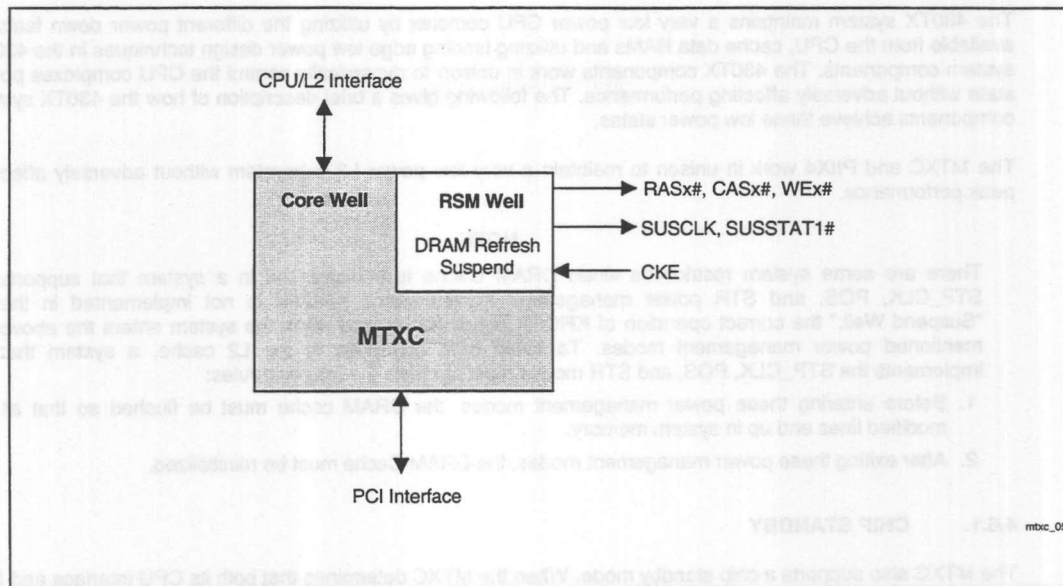


Figure 9. MTXC Power Planes

#### 4.6.2.1. Power Transition Changes

The MTXC supports several suspend modes that support the PIIX4 system suspend states. Table 21 illustrates what suspend mode the MTXC enters upon the appropriate PIIX4 suspend mode.

Table 21. Power Transition States

PIIX4 Suspend State	MTXC Suspend State	MTXC Description
POS	PonS	All interfaces enabled, clocks stopped.
STR	PoffS	CPU, L2, PCI interfaces disabled
STD	Off	Chip is off.
Off/Soft Off	Off	Chip is off.

The core logic should be reset when the PCI bus is reset. This means that the refresh logic and power sequencing logic is not reset during resumes (part of the resume well).

#### 4.7. PCI Interface

The MTCX integrates a high performance interface to the PCI local bus taking full advantage of the high bandwidth and low latency of PCI. The MTCX is fully PCI 2.1 compliant. Table 22 lists the PCI bus commands supported. Five PCI masters are supported by the integrated arbiter including the PIIX4 and four general PCI masters. The MTCX acts as a PCI master for CPU accesses to PCI. The PCI bus is clocked at one half the frequency of the CPU clock. This divided synchronous interface minimizes latency for CPU-to-PCI cycles and PCI-to-main memory cycles.

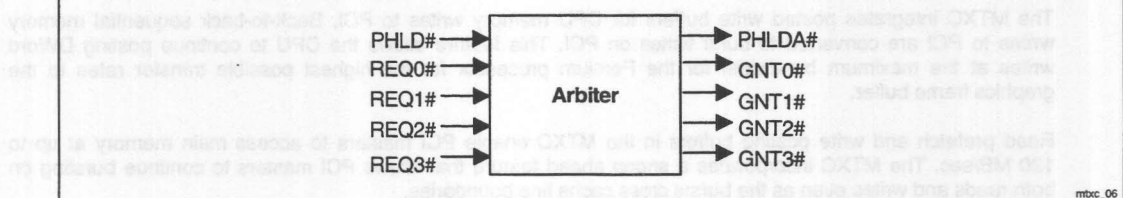
The MTCX integrates posted write buffers for CPU memory writes to PCI. Back-to-back sequential memory writes to PCI are converted to burst writes on PCI. This feature allows the CPU to continue posting DWord writes at the maximum bandwidth for the Pentium processor for the highest possible transfer rates to the graphics frame buffer.

Read prefetch and write posting buffers in the MTCX enable PCI masters to access main memory at up to 120 MB/sec. The MTCX incorporates a snoop ahead feature that allows PCI masters to continue bursting on both reads and writes even as the bursts cross cache line boundaries.

The MTCX forwards each of the CPU shutdown, Halt, and Stop Grant cycles to the PCI bus as special cycles. These cycles are terminated on PCI as master abort and a BRDY# is returned to the CPU. The Stop Grant cycle is propagated with 0002h in the message field and 0012h in the message dependent data field.

Table 22. PCI Commands

C/BE#	Command	Target Support	Initiator Support
0000	Interrupt Acknowledge	NO	YES
0001	Special cycle	NO	YES
0010	I/O read	YES	YES
0011	I/O write	YES	YES
0100	reserved	NO	NO
0101	reserved	NO	NO
0110	Memory read	YES	YES
0111	Memory write	YES	YES
1000	reserved	NO	NO
1001	reserved	NO	NO
1010	Configuration Read	NO	YES
1011	Configuration Write	NO	YES
1100	Memory Read Multiple	As Memory Read	NO
1101	Dual Address Cycle	NO	NO
1110	Memory Read Line	As Memory Read	NO
1111	Memory Write and Invalidate	As Memory Write	NO



**Figure 10. PCI Arbiter**

#### 4.8.1. PRIORITY SCHEME AND BUS GRANT

The highest priority requester is determined by a fixed order queue together with a highest priority pointer. Although the priority ring is fixed, the highest priority pointer moves to determine which PCI agent is at the top (and bottom) of the queue. The arbiter counts three grant assertions to requesters different than the one it is currently granting (and all grants within MTT are collapsed to one) to decide when it's time to let the host in.

The grant signals (GNT#) are normally negated after recognition of FRAME# assertion, or 16 PCLKs from grant assertion, if no cycle has started.



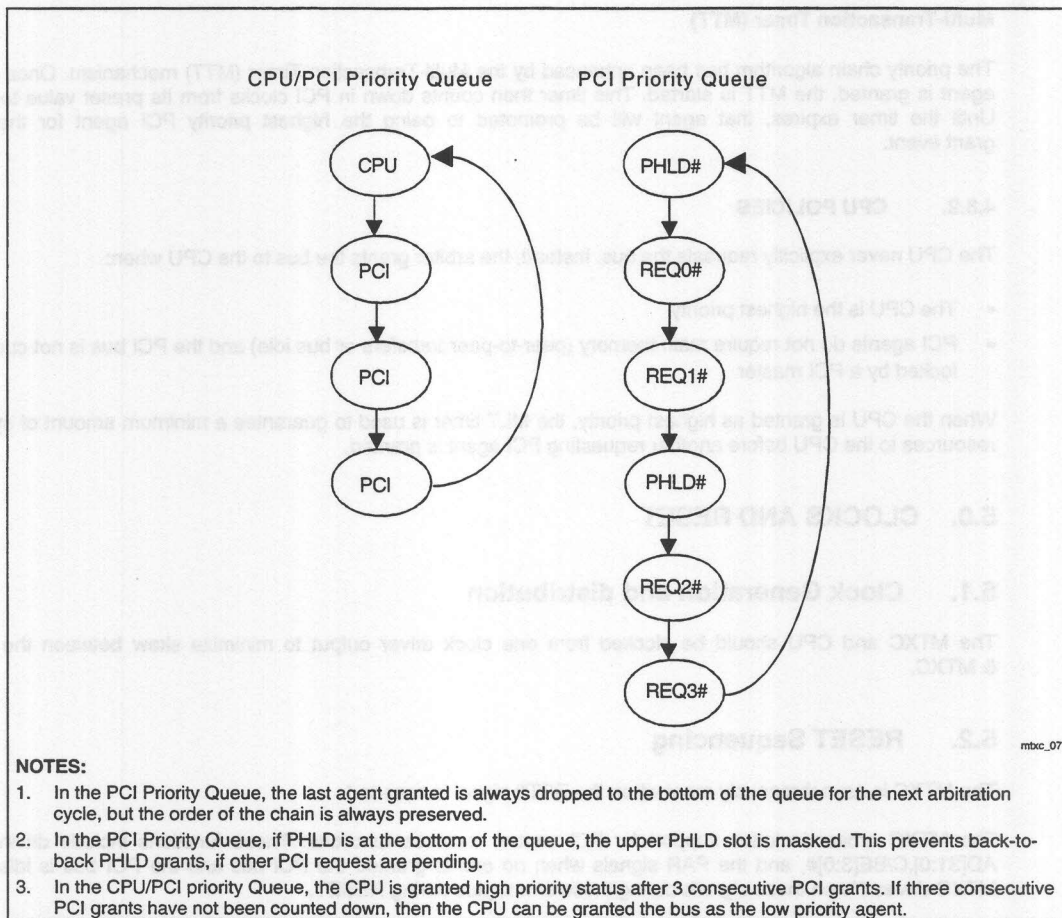


Figure 11. Arbitration Priority Rotation

### Multi-Transaction Timer (MTT)

The priority chain algorithm has been enhanced by the Multi-Transaction Timer (MTT) mechanism. Once a PCI agent is granted, the MTT is started. This timer then counts down in PCI clocks from its preset value to zero. Until the timer expires, that agent will be promoted to being the highest priority PCI agent for the next grant event.

#### 4.8.2. CPU POLICIES

The CPU never explicitly requests the bus. Instead, the arbiter grants the bus to the CPU when:

- The CPU is the highest priority
- PCI agents do not require main memory (peer-to-peer transfers or bus idle) and the PCI bus is not currently locked by a PCI master

When the CPU is granted as highest priority, the MTT timer is used to guarantee a minimum amount of system resources to the CPU before another requesting PCI agent is granted.

### 5.0. CLOCKS AND RESET

#### 5.1. Clock Generation and distribution

The MTXC and CPU should be clocked from one clock driver output to minimize skew between the CPU & MTXC.

#### 5.2. RESET Sequencing

The MTXC is asynchronously reset when the RST# signal is asserted.

The MTXC arbiter includes support for PCI central resource functions. These functions include driving the AD[31:0], C/BE[3:0]#, and the PAR signals when no one is granted the PCI bus and the PCI bus is idle. The MTXC drives 0's on these signals during these times, plus during RESET.

## 6.0. PINOUT INFORMATION

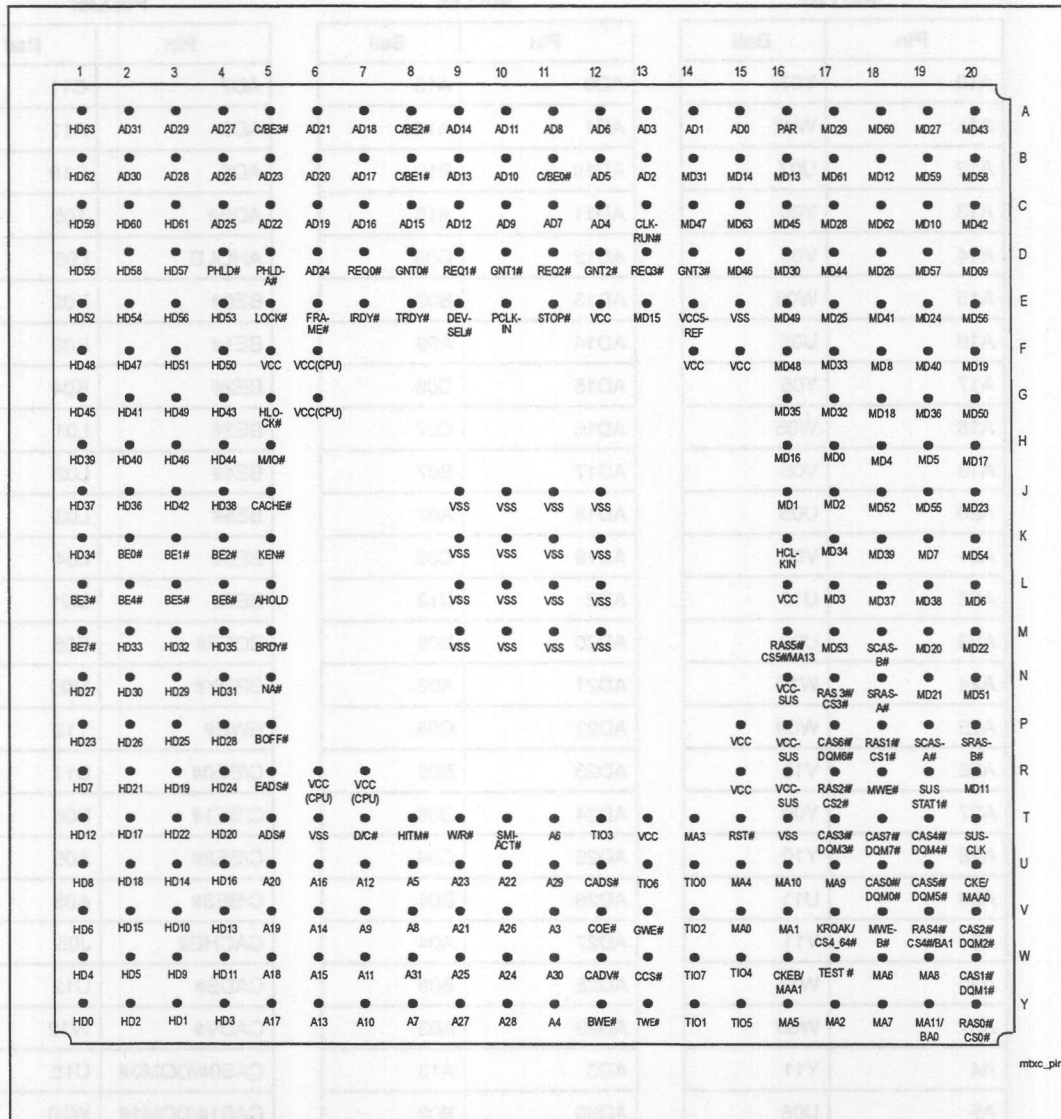


Figure 12. MTXC Pinout (Top View)



Table 23. MTXC Alphabetical  
Pin List

Pin	Ball
A10	Y07
A11	W07
A12	U07
A13	Y06
A14	V06
A15	W06
A16	U06
A17	Y05
A18	W05
A19	V05
A20	U05
A21	V09
A22	U10
A23	U09
A24	W10
A25	W09
A26	V10
A27	Y09
A28	Y10
A29	U11
A3	V11
A30	W11
A31	W08
A4	Y11
A5	U08
A6	T11
A7	Y08
A8	V08
A9	V07

Table 23. MTXC Alphabetical  
Pin List

Pin	Ball
AD0	A15
AD1	A14
AD10	B10
AD11	A10
AD12	C09
AD13	B09
AD14	A09
AD15	C08
AD16	C07
AD17	B07
AD18	A07
AD19	C06
AD2	B13
AD20	B06
AD21	A06
AD22	C05
AD23	B05
AD24	D06
AD25	C04
AD26	B04
AD27	A04
AD28	B03
AD29	A03
AD3	A13
AD30	B02
AD31	A02
AD4	C12
AD5	B12
AD6	A12

Table 23. MTXC Alphabetical  
Pin List

Pin	Ball
AD7	C11
AD8	A11
AD9	C10
ADS#	T05
AHOLD	L05
BE0#	K02
BE1#	K03
BE2#	K04
BE3#	L01
BE4#	L02
BE5#	L03
BE6#	L04
BE7#	M01
BOFF#	P05
BRDY#	M05
BWE#	Y12
C/BE0#	B11
C/BE1#	B08
C/BE2#	A08
C/BE3#	A05
CACHE#	J05
CADS#	U12
CADV#	W12
CAS0#/DQM0#	U18
CAS1#/DQM1#	W20
CAS2#/DQM2#	V20
CAS3#/DQM3#	T17
CAS4#/DQM4#	T19
CAS5#/DQM5#	U19

Table 23. MTXC Alphabetical Pin List

Pin	Ball
CAS6#/DQM6#	P17
CAS7#/DQM7#	T18
CCS#	W13
CKE/MAA0	U20
CKEB/MAA1	W16
CLKRUN#	C13
COE#	V12
D/C#	T07
DEVSEL#	E09
EADS#	R05
FRAME#	E06
GNT0#	D08
GNT1#	D10
GNT2#	D12
GNT3#	D14
GWE#	V13
HCLKIN	K16
HD0	Y01
HD1	Y03
HD10	V03
HD11	W04
HD12	T01
HD13	V04
HD14	U03
HD15	V02
HD16	U04
HD17	T02
HD18	U02
HD19	R03

Table 23. MTXC Alphabetical Pin List

Pin	Ball
HD2	Y02
HD20	T04
HD21	R02
HD22	T03
HD23	P01
HD24	R04
HD25	P03
HD26	P02
HD27	N01
HD28	P04
HD29	N03
HD3	Y04
HD30	N02
HD31	N04
HD32	M03
HD33	M02
HD34	K01
HD35	M04
HD36	J02
HD37	J01
HD38	J04
HD39	H01
HD4	W01
HD40	H02
HD41	G02
HD42	J03
HD43	G04
HD44	H04
HD45	G01

Table 23. MTXC Alphabetical Pin List

Pin	Ball
HD46	H03
HD47	F02
HD48	F01
HD49	G03
HD5	W02
HD50	F04
HD51	F03
HD52	E01
HD53	E04
HD54	E02
HD55	D01
HD56	E03
HD57	D03
HD58	D02
HD59	C01
HD6	V01
HD60	C02
HD61	C03
HD62	B01
HD63	A01
HD7	R01
HD8	U01
HD9	W03
HITM#	T08
HLOCK#	G05
IRDY#	E07
KEN#	K05
KRQAK/ CS4_64#	V17
LOCK#	E05

PRELIMINARY

Table 23. MTXC Alphabetical  
Pin List

Pin	Ball
M/IO#	H05
MA0	V15
MA1	V16
MA10	U16
MA11/BA0	Y19
MA2	Y17
MA3	T14
MA4	U15
MA5	Y16
MA6	W18
MA7	Y18
MA8	W19
MA9	U17
MD0	H17
MD1	J16
MD10	C19
MD11	R20
MD12	B18
MD13	B16
MD14	B15
MD15	E13
MD16	H16
MD17	H20
MD18	G18
MD19	F20
MD2	J17
MD20	M19
MD21	N19
MD22	M20

Table 23. MTXC Alphabetical  
Pin List

Pin	Ball
MD23	J20
MD24	E19
MD25	E17
MD26	D18
MD27	A19
MD28	C17
MD29	A17
MD3	L17
MD30	D16
MD31	B14
MD32	G17
MD33	F17
MD34	K17
MD35	G16
MD36	G19
MD37	L18
MD38	L19
MD39	K18
MD4	H18
MD40	F19
MD41	E18
MD42	C20
MD43	A20
MD44	D17
MD45	C16
MD46	D15
MD47	C14
MD48	F16
MD49	E16

Table 23. MTXC Alphabetical  
Pin List

Pin	Ball
MD5	H19
MD50	G20
MD51	N20
MD52	J18
MD53	M17
MD54	K20
MD55	J19
MD56	E20
MD57	D19
MD58	B20
MD59	B19
MD6	L20
MD60	A18
MD61	B17
MD62	C18
MD63	C15
MD7	K19
MD8	F18
MD9	D20
MWE#	R18
MWEB#	V18
NA#	N05
PAR	A16
PCLKIN	E10
PHLD#	D04
PHLDA#	D05
RAS0#/CS0#	Y20
RAS1#/CS1#	P18
RAS2#/CS2/#	R17



Table 23. MTXC Alphabetical Pin List

Pin	Ball
RAS3#/CS3#	N17
RAS4#/CS4#/ BA1	V19
RAS5#/CS5#/ MA13	M16
REQ0#	D07
REQ1#	D09
REQ2#	D11
REQ3#	D13
RST#	T15
SCASA#	P19
SCASB#	M18
SMIACK#	T10
SRASA#	N18
SRASB#	P20
STOP#	E11
SUSCLK	T20
SUSSTAT1#	R19

Table 23. MTXC Alphabetical Pin List

Pin	Ball
TEST#	W17
TIO0	U14
TIO1	Y14
TIO2	V14
TIO3	T12
TIO4	W15
TIO5	Y15
TIO6	U13
TIO7	W14
TRDY#	E08
TWE#	Y13
W/R#	T09
Vcc	F05, L16, R15, F15, E12, P15, F14, T13

Table 23. MTXC Alphabetical Pin List

Pin	Ball
Vcc (CPU)	F06, G06, R07, R06
Vcc (SUS)	R16, N16, P16
Vcc5REF	E14
Vss	E15, J9, J10 J11, J12, K09, K10, K11, K12, L09, L10, L11, L12, M09, M10, M11, M12, T06, T16

## 7.0. MTXC PACKAGE INFORMATION

This specification outlines the mechanical dimensions for the MTXC. The package is a 324 pin ball grid array (BGA).

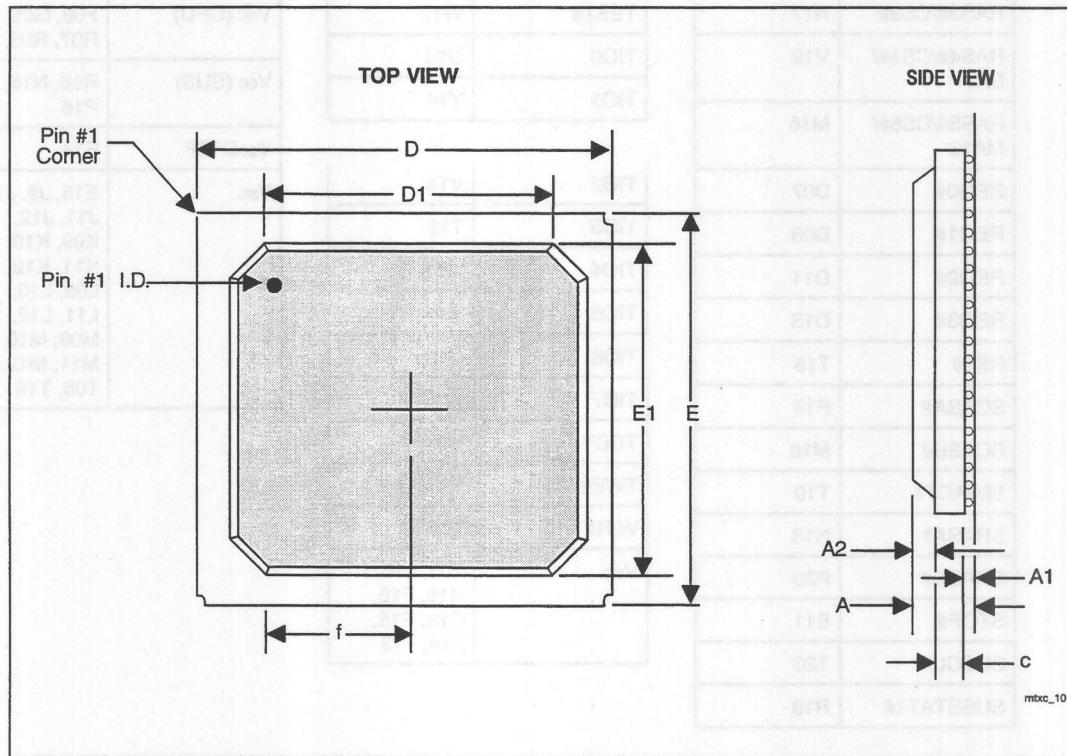


Figure 13. MTXC 324-pin Ball Grid Array (BGA)

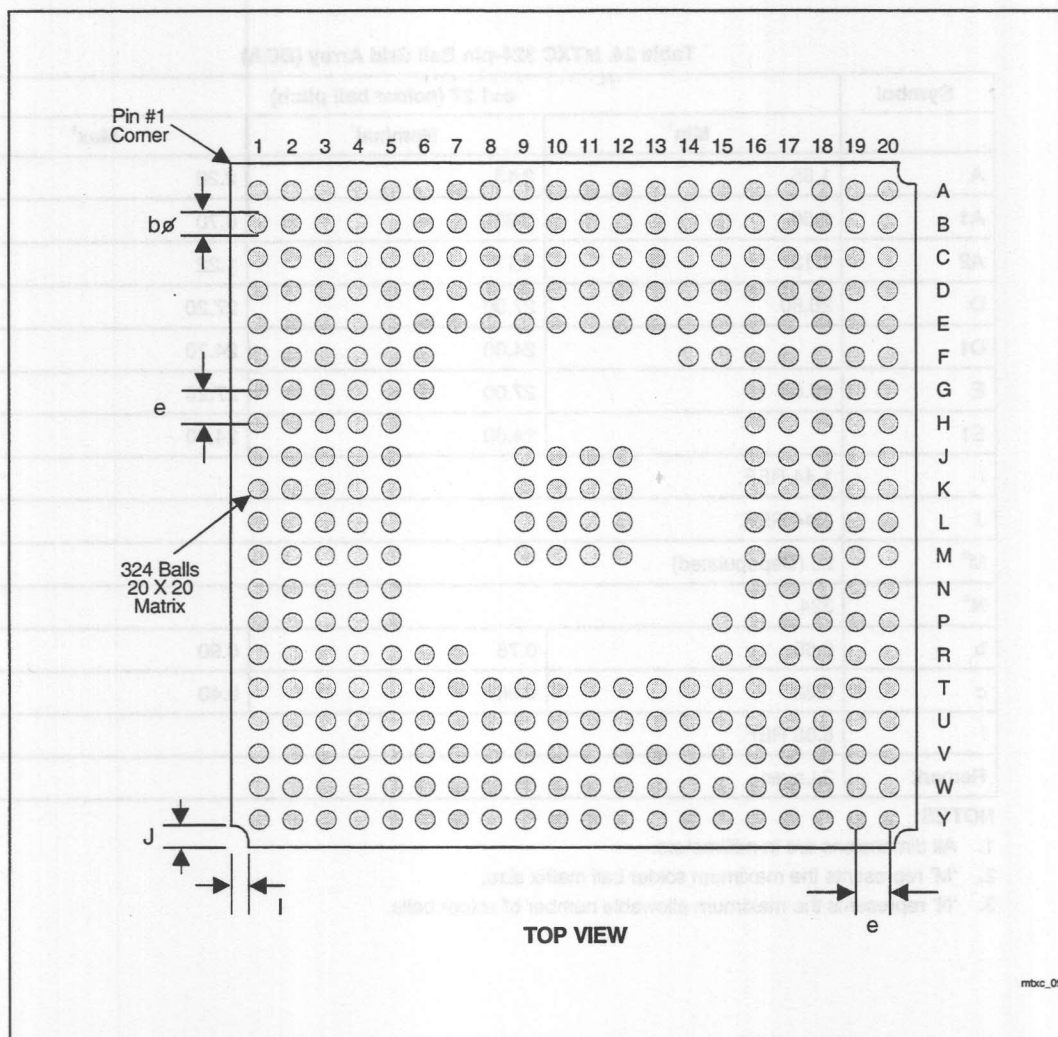


Figure 14. MTXC 324-pin Ball Grid Array (BGA) Ball Pattern



Table 24. MTCX 324-pin Ball Grid Array (BGA)

Symbol	e=1.27 (solder ball pitch)		
	Min <sup>1</sup>	Nominal <sup>1</sup>	Max <sup>1</sup>
A	1.95	2.13	2.28
A1	0.50	0.60	0.70
A2	1.12	1.17	1.22
D	26.80	27.00	27.20
D1		24.00	24.70
E	26.80	27.00	27.20
E1		24.00	24.70
I	1.44 REF.		
J	1.44 REF.		
M <sup>2</sup>	20 (Depopulated)		
N <sup>3</sup>	324		
b	0.60	0.76	0.90
c	0.32	0.36	0.40
f	8.05 REF.		
Remark	2 Layer		

**NOTES:**

1. All dimensions are in millimeters.
2. 'M' represents the maximum solder ball matrix size.
3. 'N' represents the maximum allowable number of solder balls.

## 8.0. TESTABILITY

### 8.1. NAND Tree Mode

A NAND tree mode is provided for Automated Test Equipment (ATE) board level testing. The NAND tree allows the tester to set the connectivity of each of the MTC's signal pins. In Mobile/desktop mode, the NAND tree mode is activated by driving the test pin TEST# low when REQ# pins are at 0010. If TEST# is negated at any time, the test mode is deactivated and the MTC goes back to normal operation. There is no guarantee that upon re-entering normal operation the chip will function properly, if the test mode was entered while the MTC was not in a completely idle state.

The MTC has several test modes to improve board manufacturing. If the TEST# signal is asserted (driven low), the value on the REQ[3:0]# indicates the test mode to enable. The test mode enabled at the falling edge of TEST# will remain enabled until TEST# is negated.

Table 25 shows each test mode and the value of REQ[3:0] required to enable it. All other values of REQ[3:0]# while TEST# is active, are reserved and should not be asserted by the customer.

Table 25. Test Modes

REQ[3:0]#	TEST#	PHLD#	TEST Mode	Description
0010	0	x	NAND Chain	Float outputs, enable NAND chains on GNT[3:0]#
1110	0	1	ID/REV code	Drives Device ID on AD[31:16] and revision ID on AD[7:0]
1110	0	0	MID Code	Drives Manufacture ID on AD[31:0]
1111	0	x	Disable test mode <sup>1</sup>	Disables any active test mode, puts MTC back into normal mode

#### NOTES:

1. It is recommended to assert RST# if this mode is used, to guarantee pins and PCIset will function normally.

### 8.2. NAND Chain Mode

In NAND Tree mode, all outputs are tri-stated, except for GNT#[3:0]. These pins contain the NAND Chain. Note, also, that the internal pull-ups and pull-downs are still active. Because of the 282 pins in the NAND Chain, it must be separated into 4 chains. Two chains contain 72 pins each, 1 chain contains 70 pins, and 1 chain contains 68 pins. The MTC remains in this mode until a new test mode is selected or RST# is asserted. The HCLK and PCLK are part of the NAND Chain and *must* be deactivated during this test.

HCLK and PCLK need to run for a few clocks in the beginning to put the MTXC in the NAND chain mode. During the testing of chains 2 and 3, SUSSTAT# will be held high throughout the test. RST#, TEST#, and SUSSTAT1# are not part of the NAND chain. The following tables show the pin order for each chain:

Table 26. Chain #0 (GNT#0)

Pin Name	Chain Element
A25	CH0_00
A7	CH0_01
A10	CH0_02
A21	CH0_03
A23	CH0_04
SMIACK#	CH0_05
A31	CH0_06
A18	CH0_07
HD3	CH0_08
A12	CH0_09
A14	CH0_10
HD11	CH0_11
A19	CH0_12
A16	CH0_13
HITM#	CH0_14
HD13	CH0_15
D/C#	CH0_16
HD0	CH0_17
HD10	CH0_18
HD16	CH0_19
HD6	CH0_20
HD14	CH0_21
BOFF#	CH0_22
HD18	CH0_23

Table 26. Chain #0 (GNT#0)

Pin Name	Chain Element
HD24	CH0_24
HD8	CH0_25
HD19	CH0_26
HD7	CH0_27
HD31	CH0_28
HD26	CH0_29
HD27	CH0_30
HD33	CH0_31
AHOLD	CH0_32
BE5#	CH0_33
BE6#	CH0_34
HD34	CH0_35
BE2#	CH0_36
BE0#	CH0_37
HD37	CH0_38
BE1#	CH0_39
HD36	CH0_40
HD41	CH0_41
HD52	CH0_42
CACHE#	CH0_43
HD47	CH0_44
HD44	CH0_45
HD49	CH0_46
HD54	CH0_47

Table 26. Chain #0 (GNT#0)

Pin Name	Chain Element
HD55	CH0_48
HD57	CH0_49
HLOCK#	CH0_50
HD53	CH0_51
HD60	CH0_52
HD62	CH0_53
HD61	CH0_54
AD30	CH0_55
AD25	CH0_56
AD22	CH0_57
AD24	CH0_58
AD27	CH0_59
AD19	CH0_60
C/BE3#	CH0_61
REQ0#	CH0_62
AD20	CH0_63
AD21	CH0_64
TRDY#	CH0_65
AD16	CH0_66
C/BE2#	CH0_67
C/BE1#	CH0_68
AD14	CH0_69
AD12	CH0_70
AD13	CH0_71



Table 27. Chain #1 (GNT#1)

Pin Name	Chain Element
A24	CH1_00
A27	CH1_01
A26	CH1_02
A13	CH1_03
A8	CH1_04
W/R#	CH1_05
A11	CH1_06
A17	CH1_07
A15	CH1_08
A5	CH1_09
A9	CH1_10
HD1	CH1_11
HD9	CH1_12
A20	CH1_13
HD2	CH1_14
HD5	CH1_15
HD4	CH1_16
ADS#	CH1_17
HD15	CH1_18
EADS#	CH1_19
HD20	CH1_20
HD17	CH1_21
HD22	CH1_22
HD12	CH1_23

Table 27. Chain #1 (GNT#1)

Pin Name	Chain Element
HD28	CH1_24
HD21	CH1_25
NA#	CH1_26
HD25	CH1_27
BRDY#	CH1_28
HD23	CH1_29
HD35	CH1_30
HD29	CH1_31
HD30	CH1_32
BE7#	CH1_33
HD32	CH1_34
BE3#	CH1_35
BE4#	CH1_36
HD39	CH1_37
HD45	CH1_38
HD42	CH1_39
HD38	CH1_40
HD40	CH1_41
HD48	CH1_42
KEN#	CH1_43
HD46	CH1_44
HD43	CH1_45
HD51	CH1_46
HD58	CH1_47

Table 27. Chain #1 (GNT#1)

Pin Name	Chain Element
HD56	CH1_48
HD50	CH1_49
M/IO#	CH1_50
HD59	CH1_51
HD63	CH1_52
PHLD#	CH1_53
AD31	CH1_54
LOCK#	CH1_55
AD28	CH1_56
FRAME#	CH1_57
AD29	CH1_58
PHLDA#	CH1_59
IRDY#	CH1_60
AD26	CH1_61
AD23	CH1_62
AD17	CH1_63
DEVSEL#	CH1_64
AD18	CH1_65
REQ1#	CH1_66
AD15	CH1_67
PCLKIN	CH1_68
AD11	CH1_69
AD10	CH1_70
AD9	CH1_71

Table 28. Chain #2 (GNT#2)

Pin Name	Chain Element
A28	CH2_00
A29	CH2_01
A3	CH2_02
A30	CH2_03
A4	CH2_04
COE#	CH2_05
BWE#	CH2_06
CCS#	CH2_07
MA5	CH2_08
MA10	CH2_09
KRQAK/ CS4_64#	CH2_10
MA7	CH2_11
MA11	CH2_12
MA6	CH2_13
MA9	CH2_14
MWEB#	CH2_15
RAS0#	CH2_16
RAS4#	CH2_17
RAS2#	CH2_18
CAS7#	CH2_19
CAS5#	CH2_20
CAS6#	CH2_21
CKE/MAA0	CH2_22

Table 28. Chain #2 (GNT#2)

Pin Name	Chain Element
CAS4#	CH2_23
SUSCLK	CH2_24
SRASA	CH2_25
MD11	CH2_26
MD53	CH2_27
SCASB#	CH2_28
MD22	CH2_29
MD6	CH2_30
MD34	CH2_31
MD39	CH2_32
MD7	CH2_33
MD54	CH2_34
HCLKIN	CH2_35
MD55	CH2_36
MD5	CH2_37
MD17	CH2_38
MD2	CH2_39
MD50	CH2_40
MD1	CH2_41
MD0	CH2_42
MD18	CH2_43
MD16	CH2_44
MD19	CH2_45
MD40	CH2_46

Table 28. Chain #2 (GNT#2)

Pin Name	Chain Element
MD32	CH2_47
MD25	CH2_48
MD26	CH2_49
MD42	CH2_50
MD48	CH2_51
MD49	CH2_52
MD59	CH2_53
MD43	CH2_54
MD30	CH2_55
MD27	CH2_56
MD28	CH2_57
MD12	CH2_58
MD60	CH2_59
CLKRUN#	CH2_60
AD0	CH2_61
AD2	CH2_62
STOP#	CH2_63
AD4	CH2_64
AD3	CH2_65
AD5	CH2_66
AD7	CH2_67
AD6	CH2_68
REQ2#	CH2_69

Table 29. Chain #3 (GNT#3)

Pin Name	Chain Element
A22	CH3_00
CADV#	CH3_01
A6	CH3_02
TWE#	CH3_03
GWE#	CH3_04
CADS#	CH3_05
TIO1	CH3_06
TIO3	CH3_07
TIO7	CH3_08
TIO6	CH3_09
TIO2	CH3_10
TIO5	CH3_11
TIO4	CH3_12
TIO0	CH3_13
MA0	CH3_14
MA2	CH3_15
MA4	CH3_16
CKEB/ MAA1	CH3_17
MA1	CH3_18
MA3	CH3_19
MA8	CH3_20
CAS1#	CH3_21
CAS3#	CH3_22

Table 29. Chain #3 (GNT#3)

Pin Name	Chain Element
CAS0#	CH3_23
CAS2#	CH3_24
MWEB#	CH3_25
RAS1#	CH3_26
RAS3#	CH3_27
RAS5#	CH3_28
SCASA	CH3_29
MD21	CH3_30
SRASB#	CH3_31
MD51	CH3_32
MD20	CH3_33
MD37	CH3_34
MD38	CH3_35
MD3	CH3_36
MD52	CH3_37
MD23	CH3_38
MD4	CH3_39
MD36	CH3_40
MD56	CH3_41
MD8	CH3_42
MD9	CH3_43
MD33	CH3_44
MD24	CH3_45

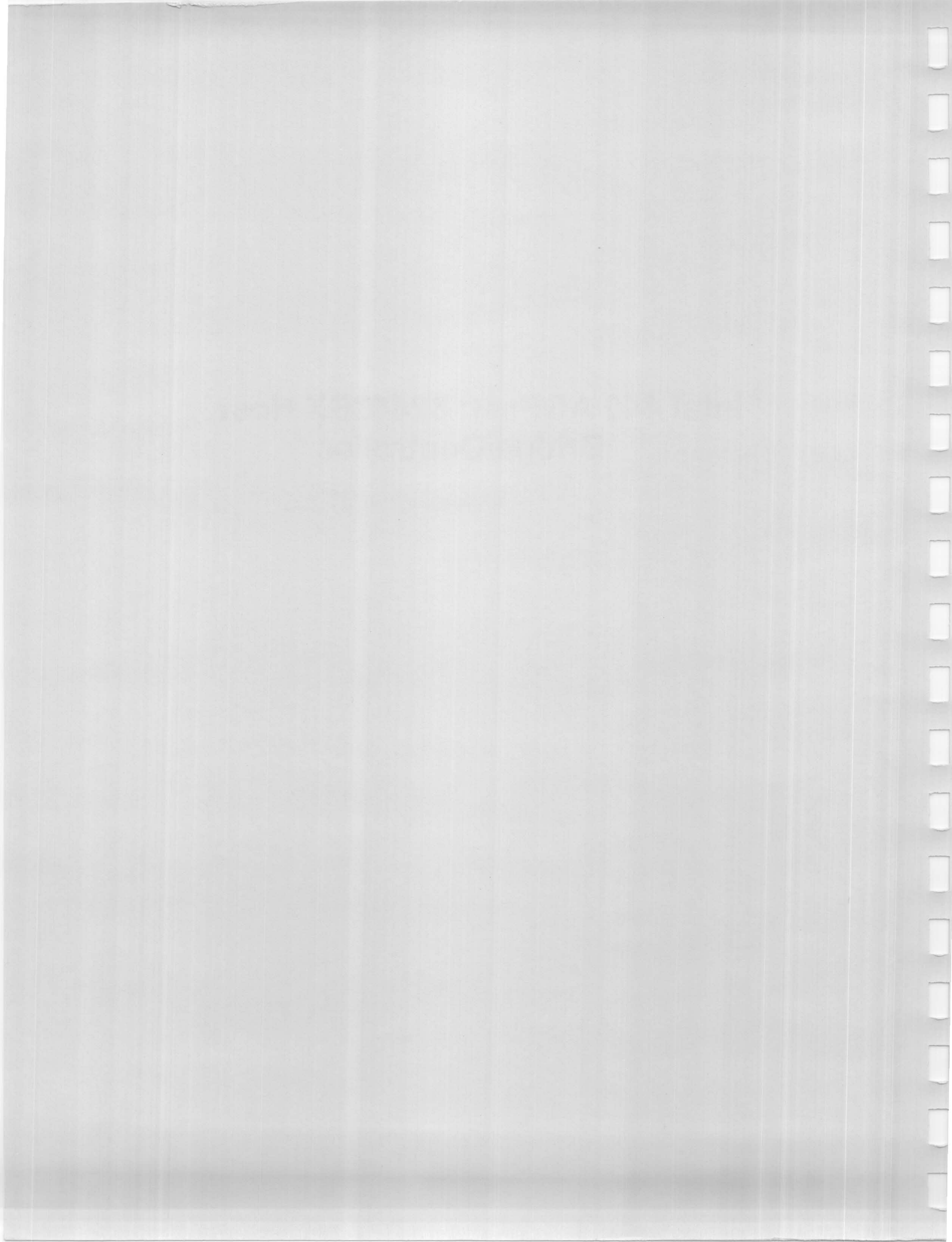
Table 29. Chain #3 (GNT#3)

Pin Name	Chain Element
MD41	CH3_46
MD57	CH3_47
MD35	CH3_48
MD58	CH3_49
MD10	CH3_50
MD44	CH3_51
MD62	CH3_52
MD15	CH3_53
MD46	CH3_54
MD45	CH3_55
MD61	CH3_56
MD63	CH3_57
MD29	CH3_58
MD13	CH3_59
MD47	CH3_60
REQ3#	CH3_61
MD14	CH3_62
PAR	CH3_63
MD31	CH3_64
AD1	CH3_65
C/BE0#	CH3_66
AD8	CH3_67





**Intel 440 AGPset: 82443BX Host  
Bridge/Controller**







# Intel® 440BX AGPset: 82443BX Host Bridge/Controller

## Datasheet

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April 1998

Order Number: 290633-001



# Intel® 82443BX Host Bridge/Controller Intel® 440BX AGPset:

Datasheet

April 1998

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## Intel 82443BX Features

- Processor/host bus support
  - Optimized for Pentium® II processor at 100 MHz system bus frequency; Support for 66 MHz
  - Supports full symmetric Multiprocessor (SMP) Protocol for up to two processors; I/O APIC related buffer management support (WSC# signal)
  - In-order transaction and dynamic deferred transaction support
  - Desktop optimized GTL+ bus driver technology (gated GTL+ receivers for reduced power)
- Integrated DRAM controller
  - 8 to 512 Mbytes or 1GB (with registered DIMMs)
  - Supports up to 4 double-sided DIMMs (8 rows memory)
  - 64-bit data interface with ECC support (SDRAM only)
  - Unbuffered and Registered SDRAM (Synchronous) DRAM Support (x-1-1-1 access @ 66 MHz, x-1-1-1 access @ 100 MHz)
  - Enhanced SDRAM Open Page Architecture Support for 16- and 64-Mbit DRAM devices with 2k, 4k and 8k page sizes
- PCI bus interface
  - PCI Rev. 2.1, 3.3V and 5V, 33MHz interface compliant
  - PCI Parity Generation Support
  - Data streaming support from PCI to DRAM
  - Delayed Transaction support for PCI-DRAM Reads
  - Supports concurrent CPU, AGP and PCI transactions to main memory
- AGP interface
  - Supports single AGP compliant device (AGP-66/133 3.3V device)
  - AGP Specification Rev 1.0 compliant
  - AGP-data/transaction flow optimized arbitration mechanism
  - AGP side-band interface for efficient request pipelining without interfering with the data streams
  - AGP-specific data buffering
  - Supports concurrent CPU, AGP and PCI transactions to main memory
  - AGP high-priority transactions ("expedite") support
- Power Management Functions
  - Stop Clock Grant and Halt special cycle translation (host to PCI Bus)
  - Mobile and "Deep Green" Desktop support for system suspend/resume (i.e., DRAM and power-on suspend)
  - Dynamic power down of idle DRAM rows
  - SDRAM self-refresh power down support in suspend mode
  - Independent, internal dynamic clock gating reduces average power dissipation
  - Static STOP CLOCK support
  - Power-on Suspend mode
  - Suspend to DRAM
  - ACPI compliant power management
- Packaging/Voltage
  - 492 Pin BGA
  - 3.3V core and mixed 3.3V and GTL I/O
- Supporting I/O Bridge
  - System Management Bus (SMB) with support for DIMM Serial Presence Detect (SPD)
  - PCI-ISA Bridge (PIIX4E)
  - Power Management Support
  - 3.3V core and mixed 5V, 3.3V I/O and interface to the 2.5V CPU signals via open-drain output buffers

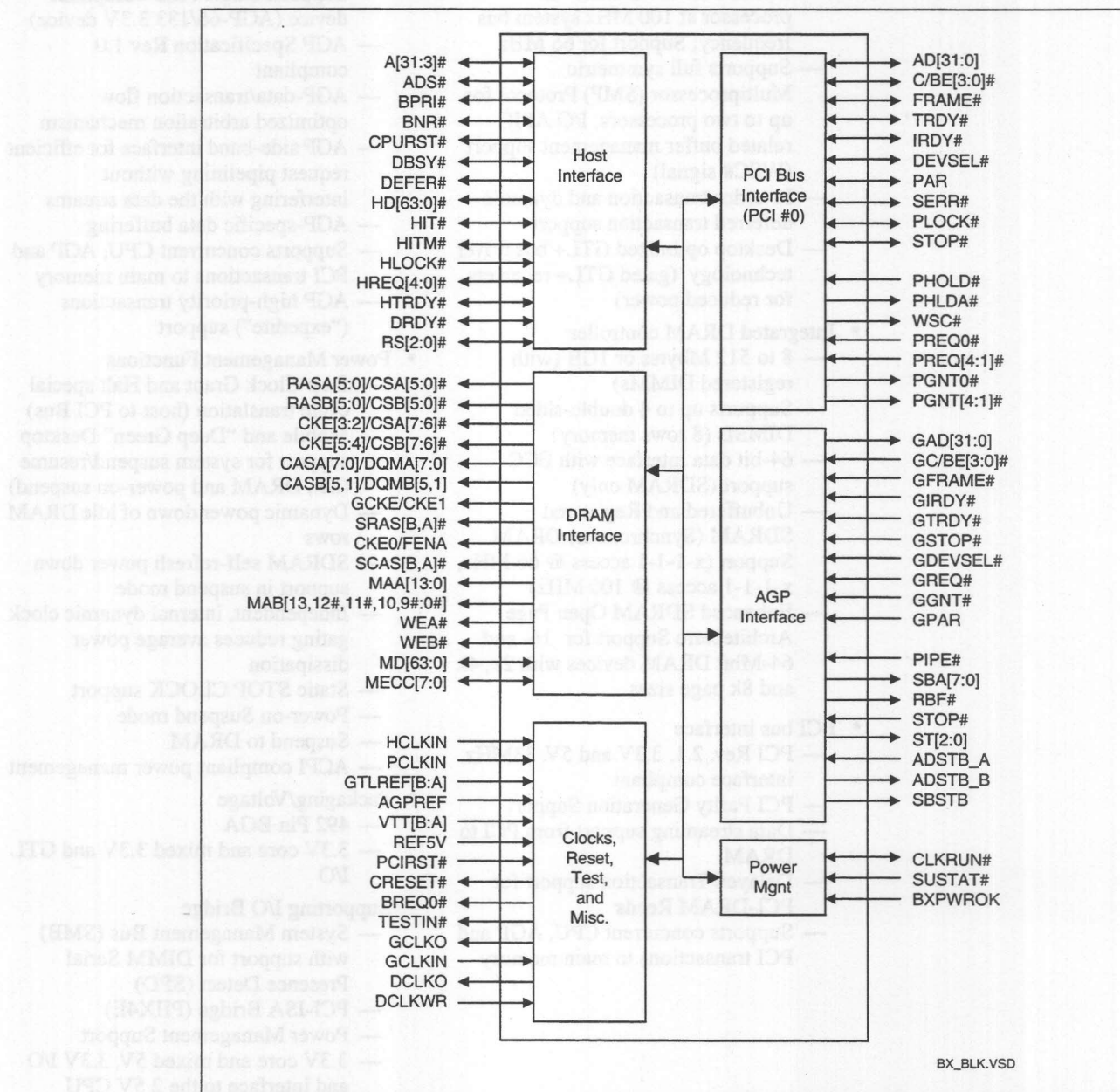
The Intel® 440BX AGPset is intended for the Pentium® II processor platform and emerging 3D graphics/multimedia applications. The 82443BX Host Bridge provides a Host-to-PCI bridge, optimized DRAM controller and data path, and an Accelerated Graphic Port (AGP) interface. AGP is a high performance, component level interconnect targeted at 3D graphics applications and is based on a set of performance enhancements to PCI.

The Intel 82443BX may contain design defects or errors known as errata which may cause the products to deviate from published specifications. Current characterized errata are available on request.



The I/O subsystem portion of the Intel® 440BX AGPset platform is based on the 82371EB (PIIX4E), a highly integrated version of the Intel's PCI-ISA bridge family. The Intel® 440BX AGPset is ideal for the Mobile AGPset Pentium II processor platforms; providing full support for all system suspend modes and segmented power planes.

### Intel 82443BX Simplified Block Diagram





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# Architectural Overview

1

The Intel® 440BX AGPset includes the 82443BX Host Bridge and the 82371EB PIIX4E for the I/O subsystem. The 82443BX functions and capabilities include:

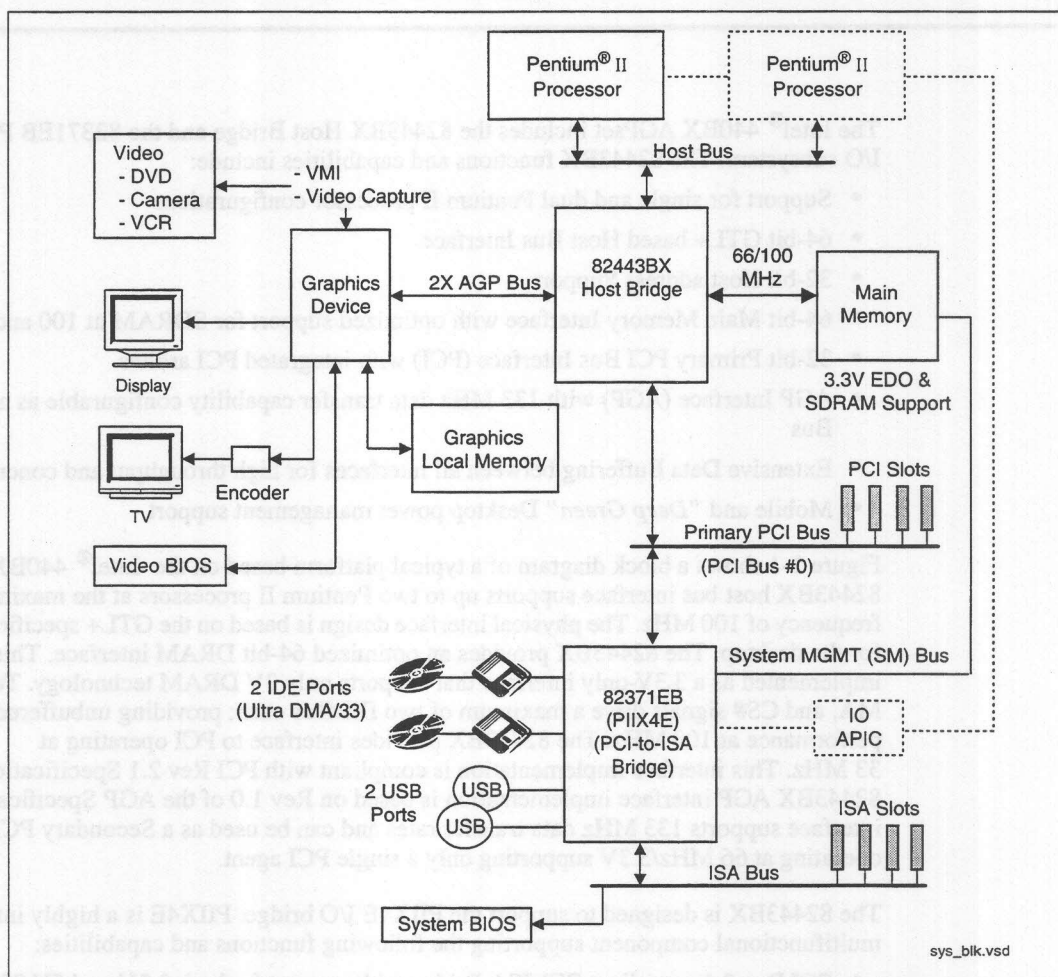
- Support for single and dual Pentium II processor configurations
- 64-bit GTL+ based Host Bus Interface
- 32-bit Host address Support
- 64-bit Main Memory Interface with optimized support for SDRAM at 100 and 66/60 MHz
- 32-bit Primary PCI Bus Interface (PCI) with integrated PCI arbiter
- AGP Interface (AGP) with 133 MHz data transfer capability configurable as a Secondary PCI Bus
- Extensive Data Buffering between all interfaces for high throughput and concurrent operations
- Mobile and "Deep Green" Desktop power management support

Figure 1-1 shows a block diagram of a typical platform based on the Intel® 440BX AGPset. The 82443BX host bus interface supports up to two Pentium II processors at the maximum bus frequency of 100 MHz. The physical interface design is based on the GTL+ specification optimized for the desktop. The 82443BX provides an optimized 64-bit DRAM interface. This interface is implemented as a 3.3V-only interface that supports only 3V DRAM technology. Two copies of the MA, and CS# signals drive a maximum of two DIMMs each; providing unbuffered high performance at 100 MHz. The 82443BX provides interface to PCI operating at 33 MHz. This interface implementation is compliant with PCI Rev 2.1 Specification. The 82443BX AGP interface implementation is based on Rev 1.0 of the AGP Specification. The AGP interface supports 133 MHz data transfer rates and can be used as a Secondary PCI interface operating at 66 MHz/3.3V supporting only a single PCI agent.

The 82443BX is designed to support the PIIX4E I/O bridge. PIIX4E is a highly integrated multifunctional component supporting the following functions and capabilities:

- PCI Rev 2.1 compliant PCI-ISA Bridge with support for both 3.3V and 5V 33 MHz PCI operations
- Deep Green Desktop Power Management Support
- Mobile Power Management Support
- Enhanced DMA controller and Interrupt Controller and Timer functions
- Integrated IDE controller with Ultra DMA/33 support
- USB host interface with support for 2 USB ports
- System Management Bus (SMB) with support for DIMM Serial PD
- Support for an external I/O APIC component

Figure 1-1. Intel® 440BX AGPset System Block Diagram



### Host Interface

The Pentium II processor supports a second level cache via a back-side bus (BSB) interface. All control for the L2 cache is handled by the processor. The 82443BX provides bus control signals and address paths for transfers between the processors front-side bus (host bus), PCI bus, AGP and main memory. The 82443BX supports a 4-deep in-order queue (i.e., supports pipelining of up to 4 outstanding transaction requests on the host bus). Due to the system concurrency requirements, along with support for pipelining of address requests from the host bus, the 82443BX supports request queuing for all three interfaces (Host, AGP and PCI).

Host-initiated I/O cycles are decoded to PCI, AGP or PCI configuration space. Host-initiated memory cycles are decoded to PCI, AGP (prefetchable or non-prefetchable memory space) or DRAM (including AGP aperture memory). For memory cycles (host, PCI or AGP initiated) that target the AGP aperture space in DRAM, the 82443BX translates the address using the AGP address translation table. Other host cycles forwarded to AGP are defined by the AGP address map.

PCI and AGP initiated cycles that target the AGP graphics aperture are also translated using the AGP aperture translation table. AGP-initiated cycles that target the AGP graphics aperture mapped in main memory do not require a snoop cycle on the host bus, since the coherency of data for that particular memory range will be maintained by the software.



### DRAM Interface

The 82443BX integrates a DRAM controller that supports a 64-bit main memory interface. The DRAM controller supports the following features:

- *DRAM type:* Extended Data Out (EDO) (mobile only) or Synchronous (SDRAM) DRAM controller optimized for dual/quad-bank SDRAM organization on a row by row basis
- *Memory Size:* 8 MB to 512 MB (1GB with Registered DIMMs) with eight memory rows
- *Addressing Type:* Symmetrical and Asymmetrical addressing
- *Memory Modules supported:* Single and double density 3.3V DIMMs
- *DRAM device technology:* 16 Mbit and 64 Mbit
- *DRAM Speeds:* 60 ns for EDO and 100/66 MHz for synchronous memory (SDRAM).

The Intel® 440BX AGPset also provides DIMM plug-and-play support via Serial Presence Detect (SPD) mechanism using the SMBus interface. The 82443BX provides optional data integrity features including ECC in the memory array. During reads from DRAM, the 82443BX provides error checking and correction of the data. The 82443BX supports multiple-bit error detection and single-bit error correction when ECC mode is enabled and single/multi-bit error detection when correction is disabled. During writes to the DRAM, the 82443BX generates ECC for the data on a QWord basis. Partial QWord writes require a read-modify-write cycle when ECC is enabled.

### AGP Interface

The 82443BX AGP implementation is compatible with the following:

- The Accelerated Graphics Port Specification, Rev 1.0
- Accelerated Graphics Port Memory Performance Specification, Rev 1.0 (4/12/96)

The 82443BX supports only a synchronous AGP interface coupling to the 82443BX core frequency. The AGP interface can reach a theoretical ~500 MByte/sec transfer rate (i.e., using 133 MHz AGP compliant devices).

### PCI Interface

The 82443BX PCI interface is 3.3V (5V tolerant), 33 MHz Rev. 2.1 compliant and supports up to five external PCI bus masters in addition to the I/O bridge (PIIX4/PIIX4E). The PCI-to-DRAM interface can reach over 100 MByte/sec transfer rate for streaming reads and over 120 MBytes/sec for streaming writes.

### System Clocking

The 82443BX operates the host interface at 66 or 100 MHz, the SDRAM/core at 66 or 100 MHz, PCI at 33 MHz and AGP at 66/133 MHz.

### I/O APIC

I/O APIC is used to support dual processors as well as enhanced interrupt processing in the single processor environment. The 82443BX supports an external status output signal that can be used to control synchronization of interrupts in configurations that use PIIX4E with stand-alone I/O APIC component.



# Signal Description

## 2

This chapter provides a detailed description of 443BX signals. The signals are arranged in functional groups according to their associated interface.

The “#” symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “#” is not present after the signal name the signal is asserted when at the high voltage level.

The following notations are used to describe the signal type:

- I** Input pin
- O** Output pin
- OD** Open Drain Output pin. This pin requires a pullup to the VCC of the processor core
- I/OD** Input / Open Drain Output pin. This pin requires a pullup to the VCC of the processor core
- I/O** Bi-directional Input/Output pin

The signal description also includes the type of buffer used for the particular signal:

- GTL+** Open Drain GTL+ interface signal. Refer to the GTL+ I/O Specification for complete details
- PCI** PCI bus interface signals. These signals are compliant with the PCI 3.3V and 5.0V Signaling Environment DC and AC Specifications
- AGP** AGP interface signals. These signals are compatible with AGP 3.3V Signaling Environment DC and AC Specifications
- CMOS** The CMOS buffers are Low Voltage TTL compatible signals. These are 3.3V only.

## 2.1 Host Interface Signals

Table 2-1. Host Interface Signals (Sheet 1 of 2)

Name	Type	Description
CPURST#	O GTL+	<b>CPU Reset.</b> The CPURST# pin is an output from the 82443BX. The 82443BX generates this signal based on the PCIRST# input (from PIIX4E) and also the SUSTAT# pin in mobile mode. The CPURST# allows the CPUs to begin execution in a known state.
A[31:3]#	I/O GTL+	<b>Address Bus:</b> A[31:3]# connect to the CPU address bus. During CPU cycles, the A[31:3]# are inputs.
HD[63:0]#	I/O GTL+	<b>Host Data:</b> These signals are connected to the CPU data bus. Note that the data signals are inverted on the CPU bus.



Table 2-1. Host Interface Signals (Sheet 2 of 2)

Name	Type	Description																		
ADS#	I/O GTL+	<b>Address Strobe:</b> The CPU bus owner asserts ADS# to indicate the first of two cycles of a request phase.																		
BNR#	I/O GTL+	<b>Block Next Request:</b> Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.																		
BPRI#	O GTL+	<b>Priority Agent Bus Request:</b> The 82443BX is the only Priority Agent on the CPU bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.																		
BREQ0#	O GTL+	<b>Symmetric Agent Bus Request:</b> Asserted by the 82443BX when CPURST# is asserted to configure the symmetric bus agents. BREQ0# is negated 2 host clocks after CPURST# is negated.																		
DBSY#	I/O GTL+	<b>Data Bus Busy:</b> Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.																		
DEFER#	O GTL+	<b>Defer:</b> The 82443BX generates a deferred response as defined by the rules of the 82443BX's dynamic defer policy. The 82443BX also uses the DEFER# signal to indicate a CPU retry response.																		
DRDY#	I/O GTL+	<b>Data Ready:</b> Asserted for each cycle that data is transferred.																		
HIT#	I/O GTL+	<b>Hit:</b> Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.																		
HITM#	I/O GTL+	<b>Hit Modified:</b> Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also driven in conjunction with HIT# to extend the snoop window.																		
HLOCK#	I GTL+	<b>Host Lock:</b> All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no PCI or AGP snoopable access to DRAM is allowed when HLOCK# is asserted by the CPU.																		
HREQ[4:0]#	I/O GTL+	<b>Request Command:</b> Asserted during both clocks of request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type. The transactions supported by the 82443BX Host Bridge are defined in the Host Interface section of this document.																		
HTRDY#	I/O GTL+	<b>Host Target Ready:</b> Indicates that the target of the CPU transaction is able to enter the data transfer phase.																		
RS[2:0]#	I/O GTL+	<b>Response Signals:</b> Indicates type of response according to the following table: <table><tr><th>RS[2:0]</th><th>Response type</th></tr><tr><td>000</td><td>Idle state</td></tr><tr><td>001</td><td>Retry response</td></tr><tr><td>010</td><td>Deferred response</td></tr><tr><td>011</td><td>Reserved (not driven by 82443BX)</td></tr><tr><td>100</td><td>Hard Failure (not driven by 82443BX)</td></tr><tr><td>101</td><td>No data response</td></tr><tr><td>110</td><td>Implicit Writeback</td></tr><tr><td>111</td><td>Normal data response</td></tr></table>	RS[2:0]	Response type	000	Idle state	001	Retry response	010	Deferred response	011	Reserved (not driven by 82443BX)	100	Hard Failure (not driven by 82443BX)	101	No data response	110	Implicit Writeback	111	Normal data response
RS[2:0]	Response type																			
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101	No data response																			
110	Implicit Writeback																			
111	Normal data response																			

**NOTE:**

1. All of the signals in the host interface are described in the CPU External Bus Specification. The preceding table highlights 82443BX specific uses of these signals.

Table 2-2 lists the CPU bus interface signals which are NOT supported by the Intel® 440BX AGPset.

**Table 2-2. Host Signals Not supported by the 82443BX**

Signal	Function	Not Supported By 82443BX
A[35:32]#	Address	Extended addressing (over 4 GB)
AERR#	Address Parity Error	Parity protection on address bus
AP[1:0]#	Address Parity	Parity protection on address bus
BINIT#	Bus Initialization	Checking for bus protocol violation and protocol recovery mechanism
DEP[7:0]#	Data Bus ECC/Parity	Enhanced data bus integrity
IERR#	Internal Error	Direct internal error observation via IERR# pin
INIT#	Soft Reset	Implemented by PIIX4E, BIST supported by external logic.
BERR#	Bus Error	Unrecoverable error without a bus protocol violation
RP#	Request Parity	Parity protection on ADS# and PREQ[4:0]#
RSP#	Response Parity Signal	Parity protection on RS[2:0]#

## 2.2 DRAM Interface

**Table 2-3. DRAM Interface Signals (Sheet 1 of 2)**

Name	Type	Description
RASA[5:0]# /CSA[5:0]#	O CMOS	<p><b>Row Address Strobe (EDO):</b> These signals are used to latch the row address on the MAxx lines into the DRAMs. Each signal is used to select one DRAM row. These signals drive the DRAM array directly without any external buffers.</p> <p><b>Chip Select (SDRAM):</b> For the memory row configured with SDRAM these pins perform the function of selecting the particular SDRAM components during the active state.</p> <p>Note that there are 2 copies of RAS# per physical memory row to improve the loading.</p>
RASB[5:0]# /CSB[5:0]#		
CKE[3:2] /CSA[7:6]#	O CMOS	<p><b>Clock Enable:</b> In mobile mode, SDRAM Clock Enable is used to signal a self-refresh or power-down command to an SDRAM array when entering system suspend. CKE is also used to dynamically power down inactive SDRAM rows. This CKE function is not supported with Registered DIMMs.</p> <p><b>Chip Select (SDRAM):</b> These pins perform the function of selecting the particular SDRAM components during the active state.</p> <p>Note that there are 2 copies of CS# per physical memory row to reduce the loading.</p>
CKE[5:4] /CSB[7:6]#		
CASA[7:0]# /DQMA[7:0]	O CMOS	<p><b>Column Address Strobe A-side (EDO):</b> The CASA[7:0]# signals are used to latch the column address on the MA[13:0] lines into the DRAMs of the A half of the memory array. These are active low signals that drive the DRAM array directly without external buffering.</p> <p><b>Input/Output Data Mask A-side (SDRAM):</b> These pins control A half of the memory array and act as synchronized output enables during read cycles and as a byte enables during write cycles.</p>
CASB[1,5]# /DQMB[1,5]	O CMOS	<p><b>Column Address Strobe B-side (EDO) / Input/Output Data Mask B-side (SDRAM):</b> The same function as a corresponding signals for A side. These signals are used to reduce the loading in an ECC configuration</p>

Table 2-3. DRAM Interface Signals (Sheet 2 of 2)

Name	Type	Description
GCKE/CKE1	O CMOS	<b>Global CKE (SDRAM):</b> Global CKE is used in a 4 DIMM configuration requiring power down mode for the SDRAM. External logic must be used to implement this function. <b>SDRAM Clock Enable (CKE1):</b> In mobile mode, SDRAM Clock Enable is used to signal a self-refresh or power-down command to an SDRAM array when entering system suspend. CKE is also used to dynamically power down inactive SDRAM rows. The combination of SDRAMPWR (SDRAM register) and MMCONFIG (DRAMC register) determine the functioning of the CKE signals. Refer to the DRAMC register (Section 3.3.15, "DRAMC—DRAM Control Register (Device 0)" on page 3-19) for more details.
SRAS[B,A]#	O CMOS	<b>SDRAM Row Address Strobe (SDRAM):</b> The SRAS[B,A]# signals are multiple copies of the same logical SRASx signal (for loading purposes) used to generate SDRAM command encoded on SRASx/SCASx/WE signals.
CKE0/FENA	O CMOS	<b>SDRAM Clock Enable 0 (CKE0):</b> In mobile mode, CKE0 SDRAM Clock Enable is used to signal a self-refresh or power-down command to an SDRAM array when entering system suspend. CKE is also used to dynamically power down inactive SDRAM rows. <b>FET Enable (FENA):</b> In a 4 DIMM configuration, FENA is used to select the proper MD path through the FET switches (refer to Section 4.3, "DRAM Interface" on page 4-14 for more details).
SCAS[B,A]#	O CMOS	<b>SDRAM Column Address Strobe (SDRAM):</b> The SCAS[B,A]# signals are multiple copies of the same logical SCASx signal (for loading purposes) used to generate SDRAM command encoded on SRASx/SCASx/WE signals.
MAA[13:0] MAB[12:11]# MAB[13,10] MAB[9:0]#	O CMOS	<b>Memory Address(EDO/SDRAM):</b> MAA[13:0] and MAB[13:0]# are used to provide the multiplexed row and column address to DRAM. There are two sets of MA signals which drive a max. of 2 DIMMs each. MAA[12:11,9:0] are inverted copies of MAB[12:11,9:0]#. MAA[13,10] and MAB[13,10] are identical copies. Each MAA/MAB[13:0] line has a programmable buffer strength to optimize for different signal loading conditions.
WEA# WEB#	O CMOS	<b>Write Enable Signal (EDO/SDRAM):</b> WE# is asserted during writes to DRAM. The WE# lines have a programmable buffer strength to optimize for different signal loading conditions.
MD [63:0]	I/O CMOS	<b>Memory Data (EDO/SDRAM):</b> These signals are used to interface to the DRAM data bus.
MECC[7:0]	I/O CMOS	<b>Memory ECC Data (EDO/SDRAM):</b> These signals carry Memory ECC data during access to DRAM.



## 2.3 PCI Interface (Primary)

Table 2-4. Primary PCI Interface Signals (Sheet 1 of 2)

Name	Type	Description
AD[31:0]	I/O PCI	<b>PCI Address/Data:</b> These signals are connected to the PCI address/data bus. Address is driven by the 82443BX with FRAME# assertion, data is driven or received in the following clocks. When the 82443BX acts as a target on the PCI Bus, the AD[31:0] signals are inputs and contain the address during the first clock of FRAME# assertion and input data (writes) or output data (reads) on subsequent clocks.
DEVSEL#	I/O PCI	<b>Device Select:</b> Device select, when asserted, indicates that a PCI target device has decoded its address as the target of the current access. The 82443BX asserts DEVSEL# based on the DRAM address range or <i>AGP address range</i> being accessed by a PCI initiator. As an input it indicates whether any device on the bus has been selected.
FRAME#	I/O PCI	<b>Frame:</b> FRAME# is an output when the 82443BX acts as an initiator on the PCI Bus. FRAME# is asserted by the 82443BX to indicate the beginning and duration of an access. The 82443BX asserts FRAME# to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is negated, the transaction is in the final data phase. FRAME# is an input when the 82443BX acts as a PCI target. As a PCI target, the 82443BX latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which it samples FRAME# active.
IRDY#	I/O PCI	<b>Initiator Ready:</b> IRDY# is an output when 82443BX acts as a PCI initiator and an input when the 82443BX acts as a PCI target. The assertion of IRDY# indicates the current PCI Bus initiator's ability to complete the current data phase of the transaction.
C/BE[3:0]#	I/O PCI	<b>Command/Byte Enable:</b> PCI Bus Command and Byte Enable signals are multiplexed on the same pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as byte enables. The byte enables determine which byte lanes carry meaningful data. PCI Bus command encoding and types are listed below.  <b>C/BE[3:0]#    Command Type</b> 0000    Interrupt Acknowledge 0001    Special Cycle 0010    I/O Read 0011    I/O Write 0100    Reserved 0101    Reserved 0110    Memory Read 0111    Memory Write 1000    Reserved 1001    Reserved 1010    Configuration Read 1011    Configuration Write 1100    Memory Read Multiple 1101    Reserved (Dual Address Cycle) 1110    Memory Read Line 1111    Memory Write and Invalidate
PAR	I/O PCI	<b>Parity:</b> PAR is driven by the 82443BX when it acts as a PCI initiator during address and data phases for a write cycle, and during the address phase for a read cycle. PAR is driven by the 82443BX when it acts as a PCI target during each data phase of a PCI memory read cycle. Even parity is generated across AD[31:0] and C/BE[3:0]#.
PLOCK#	I/O PCI	<b>Lock:</b> PLOCK# indicates an exclusive bus operation and may require multiple transactions to complete. When PLOCK# is asserted, non-exclusive transactions may proceed. The 82443BX supports lock for CPU initiated cycles only. PCI initiated locked cycles are not supported.
TRDY#	I/O PCI	<b>Target Ready:</b> TRDY# is an input when the 82443BX acts as a PCI initiator and an output when the 82443BX acts as a PCI target. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction.

Table 2-4. Primary PCI Interface Signals (Sheet 2 of 2)

Name	Type	Description
SERR#	I/O PCI	<p><b>System Error:</b> The 82443BX asserts this signal to indicate an error condition. The SERR# assertion by the 82443BX is enabled globally via SERRE bit of the PCICMD register. SERR# is asserted under the following conditions:</p> <p>In an ECC configuration, the 82443BX asserts SERR#, for single bit (correctable) ECC errors or multiple bit (non-correctable) ECC errors if SERR# signaling is enabled via the ERRCMD control register. Any ECC errors received during initialization should be ignored.</p> <ul style="list-style-type: none"> <li>The 82443BX asserts SERR# for one clock when it detects a target abort during 82443BX initiated PCI cycle.</li> <li>The 82443BX can also assert SERR# when a PCI parity error occurs during the address or data phase.</li> <li>The 82443BX can assert SERR# when it detects a PCI address or data parity error on AGP.</li> <li>The 82443BX can assert SERR# upon detection of access to an invalid entry in the Graphics Aperture Translation Table.</li> <li>The 82443BX can assert SERR# upon detecting an invalid AGP master access outside of AGP aperture and outside of main DRAM range (i.e. in the 640k - 1M range or above TOM).</li> <li>The 82443BX can assert SERR# upon detecting an invalid AGP master access outside of AGP aperture.</li> <li>The 82443BX asserts SERR# for one clock when it detects a target abort during 82443BX initiated AGP cycle.</li> </ul>
STOP#	I/O PCI	<p><b>Stop:</b> STOP# is an input when the 82443BX acts as a PCI initiator and an output when the 82443BX acts as a PCI target. STOP# is used for disconnect, retry, and abort sequences on the PCI Bus.</p>

**NOTE:**

1. All PCI interface signals conform to the PCI Rev 2.1 specification.

## 2.4 Primary PCI Sideband Interface

Table 2-5. Primary PCI Sideband Interface Signals

Name	Type	Description
PHOLD#	I PCI	<b>PCI Hold:</b> This signal comes from the PIIX4E. It is the PIIX4E request for PCI bus ownership. The 82443BX will flush and disable the CPU-to-PCI write buffers before granting the PIIX4E the PCI bus via PHLDA#. This prevents bus deadlock between PCI and ISA.
PHLDA#	O PCI	<b>PCI Hold Acknowledge:</b> This signal is driven by the 82443BX to grant PCI bus ownership to the PIIX4E after CPU-PCI post buffers have been flushed and disabled.
WSC#	O CMOS	<b>Write Snoop Complete.</b> This signal is asserted active to indicate that all that the snoop activity on the CPU bus on the behalf of the last PCI-DRAM write transaction is complete and that is safe to send the APIC interrupt message.
PREQ[4:0]#	I PCI	<b>PCI Bus Request:</b> PREQ[4:0]# are the PCI bus request signals used as inputs by the internal PCI arbiter.
PGNT[4:0]#	O PCI	<b>PCI Grant:</b> PGNT[4:0]# are the PCI bus grant output signals generated by the internal PCI arbiter.

## 2.5 AGP Interface Signals

There are 17 new signals added to the normal PCI group of signals that together constitute the AGP interface. The sections below describe their operation and use, and are organized in five groups:

- AGP Addressing Signals
- AGP Flow Control Signals
- AGP Status Signals
- AGP Clocking Signals - Strobes
- PCI Signals

Table 2-6. AGP Interface Signals (Sheet 1 of 2)

Name	Type	Description
<b>AGP Sideband Addressing Signals<sup>1</sup></b>		
PIPE#	I AGP	<b>Pipelined Read:</b> This signal is asserted by the current master to indicate a full width address is to be queued by the target. The master queues one request each rising clock edge while PIPE# is asserted. When PIPE# is deasserted no new requests are queued across the AD bus. PIPE# is a sustained tri-state signal from <i>masters</i> (graphics controller) and is an input to the 82443BX. Note that initial AGP designs may not use PIPE#.
SBA[7:0]	I AGP	<b>Sideband Address:</b> This bus provides an additional bus to pass address and command to the 82443BX from the AGP master. Note that, when sideband addressing is disabled, these signals are isolated (no external/internal pull-ups are required).
<b>AGP Flow Control Signals</b>		
RBF#	I AGP	<b>Read Buffer Full.</b> This signal indicates if the master is ready to accept previously requested low priority read data. When RBF# is asserted the 82443BX is not allowed to return low priority read data to the AGP master on the first block. RBF# is only sampled at the beginning of a cycle.  If the AGP master is always ready to accept return read data then it is not required to implement this signal.
<b>AGP Status Signals</b>		
ST[2:0]	O AGP	<b>Status Bus:</b> This bus provides information from the arbiter to a AGP Master on what it may do. ST[2:0] only have meaning to the master when its GGNT# is asserted. When GGNT# is deasserted these signals have no meaning and must be ignored. 000 Indicates that previously requested low priority read data is being returned to the master. 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously queued write command. 011 Indicates that the master is to provide high priority write data for a previously queued write command. 100 Reserved 101 Reserved 110 Reserved 111 Indicates that the master has been given permission to start a bus transaction. The master may queue AGP requests by asserting PIPE# or start a PCI transaction by asserting FRAME#. ST[2:0] are always an output from the 82443BX and an input to the master.



Table 2-6. AGP Interface Signals (Sheet 2 of 2)

Name	Type	Description
<b>AGP Clocking Signals - Strobes</b>		
ADSTB_A	I/O AGP	<b>AD Bus Strobe A:</b> This signal provides timing for double clocked data on the AD bus. The agent that is providing data drives this signal. This signal requires an 8.2K ohm external pull-up resistor.
ADSTB_B	I/O AGP	<b>AD Bus Strobe B:</b> This signal is an additional copy of the AD_STBA signal. This signal requires an 8.2K ohm external pull-up resistor.
SBSTB	I AGP	<b>Sideband Strobe:</b> This signal provides timing for a side-band bus. This signal requires an 8.2K ohm external pull-up resistor.
<b>AGP FRAME# Protocol Signals (similar to PCI)<sup>2</sup></b>		
GFRAME#	I/O AGP	<b>Graphics Frame:</b> Same as PCI. Not used by AGP. GFRAME# remains deasserted by its own pull up resistor.
GIRDY#	I/O AGP	<b>Graphics Initiator Ready:</b> New meaning. GIRDY# indicates the AGP compliant master is ready to provide <i>all</i> write data for the current transaction. Once IRDY# is asserted for a write operation, the master is not allowed to insert wait states. The assertion of IRDY# for reads indicates that the master is ready to transfer to a subsequent block (32 bytes) of read data. The master is <i>never</i> allowed to insert wait states during the initial data transfer (32 bytes) of a read transaction. However, it may insert wait states after each 32 byte block is transferred. <i>(There is no GFRAME# -- GIRDY# relationship for AGP transactions.)</i>
GTRDY#	I/O AGP	<b>Graphics Target Ready:</b> New meaning. GTRDY# indicates the AGP compliant target is ready to provide read data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait states after each block (32 bytes) is transferred on both read and write transactions.
GSTOP#	I/O AGP	<b>Graphics Stop:</b> Same as PCI. Not used by AGP.
GDEVSEL#	I/O AGP	<b>Graphics Device Select:</b> Same as PCI. Not used by AGP.
GREQ#	I AGP	<b>Graphics Request:</b> Same as PCI. (Used to request access to the bus to initiate a PCI or AGP request.)
GGNT#	O AGP	<b>Graphics Grant:</b> Same meaning as PCI but additional information is provided on ST[2:0]. The additional information indicates that the selected master is the recipient of previously requested read data (high or normal priority), it is to provide write data (high or normal priority), for a previously queued write command or has been given permission to start a bus transaction (AGP or PCI).
GAD[31:0]	I/O AGP	<b>Graphics Address/Data:</b> Same as PCI.
GC/BE[3:0]#	I/O AGP	<b>Graphics Command/Byte Enables:</b> Slightly different meaning. Provides command information (different commands than PCI) when requests are being queued when using PIPE#. Provide valid byte information during AGP write transactions and are not used during the return of read data.
GPAR	I/O AGP	<b>Graphics Parity:</b> Same as PCI. Not used on AGP transactions, but used during PCI transactions as defined by the PCI specification.

**NOTE:**

- AGP Sideband Addressing Signals.** The above table contains two mechanisms to queue requests by the AGP master. Note that the master can only use one mechanism. When PIPE# is used to queue addresses the master is not allowed to queue addresses using the SBA bus. For example, during configuration time, if the master indicates that it can use either mechanism, the configuration software will indicate which mechanism the master will use. Once this choice has been made, the master will continue to use the mechanism selected until the master is reset (and reprogrammed) to use the other mode. This change of modes is not a dynamic mechanism but rather a static decision when the device is first being configured after reset.

2. PCI signals are redefined when used in AGP transactions carried using AGP protocol extension. For transactions on the AGP interface carried using PCI protocol these signals completely preserve PCI semantics. The exact role of all PCI signals during AGP transactions is in Table 2-6.
3. The LOCK# signal is not supported on the AGP interface (even for PCI operations).
4. PCI signals described in Table 2-4 behave according to PCI 2.1 specifications when used to perform PCI transactions on the AGP Interface.

## 2.6 Clocks, Reset, and Miscellaneous

Table 2-7. Clocks, Reset, and Miscellaneous

Name	Type	Description
HCLKIN	I CMOS	<b>Host Clock In:</b> This pin receives a buffered host clock. This clock is used by all of the 82443BX logic that is in the Host clock domain. When SUSTAT# is active, there is an internal 100K ohm pull down on this signal.
PCLKIN	I CMOS	<b>PCI Clock In:</b> This is a buffered PCI clock reference that is synchronously derived by an external clock synthesizer component from the host clock. This clock is used by all of the 82443BX logic that is in the PCI clock domain. When SUSTAT# is active, there is an internal 100K ohm pull down on this signal.
DCLKO	O CMOS	<b>SDRAM Clock Out:</b> 66 or 100 MHz SDRAM clock reference. It feeds an external buffer clock device that produces multiple copies for the DIMMs.
DCLKWR	I CMOS	<b>SDRAM Write Clock:</b> Feedback reference from the external SDRAM clock buffer. This clock is used by the 82443BX when writing data to the SDRAM array. Note: See the Design Guide for routing constraints.
PCIRST#	I CMOS	<b>PCI Reset:</b> When asserted, this signal will reset the 82443BX logic. All PCI output and bi-directional signals will also tri-state compliant to PCI Rev 2.0 and 2.1 specifications. When SUSTAT# is active, there is an internal 100K ohm pull down on this signal.
GCLKIN	I CMOS	<b>AGP Clock In:</b> The GCLKIN input is a feedback reference from the GCLKOUT signal.
GCLKO	O CMOS	<b>AGP Clock Out:</b> The frequency is 66 MHz. The GCLKOUT output is used to feed both the reference input pin on the 82443BX and the AGP compliant device.
CRESET#	O CMOS	<b>Delayed CPU Reset:</b> CRESET# is a delayed copy of CPURST#. This signal is used to control the multiplexer for the CPU strap signals. CRESET# is delayed from CPURST# by two host clocks. Note: This pin requires an external pull-up resistor. If not used, no pull up is required.
TESTIN#	I CMOS	<b>Test Input:</b> This pin is used for manufacturing, and board level test purposes. Note: This pin has an internal 50K ohm pull-up.

Table 2-8. Power Management Interface

Name	Type	Description
CLKRUN#	I/OD CMOS	<b>Primary PCI Clock Run:</b> The 82443BX requests the central resource (PIIX4E) to start or maintain the PCI clock by the assertion of CLKRUN#. The 82443BX tristates CLKRUN# upon deassertion of PCIRST# (since CLK is running upon deassertion of reset). If connected to PIIX4E an external 2.7K Ohm pull-up is required for Desktop, Mobile requires (8.2k–10K) pull-up. Otherwise, a 100 Ohm pull down is required.
SUSTAT#	I CMOS	<b>Suspend Status (from PIIX):</b> SUSTAT# signals the system suspend state transition from the PIIX4E. It is used to isolate the suspend voltage well and enter/exit DRAM self-refresh mode. During POS/STR SUSTAT# is active.
BXPWROK	I CMOS	<b>BX Power OK:</b> BXPWROK input must be connected to the PWROK signal that indicates valid power is applied to the 82443BX.

Table 2-9. Reference Pins

Name	Description
GTLREF[B:A]	GTL Buffer voltage reference input
VTT[B:A]	GTL Threshold voltage for early clamps
VCC	Power pin @ 3.3V
VSS	Ground
REF5V	PCI 5V reference voltage (for 5V tolerant buffers)
AGPREF	External Input Reference

## 2.7 Power-Up/Reset Strap Options

Table 2-10 is the list of all power-up options that are loaded into the 82443BX during cold reset. The 82443BX is required to float all the signals connected to straps during cold reset and keep them floated for a minimum of 4 host clocks after the end of cold reset sequence. Cold reset sequence is performed when the 82443BX power is applied.

**Note:** All signals used to select power-up strap options are connected to either internal pull-down or pull-up resistors of minimum 50K ohms (maximum is 150K). That selects a default mode on the signal during reset. To enable different modes, external pull ups or pull downs (the opposite of the internal resistor) of approximately 10K ohm can be connected to particular signals. These pull up or pull down resistors should be connected to the 3.3V power supply.

During normal operation of the 82443BX, including while it is in suspend mode, the paths from GND or Vcc to internal strapping resistors are disabled to effectively disable the resistors. In these cases, the MAB# lines are driven by the 82443BX to a valid voltage levels.

**Note:** Note that when resuming from suspend, even while PCIRST# is active, the MAB# lines remain driven by the 82443BX and the strapping latches maintain the value stored during the cold reset.

This first column in Table 2-10 lists the signal that is sampled to obtain the strapping option. The second column shows which register the strapping option is loaded into. The third column is a description of what functionality the strapping selects.

The GTL+ signals are connected to the VTT through the normal pull-ups. CPU bus straps controlled by the 82443BX (e.g. A7# and A15#), are driven active at least six clocks prior to the active-to-inactive edge of CPURST# and driven inactive four clocks after the active-to-inactive edge of the CPURST#.



Table 2-10. Strapping Options

Signal	Register Name[bit]	Description
MAB13#		<b>Reserved.</b>
MAB12#	NBXCFC[13]	<b>Host Frequency Select:</b> If MAB#12 is strapped to 0, the host bus frequency is 60/66 MHz. If MAB#12 is strapped to 1, the host bus frequency is 100 MHz. An internal pull-down is used to provide the default setting of 66 MHz.
MAB11#	NBXCFC[2]	<b>In-Order Queue Depth Enable.</b> If MAB11# is strapped to 0 during the rising edge of PCIRST#, then the 82442BX will drive A7# low during the CPURST# deassertion. This forces the CPU bus to be configured for non-pipelined operation. If MAB11 is strapped to 1 (default), then the 82443BX does not drive the A7# low during reset, and A7# is sampled in default non-driven state (i.e. pulled-up as far as GTL+ termination is concerned) then the maximum allowable queue depth by the CPU bus protocol is selected (i.e., 8). Note that internal pull-up is used to provide pipelined bus mode as a default.
MAB10	PMCR[3]	<b>Quick Start Select.</b> The value on this pin at reset determines which stop clock mode is used. MAB10 = 0 (default) for normal stop clock mode. If MAB10 = 1 during the rising edge of PCIRST#, then the 82443BX will drive A15# low during CPURST# deassertion. This will configure the CPU for Quick Start mode of operation. Note that internal pull-down is used to provide normal stop clock mode as a default.
MAB9#	PMCR[1]	<b>AGP Disable:</b> When strapped to a 1, the AGP interface is disabled, all AGP signals are tri-stated and isolated. When strapped to a 0 (default), the AGP interface is enabled. When MMCONFIG is strapped active, we require that AGP_DISABLE is also strapped active. When MMCONFIG is strapped inactive, AGP_DISABLE can be strapped active or inactive but IDSEL_REDIRECT (bit 16 in NBXCFC register) must never be activated. This signal has an internal pull-down resistor.
MAB8#		<b>Reserved.</b>
MAB7#	DRAMC[5]	<b>Memory Module Configuration, MMCONFIG:</b> When strapped to a 1, the 82443BX configures its DRAM interface in a 430-TX compatible manner. These unused inputs are isolated while unused outputs are tri-stated: RASB[5:0]#/CSB[5:0]#, CKE[3:2]/CSA[7:6]#, CKE[5:4]/CSB[7:6]#, CASB[5,1]#/DQMB[5,1], GCKE/CKE1, MAA[13:0], DCLKO. When strapped to a 0 (default), the 82443BX DRAM signal are used normally. IDSEL_REDIRECT (bit 16 in NBXCFC register) is programmed by BIOS, before it begins with device enumeration process. The combination of SDRAMPWR (SDRAMC register) and MMCONFIG (DRAMC register) determine the functioning of the CKE signals. Refer to the DRAMC register for more details. Note that internal pull-down is used to set the DRAM interface to a normal configuration, as a default.
MAB6#	none	<b>Host Bus Buffer Mode Select:</b> When strapped 0, the desktop GTL+ 66 MHz or 100 MHz host bus buffers are used (default). When strapped '1', the mobile Low Power GTL+ 66 MHz host bus buffers are selected. Note that internal pull-down is used to set the host bus buffers to a desktop configuration as a default. External pull-up therefore is needed for mobile systems, only.
A[15]#	none	<b>Quick Start Select.</b> The value on A15# sampled at the rising edge of CPURST# will reflect if the quick start/stop clock mode is enabled in the processors.
A7#	none	<b>In-order Queue Depth Status.</b> The value on A[7]# sampled at the rising edge of CPURST# reflects if the IOQD is set to 1 or maximum allowable by the CPU bus.

**NOTE:**

- Proper strapping must be used to define logical values for these signals. Default value "0", or "1" provided by the internal pull-up or pull-down resistor can be overridden by the external pull-up, or pull-down resistor.



# Register Description

## 3

The 82443BX contains two sets of software accessible registers, accessed via the Host CPU I/O address space:

1. Control registers that are I/O mapped into the CPU I/O space. These registers control access to PCI and AGP configuration space.
2. Internal configuration registers residing within the 82443BX, partitioned into two logical device register sets ("logical" since they reside within a single physical device). The first register set is dedicated to Host-to-PCI Bridge functionality. This set (device 0) controls PCI interface operations, DRAM configuration, and other chip-set operating parameters and optional features. The second register set (device 1) is dedicated to Host-to-AGP Bridge functions (controls AGP interface configurations and operating parameters).

The following nomenclature is used for register access attributes.

RO	<b>Read Only.</b> If a register is read only, writes to this register have no effect.
R/W	<b>Read/Write.</b> A register with this attribute can be read and written
R/WC	<b>Read/Write Clear.</b> A register bit with this attribute can be read and written. However, a write of a 1 clears (sets to 0) the corresponding bit and a write of a 0 has no effect.
R/WO	<b>Read/Write Once.</b> A register bit with this attribute can be written to only once after power up. After the first write, the bit becomes read only.
R/WL	<b>Read/Write/Lock.</b> This register includes a lock bit. Once the lock bit has been set to 1, the register becomes read only.

The 82443BX supports PCI configuration space access using the mechanism denoted as Configuration Mechanism #1 in the PCI specification.

The 82443BX internal registers (both I/O Mapped and Configuration registers) are accessible by the Host CPU. The registers can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFADD which can only be accessed as a Dword. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field).

Some of the 82443BX registers described in this section contain reserved bits. These bits are labeled "Reserved". Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back.

**Note:** Software does not need to perform read, merge, write operation for the configuration address register.

In addition to reserved bits within a register, the 82443BX contains address locations in the configuration space of the Host-to-PCI Bridge entity that are marked either "Reserved" or "Intel Reserved". The 82443BX responds to accesses to "Reserved" address locations by completing the host cycle. When a "Reserved" register location is read, a zero value is returned. ("Reserved" registers can be 8-, 16-, or 32-bit in size). Writes to "Reserved" registers have no effect on the



82443BX. Registers that are marked as “Intel Reserved” must not be modified by system software. Writes to “Intel Reserved” registers may cause system failure. Reads to “Intel Reserved” registers may return a non-zero value. Software should not write to reserved configuration locations in the device-specific region (above address offset 3Fh)

Upon reset, the 82443BX sets its internal configuration registers to predetermined default states. However, there are a few exceptions to this rule.

1. When a reset occurs during the POS/STR state, several configuration bits are not reset to their default state. These bits are noted in the following register description.
2. Some register values at reset are determined by external strapping options.

The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the 82443BX registers accordingly.

## 3.1 I/O Mapped Registers

The 82443BX contains three registers that reside in the CPU I/O address space – the Configuration Address (CONFADD) Register, the Configuration Data (CONFDATA) Register, and the Power Management Control Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

### 3.1.1 CONFADD—Configuration Address Register

I/O Address:	0CF8h Accessed as a Dword
Default Value:	00000000h
Access:	Read/Write
Size:	32 bits

CONFADD is a 32 bit register accessed only when referenced as a Dword. A Byte or Word reference will “pass through” the Configuration Address Register onto the PCI bus as an I/O cycle. The CONFADD register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Descriptions
31	<b>Configuration Enable (CFGE).</b> When this bit is set to 1 accesses to PCI configuration space are enabled. If this bit is reset to 0 accesses to PCI configuration space are disabled.
30:24	<b>Reserved.</b>
23:16	<b>Bus Number.</b> When the Bus Number is programmed to 00h the target of the Configuration Cycle is either the 82443BX or the PCI Bus that is directly connected to the 82443BX, depending on the Device Number field. A type 0 Configuration Cycle is generated on PCI if the Bus Number is programmed to 00h and the 82443BX is not the target. If the Bus Number is non-zero a type 1 configuration cycle is generated on PCI or AGP with the Bus Number mapped to AD[23:16] during the address phase.
15:11	<b>Device Number.</b> This field selects one agent on the PCI bus selected by the Bus Number. During a Type 1 Configuration cycle this field is mapped to AD[15:11]. During a Type 0 Configuration Cycle this field is decoded and one bit among AD[31:11] is driven to a 1. The 82443BX is always Device Number 0 for the Host-to-PCI bridge entity and Device Number 1 for the Host- AGP entity. Therefore, the 82443BX internally references the AD11 and AD12 pins as corresponding IDSELs for the respective devices during PCI configuration cycles. NOTE: The AD11 and AD12 must not be connected to any other PCI bus device as IDSEL signals.
10:8	<b>Function Number.</b> This field is mapped to AD[10:8] during PCIX configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The 82443BX only responds to configuration cycles with a function number of 000b; all other function number values attempting access to the 82443BX (Device Number = 0 and 1, Bus Number = 0) will generate a master abort.
7:2	<b>Register Number.</b> This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to AD[7:2] during PCI configuration cycles.
1:0	<b>Reserved.</b>

### 3.1.2 CONFDATA—Configuration Data Register

I/O Address: 0CFCh  
 Default Value: 00000000h  
 Access: Read/Write  
 Size: 32 bits

CONFDATA is a 32 bit read/write window into configuration space. The portion of configuration space that is referenced by CONFDATA is determined by the contents of CONFADD.

Bit	Descriptions
31:0	<b>Configuration Data Window (CDW).</b> If bit 31 of CONFADD is 1 any I/O reference that falls in the CONFDATA I/O space will be mapped to configuration space using the contents of CONFADD.

### 3.1.3 PM2\_CTL—ACPI Power Control 2 Control Register

I/O Address: 0022h  
 Default Value: 00h  
 Access: Read/Write  
 Size: 8 bits

This register is used to disable both the PCI and AGP arbiters in the 82443BX to prevent any external bus masters from acquiring the PCI or AGP bus. Any currently running PCI cycles will terminate properly.

Accesses to this register are controlled by the Power Management Control Register (Offset 7Ah). When bit 6 of the PMCR is set to '1', the ACPI Register at I/O location 0022h is enabled. When bit 6 is set to '0', I/O accesses to location 0022h are forwarded to PCI or AGP (if within programmable IO range).

Bit	Description
7:1	Reserved
0	<p><b>Primary PCI and AGP Arbiter Request Disable (ARB_DIS).</b> When this bit is set to 1, the 82443BX will not respond to any PCI REQ# signals, AGP requests, or PHOLD# from PIIX4E going active until this bit is set back to 0. Only External AGP and PCI requests are masked from the arbiters. If the PIIX is in passive release mode, masking will not occur until an active release is seen via PHLDA# assertion. This prevents possible deadlock.</p> <p>ARB_DIS has no effect on AGP side band signals or AGP data transfer requests.</p>

## 3.2 PCI Configuration Space Access

The 82443BX implementation manifests two PCI devices within a single physical component body:

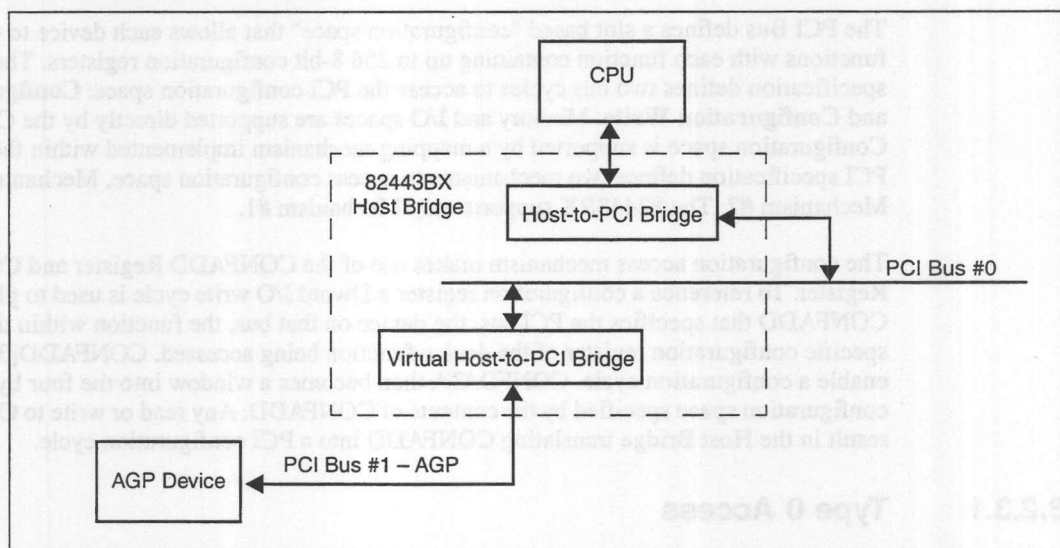
- Device 0 = Host-to-PCI Bridge = PCI bus #0 interface, Main Memory Controller, Graphics Aperture controller, 82443BX specific AGP control registers.
- Device 1 = Host-to-AGP interface = "Virtual" PCI-to-PCI Bridge, including AGP address space mapping, normal PCI interface, and associated AGP sideband signal control.

Corresponding configuration registers for both devices are mapped as devices residing on PCI (bus 0). Configuration register layout and functionality for the Device #0 should be inspected carefully, as new features added to the 82443BX initiated a reasonable level of change relative to other proliferation's of the Pentium® Pro processor AGPsets (i.e. 440FX, 440LX). Configuration registers of the 82443BX Device #1 are based on the normal configuration space template of a PCI-to-PCI Bridge as described in the *PCI to PCI Bridge Architecture Specification*.

Figure 3-1 shows the PCI bus hierarchy for the 82443BX). In the PCI bus hierarchy, the primary PCI bus is the highest level bus in the hierarchy and is PCI bus #0. The PCI-to-PCI bridge function provides access to the AGP/PCI bus 0. This bus is below the primary bus in the PCI bus hierarchy and is represented as PCI Bus #1.



Figure 3-1. 82443BX PCI Bus Hierarchy



### 3.2.1 Configuration Space Mechanism Overview

The 82443BX supports two bus interfaces: PCI (referenced as Primary PCI) and AGP (referenced as AGP). The AGP interface is treated as a second PCI bus from the configuration point of view. The following sections describe the configuration space mapping mechanism associated with both buses.

**Note:** The configuration space for device #1 is controlled by the AGP\_DIS bit in the PMCR register. When the AGP\_DIS bit (PMCR[1]) is set to 0, the configuration space for device #1 is enabled, and the registers for device #1 are accessible through the configuration mechanism defined below. When the AGP\_DIS bit (PMCR[1]) is set to 1, the configuration space for device #1 is disabled. All configuration cycles (reads and writes) to device #1 of bus 0 will cause the master abort status bit for device #0/ bus 0 to be set. Configuration read cycles will return data of all 1's. Configuration write cycles will have no effect on the registers.

### 3.2.2 Routing the Configuration Accesses to PCI or AGP

Routing of configuration accesses to AGP is controlled via PCI-to-PCI bridge normal mechanism using information contained within the PRIMARY BUS NUMBER, the SECONDARY BUS NUMBER, and the SUBORDINATE BUS NUMBER registers of the Host-to-AGP internal "virtual" PCI-to-PCI bridge device. Detailed description of the mechanism for translating CPU I/O bus cycles to configuration cycles on one of the two buses is described below.

To distinguish between PCI configuration cycles targeting the two logical device register sets supported in the 82443BX, this document refers to the Host-to-PCI bridge PCI interface as PCI and the Host- AGP PCI interface as AGP.

### 3.2.3 PCI Bus Configuration Mechanism Overview

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to 8 functions with each function containing up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: **Configuration Read** and **Configuration Write**. Memory and I/O spaces are supported directly by the CPU. Configuration space is supported by a mapping mechanism implemented within the chip-set. The PCI specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The 82443BX supports only Mechanism #1.

The configuration access mechanism makes use of the CONFADD Register and CONFDATA Register. To reference a configuration register a Dword I/O write cycle is used to place a value into CONFADD that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFADD[31] must be 1 to enable a configuration cycle. CONFDATA then becomes a window into the four bytes of configuration space specified by the contents of CONFADD. Any read or write to CONFDATA will result in the Host Bridge translating CONFADD into a PCI configuration cycle.

#### 3.2.3.1 Type 0 Access

If the Bus Number field of CONFADD is 0, a Type 0 Configuration cycle is performed on PCI (i.e. bus #0). CONFADD[10:2] is mapped directly to AD[10:2]. The Device Number field of CONFADD is decoded onto AD[31:11]. The Host-to-PCI Bridge entity within the 82443BX is accessed as Device #0 on the PCI bus segment. The Host- /AGP Bridge entity within the 82443BX is accessed as Device #1 on the PCI bus segment. To access Device #2, the 82443BX will assert AD13, for Device #3 will assert AD14, and so forth up to Device #20 for which will assert AD31. Only one AD line is asserted at a time. All device numbers higher than 20 cause a type 0 configuration access with no IDSEL asserted, which will result in a Master Abort.

#### 3.2.3.2 Type 1 Access

If the Bus Number field of CONFADD is non-zero, then a Type 1 Configuration cycle is performed on PCI bus (i.e. bus #0). CONFADD[23:2] is mapped directly to AD[23:2]. AD[1:0] are driven to 01 to indicate a Type 1 Configuration cycle. All other lines are driven to 0.

### 3.2.4 AGP Bus Configuration Mechanism Overview

This mechanism is compatible with PCI mechanism #1 supported for the PCI bus as defined above. The configuration mechanism is the same for both accessing AGP or PCI-only devices attached to the AGP interface.

### 3.2.5 Mapping of Configuration Cycles on AGP

From the AGPset configuration perspective, AGP is seen as another PCI bus interface residing on a Secondary Bus side of the “virtual” PCI-to-PCI bridge referred to as the 82443BX Host- AGP bridge. On the Primary bus side, the “virtual” PCI-to-PCI bridge is attached to the BUS #0 referred to in this document as the PCI interface. The “virtual” PCI-to-PCI bridge entity is used to map Type #1 PCI Bus Configuration cycles on PCI onto Type #0 or Type #1 configuration cycles on the AGP interface.

Type 1 configuration cycles on PCI that have a BUS-NUMBER that matches the SECONDARY-BUS-NUMBER of the “virtual” PCI to PCI bridge will be translated into Type 0 configuration cycles on the AGP interface. Type 1 configuration cycles on PCI that have a BUS-NUMBER that is behind the “virtual” P2P bridge will be translated into Type 1 configuration cycles on the AGP interface.

**Note:** The PCI bus supports a total of 21 devices by mapping bits 15:11 of the CONFADD to the IDSEL lines on AD[31:11]. For secondary PCI busses (including the AGP bus), only 16 devices are supported by mapping bits 15:11 of the CONFADD to the IDSEL lines (AD[31:16]).

To prepare for mapping of the configuration cycles on AGP the initialization software will go through the following sequence:

1. Scan all devices residing on the PCI bus (i.e., Bus #0) using Type 0 configuration accesses.
2. For every device residing at bus #0 which implements PCI-to-PCI bridge functionality, it will configure the secondary bus of the bridge with the appropriate number and scan further down the hierarchy. This process will include the configuration of the “virtual” PCI-to-PCI Bridge within the 82443BX used to map the AGP address space in a software specific manner.



### 3.3 Host-to-PCI Bridge Registers (Device 0)

Table 3-1 shows the 82443BX configuration space for device #0.

**Table 3-1. 82443BX Register Map — Device 0 (Sheet 1 of 2)**

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	7190h/7192h	RO
04–05h	PCICMD	PCI Command Register	0006h	R/W
06–07h	PCISTS	PCI Status Register	0210h/0200h	RO, R/WC
08	RID	Revision Identification	00/01h/02h	RO
09	—	Reserved	00h	—
0Ah	SUBC	Sub-Class Code	00h	RO
0Bh	BCC	Base Class Code	06h	RO
0Ch	—	Reserved	00h	—
0Dh	MLT	Master Latency Timer	00h	R/W
0Eh	HDR	Header Type	00h	RO
10–13h	APBASE	Aperture Base Address	00000008h	R/W,RO
14–2Bh	—	Reserved	00h	—
2C–2Dh	SVID	Subsystem Vendor Identification	00h	R/WO
2E–2Fh	SID	Subsystem Identification	00h	R/WO
30–33h	—	Reserved	00h	—
34h	CAPPTR	Capabilities Pointer	A0h/00h	RO
35–4Fh	—	Reserved	00h	—
50–53h	NBXCFC	440BX Configuration	[0000h]:[00S0_0000_0000S_0S00b]	R/W
54–56h	—	Reserved	00h	—
57h	DRAMC	DRAM Control	00S0_0000b	R/W
58h	DRAMT	DRAM Timing	03h	R/W
59–5Fh	PAM[6:0]	Programmable Attribute Map (7 registers)	00h	R/W
60–67h	DRB[7:0]	DRAM Row Boundary (8 registers)	01h	R/W
68h	FDHC	Fixed DRAM Hole Control	00h	R/W
69–6Eh	MBSC	Memory Buffer Strength Control	0000-0000-0000h	R/W
6F–70h	—	Reserved	00h	—
71h	—	Intel Reserved	1Fh	—
72h	SMRAM	System Management RAM Control	02h	R/W
73h	ESMRAMC	Extended System Management RAM Control.	38h	R/W
74–75h	RPS	SDRAM Row Page Size	0000h	R/W
76–77h	SDRAMC	SDRAM Control Register	0000h	R/W
78–79h	PGPOL	Paging Policy Register	00h	R/W
7Ah	PMCR	Power Management Control Register	0000_S0S0b	R/W
7B–7Ch	SCRR	Suspend CBR Refresh Rate Register	0038h	R/W
7D–7Fh	—	Reserved	00h	—

Table 3-1. 82443BX Register Map — Device 0 (Sheet 2 of 2)

Address Offset	Register Symbol	Register Name	Default Value	Access
80–83h	EAP	Error Address Pointer Register	00000000h	RO, R/WC
84–8Fh	—	Reserved	00h	—
90h	ERRCMD	Error Command Register	80h	R/W
91–92h	ERRSTS	Error Status Register	0000h	R/WC, RO
93h	—	Reserved	00h	R/W
94–97h	—	Intel Reserved	00006104h	—
98–99h	—	Intel Reserved	0500h	—
9Ah	—	Intel Reserved	00h	—
9B–9Fh	—	Reserved	—	—
A0–A3h	ACAPID	AGP Capability Identifier	00100002h 00000000h	RO
A4–A7h	AGPSTAT	AGP Status Register	1F000203h	RO
A8–ABh	AGPCMD	AGP Command Register	00000000h	RW
AC–AFh	—	Reserved	00h	—
B0–B3h	AGPCTRL	AGP Control Register)	00000000h	R/W
B4h	APSIZE	Aperture Size Control Register	00h	R/W
B5–B7h	—	Reserved	00h	—
B8–BBh	ATTBASE	Aperture Translation Table	00000000h	R/W
BCh	—	Reserved	—	—
BDh	—	Reserved	—	—
BE–BFh	—	Reserved	00h	—
C0–C3h	—	Intel Reserved	00000000h	—
C4–C7h	—	Intel Reserved	00000000h	—
C8h	—	Intel Reserved	18h	—
C9h	—	Intel Reserved	0Ch	—
CA–CCh	MBFS	Memory Buffer Frequency Select	000000h	R/W
CD–CFh	—	Reserved	00h	—
D0–D7h	BSPAD	BIOS Scratch Pad	00...00h	R/W
D8–DFh	—	Intel Reserved	000....000h	—
E0–E7h	DWTC	DRAM Write Thermal Throttling Control	000....000h	R/W/L
E8–EFh	DRTC	DRAM Read Thermal Throttling Control	000....000h	R/W/L
F0–F1h	BUFFC	Buffer Control Register	0000h	R/W/L
F2–F7h	—	Intel Reserved	0000F800h	—
F8–FBh	—	Intel Reserved	0000F20h	—
FC–FFh	—	Intel Reserved	00000000h	—

**NOTES:**

1. The 'S' symbol represents the strapping option.
2. Write operations must not be attempted to the Intel Reserved registers.

### 3.3.1 VID—Vendor Identification Register (Device 0)

Address Offset: 00–01h  
 Default Value: 8086h  
 Attribute: Read Only  
 Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identify any PCI device. Writes to this register have no effect.

Bit	Description
15:0	<b>Vendor Identification Number.</b> This is a 16-bit value assigned to Intel. Intel VID = 8086h.

### 3.3.2 DID—Device Identification Register (Device 0)

Address Offset: 02–03h  
 Default Value: 7190h/7192h  
 Attribute: Read Only  
 Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	<b>Device Identification Number.</b> This is a 16 bit value assigned to the 82443BX Host-to-PCI Bridge Function #0. 7190h = When the AGP_DIS bit (PMCR[1]) is set to 0, the DID = 7190h. 7192h = When the AGP_DIS bit is set to 1, the DID = 7192h.



### 3.3.3 PCICMD—PCI Command Register (Device 0)

Address Offset: 04–05h  
Default: 0006h  
Access: Read/Write  
Size: 16 bits

This 16-bit register provides basic control over the 82443BX PCI interface ability to respond to PCI cycles. The PCICMD Register enables and disables the SERR# signal, 82443BX response to PCI special cycles, and enables and disables PCI bus master accesses to main memory.

Bit	Descriptions
15:10	Reserved.
9	<b>Fast Back-to-Back.</b> Fast back-to-back cycles to different PCI targets are not implemented by the 82443BX. 0 = Hardwired to 0.
8	<b>SERR# Enable (SERRE).</b> Note that this bit only controls SERR# for the PCI bus. Device #1 has its own SERRE bit to control error reporting for the bus conditions occurred on the AGP bus. Two control bits are used in a logical OR manner to control SERR# pin driver. 1 = If this bit is set to a 1, the 82443BX's SERR# signal driver is enabled and SERR# is asserted when an error condition occurs, and the corresponding bit is enabled in the ERRCMD register. The error status is reported in the ERRSTS and PCISTS registers. Also, if this bit is set and the 82443BX's PCI parity error reporting is enabled by the PERRE bit located in this register, then the 82443BX will report address and data parity errors (when it is potential target). 0 = SERR# is never driven by the 82443BX.
7	<b>Address/Data Stepping.</b> Not implemented (hardwired to 0).
6	<b>Parity Error Enable (PERRE).</b> Note that the PERR# signal is not implemented by the 82443BX. 1 = Enable. Address and data parity errors are reported via SERR# mechanism (if enabled via SERRE bit). 0 = Disable. Address and data parity errors are not reported via the 82443BX SERR# signal. (NOTE: Other types of error conditions can be still signaled via SERR# mechanism.) NOTE: The 82443BX PCI bus interface is still required to generate parity even if parity error reporting is disabled via this bit.
5	Reserved.
4	<b>Memory Write and Invalidate Enable.</b> The 82443BX never uses this command. 0 = Hardwired to 0.
3	<b>Special Cycle Enable.</b> The 82443BX ignores all special cycles generated on the PCI. 0 = Hardwired to 0.
2	<b>Bus Master Enable (BME).</b> The 82443BX does not support disabling of its bus master capability on the PCI Bus. 1 = Hardwired to 1, permitting the 82443BX to function as a PCI Bus master.
1	<b>Memory Access Enable (MAE).</b> This bit enables/disables PCI master access to main memory (DRAM). The 82443BX always allows PCI master access to main memory. 1 = Hardwired to 1.
0	<b>I/O Access Enable (IOAE).</b> The 82443BX does not respond to PCI bus I/O cycles. 0 = Hardwired to 0.

### 3.3.4 PCISTS—PCI Status Register (Device 0)

Address Offset: 06–07h  
 Default Value: 0210h/0200h  
 Access: Read Only, Read/Write Clear  
 Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI master abort and PCI target abort on the PCI bus. PCISTS also indicates the DEVSEL# timing that has been set by the 82443BX hardware for target responses on the PCI bus. Bits [15:12] and bit 8 are read/write clear and bits [10:9] are read only.

Bit	Descriptions
15	<b>Detected Parity Error (DPE).</b> Note that the function of this bit is not affected by the PERRE bit. PERR# is not implemented in the 82443BX. 1 = Indicates 82443BX's detection of a parity error in the address or data phase of PCI bus transactions. 0 = Software sets DPE to 0 by writing a 1 to this bit.
14	<b>Signaled System Error (SSE).</b> 1 = This bit is set to 1 when the 82443BX asserts SERR# for any enabled error condition under device 0. 0 = Software sets SSE to 0 by writing a 1 to this bit.
13	<b>Received Master Abort Status (RMAS).</b> Note that Master abort is the normal and expected termination of PCI special cycles. 1 = When the 82443BX terminates a PCI bus transaction (82443BX is a PCI master) with an unexpected master abort, this bit is set to 1. 0 = Software resets this bit to 0 by writing a 1 to it.
12	<b>Received Target Abort Status (RTAS).</b> 1 = When a 82443BX-initiated PCI transaction is terminated with a target abort, RTAS is set to 1. The 82443BX also asserts SERR# if enabled in the ERRCMD register. 0 = Software resets RTAS to 0 by writing a 1 to it.
11	<b>Signaled Target Abort Status (STAS).</b> The 82443BX does not generate target abort. 0 = Hardwired to a 0
10:9	<b>DEVSEL# Timing (DEVT).</b> This 2-bit field indicates the timing of the DEVSEL# signal when the 82443BX responds as a target on PCI, and indicates the time when a valid DEVSEL# can be sampled by the initiator of the PCI cycle. 01 = Medium (hardwired to 01)
8	<b>Data Parity Detected (DPD).</b> 82443BX does not implement the PERR# pin. However, data parity errors are still detected and reported on SERR# (if enabled by SERRE and PERRE). 0 = Hardwired to 0
7	<b>Fast Back-to-Back (FB2B).</b> The 82443BX as a target does not support fast back-to-back transactions on the PCI bus. 0 = Hardwired to 0
6:5	Reserved.
4	<b>Capability List (CLIST).</b> 1 = When the AGP DIS bit (PMCR[1]) is set to 0, this bit is set to 1. 0 = When the AGP DIS bit (PMCR[1]) is set to 1, this bit is set 0.
3:0	Reserved.

### 3.3.5 RID—Revision Identification Register (Device 0)

Address Offset: 08h  
 Default Value: 02h  
 Access: Read Only  
 Size: 8 bits

This register contains the revision number of the 82443BX Function #0. These bits are read only and writes to this register have no effect.

Bit	Description
7:0	<b>Revision Identification Number.</b> This is an 8-bit value that indicates the revision identification number for the 82443BX Function #0. B-1 = 02h

### 3.3.6 SUBC—Sub-Class Code Register (Device 0)

Address Offset: 0Ah  
 Default Value: 00h  
 Access: Read Only  
 Size: 8 bits

This register contains the Sub-Class Code for the 82443BX Function #0. This code is 00h indicating a Host Bridge device. The register is read only.

Bit	Description
7:0	<b>Sub-Class Code (SUBC).</b> This is an 8-bit value that indicates the category of Bridge into which the 82443BX falls. The code is 00h indicating a Host Bridge.

### 3.3.7 BCC—Base Class Code Register (Device 0)

Address Offset: 0Bh  
 Default Value: 06h  
 Access: Read Only  
 Size: 8 bits

This register contains the Base Class Code of the 82443BX Function #0. This code is 06h indicating a Bridge device. This register is read only.

Bit	Description
7:0	<b>Base Class Code (BASEC).</b> This is an 8-bit value that indicates the Base Class Code for the 82443BX. This code has the value 06h, indicating a Bridge device.



### 3.3.8 MLT—Master Latency Timer Register (Device 0)

Address Offset: 0Dh  
 Default Value: 00h  
 Access: Read/Write  
 Size: 8 bits

This register controls the amount of time that 82443BX can burst data on the PCI Bus as a PCI master. The MLT[2:0] bits are reserved and assumed to be 0 when determining the Count Value.

Bit	Description
7:3	<b>Master Latency Timer Count Value for PCI Bus Access.</b> MLT is an 8-bit register that controls the amount of time the 82443BX, as a PCI bus master, can burst data on the PCI Bus. The default value of MLT is 00h and disables this function. For example, if the MLT is programmed to 18h, then the value is 24 PCI clocks.
2:0	Reserved.

### 3.3.9 HDR—Header Type Register (Device 0)

Offset: 0Eh  
 Default: 00h  
 Access: Read Only  
 Size: 8 bits

This register identifies the header layout of the configuration space.

Bit	Descriptions
7:0	<b>Header Type (HEADT).</b> This read only field always returns 0 when read. Writes have no affect on this field.

### 3.3.10 APBASE—Aperture Base Configuration Register (Device 0)

Offset: 10–13h  
 Default: 00000008h  
 Access: Read/Write, Read Only  
 Size: 32 bits

The APBASE is a normal PCI Base Address register that is used to request the base of the Graphics Aperture. The normal PCI Configuration mechanism defines the base address configuration register such that only a fixed amount of space can be requested (dependent on which bits are hardwired to “0” or behave as hardwired to “0”). To allow for flexibility (of the aperture) an additional register called APSIZE is used as a “back-end” register to control which bits of the APBASE will behave as hardwired to “0”. This register will be programmed by the 82443BX specific BIOS code that will run before any of the generic configuration software is run.

**Note:** Bit 9 of the NBXCFG register is used to prevent accesses to the aperture range before this register is initialized by the configuration software and appropriate translation table structure has been established in the main memory.

Bit	Description																																																								
31:28	<b>Upper Programmable Base Address bits (R/W).</b> These bits are used to locate the range size selected via lower bits 27:4. Default = 0000b																																																								
27:22	<b>Lower “Hardwired”/Programmable Base Address bits.</b> These bits behave as a “hardwired” or as a programmable depending on the contents of the APSIZE register as defined below: <table><tr><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>Aperture Size</th></tr><tr><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>4 MB</td></tr><tr><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>0</td><td>8 MB</td></tr><tr><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>0</td><td>0</td><td>16 MB</td></tr><tr><td>r/w</td><td>r/w</td><td>r/w</td><td>0</td><td>0</td><td>0</td><td>32 MB</td></tr><tr><td>r/w</td><td>r/w</td><td>0</td><td>0</td><td>0</td><td>0</td><td>64 MB</td></tr><tr><td>r/w</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>128 MB</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>256 MB</td></tr></table> <p>Bits 27:22 are controlled by the bits 5:0 of the APSIZE register in the following manner: If bit APSIZE[5]=0 then APBASE[27]=0 and if APSIZE[5]=1 then APBASE[27]=r/w (read/write). The same applies correspondingly to other bits. Default for APSIZE[5:0]=000000b forces default APBASE[27:22] =000000b (i.e., all bits respond as “hardwired” to 0). This provides a default to the maximum aperture size of 256 MB. The 82443BX specific BIOS is responsible for selecting smaller size (if required) before PCI configuration software runs and establishes the system address map.</p>	27	26	25	24	23	22	Aperture Size	r/w	r/w	r/w	r/w	r/w	r/w	4 MB	r/w	r/w	r/w	r/w	r/w	0	8 MB	r/w	r/w	r/w	r/w	0	0	16 MB	r/w	r/w	r/w	0	0	0	32 MB	r/w	r/w	0	0	0	0	64 MB	r/w	0	0	0	0	0	128 MB	0	0	0	0	0	0	256 MB
27	26	25	24	23	22	Aperture Size																																																			
r/w	r/w	r/w	r/w	r/w	r/w	4 MB																																																			
r/w	r/w	r/w	r/w	r/w	0	8 MB																																																			
r/w	r/w	r/w	r/w	0	0	16 MB																																																			
r/w	r/w	r/w	0	0	0	32 MB																																																			
r/w	r/w	0	0	0	0	64 MB																																																			
r/w	0	0	0	0	0	128 MB																																																			
0	0	0	0	0	0	256 MB																																																			
21:4	<b>Hardwired to “0”.</b> This forces minimum aperture size selected by this register to be 4MB.																																																								
3	<b>Prefetchable (RO).</b> This bit is hardwired to “1” to identify the Graphics Aperture range as a prefetchable ( i.e., the device returns all bytes on reads regardless of the byte enables), and the 82443BX may merge processor writes into this range without causing errors.																																																								
2:1	<b>Type (RO).</b> These bits determine addressing type and they are hardwired to “00” to indicate that address range defined by the upper bits of this register can be located anywhere in the 32-bit address space.																																																								
0	<b>Memory Space Indicator (RO).</b> Hardwired to “0” to identify aperture range as a memory range.																																																								

### 3.3.11 SVID—Subsystem Vendor Identification Register (Device 0)

Offset: 2C–2Dh  
Default: 0000h  
Access: Read/Write Once  
Size: 16 bits

Bit	Description
15:0	<b>Subsystem Vendor ID (R/WO).</b> This value is used to identify the vendor of the subsystem. The default value is 00h. This field should be programmed during boot-up. After this field is written once, it becomes read only.

### 3.3.12 SID—Subsystem Identification Register (Device 0)

Offset: 2E–2Fh  
 Default: 0000h  
 Access: Read/Write Once  
 Size: 16 bits

Bit	Description
15:0	<b>Subsystem ID (R/WO).</b> This value is used to identify a particular subsystem. The default value is 00h. This field should be programmed during boot-up. After this field is written once, it becomes read only.

### 3.3.13 CAPPTR—Capabilities Pointer Register (Device 0)

Offset: 34h  
 Default: A0h/00h  
 Access: Read Only  
 Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location where the AGP normal registers are located.

Bit	Description
7:0	<b>Pointer to the start of AGP normal register block.</b> A0h = When the AGP_DIS bit (PMCR[1]) is set to 0, the value in this field is A0h. 00h = When the AGP_DIS bit (PMCR[1]) is set to 1, this field is set to 00h.

### 3.3.14 NBXCFG—NBX Configuration Register (Device 0)

Offset: 50–53h  
 Default: bits 31–16: 0000h  
           bits 15–0: 00S0-0000-000S-0S00b  
 Access: Read/Write, Read Only for strapping options  
 Size: 32 bits

Bit	Description
31:24	<b>SDRAM Row Without ECC.</b> Bit[n] of this 8 bit array corresponds to row[n] of the SDRAM array. When reading a SDRAM row (DIMM) which is none-ECC, the 82 443BX drives the ECC data lines during the first data transfer in a burst read. 0 = ECC components are populated in this row. The 82443BX will not drive the ECC signals. 1 = ECC components are not populated in this row. The 82443BX will drive the ECC lines in the first read data transferred when this row is addressed.
23:19	Reserved.
18	<b>Host Bus Fast Data Ready Enable (HBFDR).</b> 0 = Assertion of DRAM data on host bus occurs one clock after sampling snoop results. (default) 1 = Assertion of DRAM data on host bus occurs on the same clock the snoop result is being sampled. This mode is faster by one clock cycle.



Bit	Description
17	<b>ECC - EDO static Drive mode.</b> 0 = Normal mode of operation (default). 1 = ECC signals are always driven. This mode is used in a mobile system. EDO components are used, but ECC components are not populated in any of the DRAM rows.
16	<b>IDSEL_REDIRECT.</b> This is a programmable option to make the 82443BX compatible with 430TX base design. For CPU initiated configuration cycles to PCI, Device 1 which are targeted to the 82443BX's host to AGP bridge: 0 = When set to '0' (default), IDSEL1 (or AD12) is allocated to this bridge. The external AD12 is never activated. CPU initiated configuration cycles to BUS0, DEVICE7 are targeted a PCI bus device that its IDSEL input is connected to IDSEL7 (AD18). 1 = When set to '1', IDSEL7 (or AD18) is allocated to this bridge. Since it is internal in the 82443BX, the external AD18 is never activated. CPU initiated configuration cycles to BUS0, DEVICE7 are targeted a PCI bus device that its IDSEL input is connected to IDSEL1 (AD12). In some 430TX based systems, this is connected to PIIX4E. Note that CPU initiated configuration cycles to other PCI buses or other devices are normally mapped and are not affected.
15	<b>WSC# Handshake Disable.</b> In the Uni-Processor mode, this bit should be set to '1'. In the Dual-Processor mode where external IOAPIC is used, this bit should be set to '0' (default). Setting this bit to '0', enables the WSC# handshake mechanism.
14	Intel Reserved.
13:12	<b>Host/DRAM Frequency.</b> These bits are used to determine the host and DRAM frequency. Bit 13 is set by an external strapping option at reset. These bits are also used to select the required refresh rate. These bits apply to both SDRAM and EDO, with the exception that the setting '00' for 100 MHz is illegal for an EDO system. 00 = 100 MHz 01 = Reserved 10 = 66 MHz 11 = Reserved
11	<b>AGP to PCI Access Enable.</b> When PHLDA# is active or there is an outstanding passive release transaction pending: 1) this bit is set to 1 and the 82443BX allows AGP to PCI traffic, or 2) this bit is set to 0 (default) and the 82443BX blocks AGP to PCI traffic. The AGP to PCI traffic must not target the ISA bus. 1 = Enable 0 = Disable
10	<b>PCI Agent to Aperture Access Disable.</b> This bit is used to prevent access to the aperture from the PCI side. 1 = Disable 0 = Enable (default). If this bit is "0" (default) and bit 9 = 1, accesses to the aperture are enabled for the PCI side. Note: This bit is don't care if bit 9 of this register = 0.
9	<b>Aperture Access Global Enable.</b> This bit is used to prevent access to the aperture from any port (CPU, PCI or AGP) before aperture range is established by the configuration software and appropriate translation table in the main DRAM has been initialized. Default is "0". It must be set after system is fully configured for aperture accesses. 1 = Enable. Note that this bit globally controls accesses to the aperture. Once enabled, bit 10 provides the next level of control for accesses originated from the PCI side. 0 = Disable
8:7	<b>DRAM Data Integrity Mode (DDIM) (R/W).</b> These bits select one of 4 DRAM data integrity modes. 00 = Non-ECC (Byte-Wise Writes supported) (Default) 01 = EC-only - Error Checking with No correction 10 = ECC Mode (Error Checking/Correction) 11 = ECC Mode with hardware scrubbing enabled

Bit	Description												
6	<b>ECC Diagnostic Mode Enable (EDME) (R/W).</b> 1 = Enable. When this bit is set to 1, the 82443BX will enter ECC Diagnostic test mode and the 82443BX forces the MECC[7:0] lines to 00h for all writes to memory. During reads, the read MECC[7:0] lines are compared against internally generated ECC. Recognized errors are indicated via the ERRSTS register as in normal ECC operation. 0 = Normal operation mode (default).												
5	<b>MDA Present (MDAP).</b> This bit is used to indicate the presence of a secondary monochrome adapter on the PCI bus, while the primary graphics controller is on the AGP bus. This bit works in conjunction with the VGA_EN bit (Register 3E, bit 3 of device 1) as follows: <table><tr><th>VGA_EN</th><th>MDAP</th><th>Description</th></tr><tr><td>0</td><td>X</td><td><b>All VGA cycles are sent to PCI.</b> PCI master cycles to the VGA range are not claimed by the 82443BX.</td></tr><tr><td>1</td><td>0</td><td><b>All VGA cycles are sent to AGP.</b> PCI master writes to VGA range are claimed by the 82443BX and forwarded to the AGP bus.</td></tr><tr><td>1</td><td>1</td><td><b>All VGA cycles are sent to AGP, except</b> for cycles in the MDA range (or the aliased ranges defined below). PCI master writes in the VGA range (outside of the MDA range) are claimed by the 82443BX and forwarded to AGP. PCI and AGP master read/writes to the MDA range are ignored by the 82443BX.</td></tr></table> The MDA ranges are a subset of the VGA ranges as follows: Memory: 0B0000h–0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh	VGA_EN	MDAP	Description	0	X	<b>All VGA cycles are sent to PCI.</b> PCI master cycles to the VGA range are not claimed by the 82443BX.	1	0	<b>All VGA cycles are sent to AGP.</b> PCI master writes to VGA range are claimed by the 82443BX and forwarded to the AGP bus.	1	1	<b>All VGA cycles are sent to AGP, except</b> for cycles in the MDA range (or the aliased ranges defined below). PCI master writes in the VGA range (outside of the MDA range) are claimed by the 82443BX and forwarded to AGP. PCI and AGP master read/writes to the MDA range are ignored by the 82443BX.
VGA_EN	MDAP	Description											
0	X	<b>All VGA cycles are sent to PCI.</b> PCI master cycles to the VGA range are not claimed by the 82443BX.											
1	0	<b>All VGA cycles are sent to AGP.</b> PCI master writes to VGA range are claimed by the 82443BX and forwarded to the AGP bus.											
1	1	<b>All VGA cycles are sent to AGP, except</b> for cycles in the MDA range (or the aliased ranges defined below). PCI master writes in the VGA range (outside of the MDA range) are claimed by the 82443BX and forwarded to AGP. PCI and AGP master read/writes to the MDA range are ignored by the 82443BX.											
4	Reserved.												
3	<b>USWC Write Post During I/O Bridge Access Enable (UWPIO) (R/W).</b> 1 = Enable. Host USWC writes to PCI memory are posted. 0 = Disable. Posting of USWC is not allowed.												
2	<b>In-Order Queue Depth (IOQD) (RO).</b> This bit reflects the value sampled on A7# on the deassertion of the CPURST#. It indicates the depth of the Pentium® Pro processor bus in-order queue (i.e., level of Pentium Pro processor bus pipelining). 1 = In-order queue = maximum. If A7# is sampled “1” (i.e., undriven on the Pentium Pro processor bus), the depth of the Pentium Pro processor bus in-order queue is configured to the maximum allowed by the Pentium Pro processor protocol (i.e., 8). However, the actual maximum supported by the 82443BX is 4, and it is controlled by the 82443BX’s Pentium Pro processor interface logic using the BNR# signaling mechanism. 0 = A7# is sampled asserted (i.e., “0”). The depth of the Pentium Pro processor bus in-order queue is set to 1 (i.e., no pipelining support on the Pentium Pro processor bus). NOTE: During reset, A7# can be driven either by the 82443BX or by an external source as defined by the strapping option on the MAB11# pin.												
1:0	Reserved.												

### 3.3.15 DRAMC—DRAM Control Register (Device 0)

Address Offset: 57h  
Default Value: 00S0\_0000b  
Access: Read/Write  
Size: 8 bits

Bit	Description												
7:6	Reserved.												
5	<p><b>Module Mode Configuration (MMCONFIG).</b> This bit is set by an external strapping option. The combination of this bit and the SDRAMPWR bit (SDRAMC register) determine the functioning of the CKE signals as defined as follows:</p> <table><tr><th>SDRAMPWR</th><th>MMCONFIG</th><th>CKE Operation</th></tr><tr><td>0</td><td>0</td><td>3 DIMM, CKE[5:0] driven, self-refresh entry staggered. SDRAM dynamic power down available.</td></tr><tr><td>X</td><td>1</td><td>3 DIMM, CKE0 only, self-refresh entry not staggered. SDRAM dynamic power down unavailable.</td></tr><tr><td>1</td><td>0</td><td>4 DIMM, GCKE only, self-refresh entry staggered. SDRAM dynamic power down unavailable.</td></tr></table> <p><b>NOTE:</b> Under MMCONFIG mode, the AGP must be disabled.</p>	SDRAMPWR	MMCONFIG	CKE Operation	0	0	3 DIMM, CKE[5:0] driven, self-refresh entry staggered. SDRAM dynamic power down available.	X	1	3 DIMM, CKE0 only, self-refresh entry not staggered. SDRAM dynamic power down unavailable.	1	0	4 DIMM, GCKE only, self-refresh entry staggered. SDRAM dynamic power down unavailable.
SDRAMPWR	MMCONFIG	CKE Operation											
0	0	3 DIMM, CKE[5:0] driven, self-refresh entry staggered. SDRAM dynamic power down available.											
X	1	3 DIMM, CKE0 only, self-refresh entry not staggered. SDRAM dynamic power down unavailable.											
1	0	4 DIMM, GCKE only, self-refresh entry staggered. SDRAM dynamic power down unavailable.											
4:3	<p><b>DRAM Type (DT).</b> This field indicates the DRAM type used to populate the entire array. When set to 00, EDO timings are used for all cycles to main memory. When set to 01, SDRAM timings are used for all cycles to memory. When set to 10, timings for memory cycles accommodate Registered SDRAMs. For registered SDRAM timings, all address and control lines to the SDRAMs are assumed to be registered, while memory data and ECC bits are not registered. EDO, SDRAM and Registered SDRAM cannot be mixed within a system.</p> <p>00 = EDO 01 = SDRAM 10 = Registered SDRAM 11 = Reserved</p> <p><b>NOTE:</b> When PCIRST# assertion occurs during POS/STR, this bit is not reset to '0'.</p>												
2:0	<p><b>DRAM Refresh Rate (DRR).</b> The DRAM refresh rate is adjusted according to the frequency selected by this field. Disabling the refresh cycle (000) results in the eventual loss of DRAM data. Changing DRR value will reset the refresh request timer. This field is used in conjunction with the SDRAM frequency bits in the NBXCFG register to determine the correct load value for the refresh timer.</p> <p>000 = Refresh Disabled 001 = 15.6 us 010 = 31.2 us 011 = 62.4 us 100 = 124.8 us 101 = 249.6 us 110 = Reserved 111 = Reserved</p> <p><b>NOTE:</b> When PCIRST# assertion occurs during POS/STR, this bit is not reset to '0'.</p>												



### 3.3.16 DRAMT—DRAM Timing Register (Device 0)

Address Offset: 58h  
 Default Value: 03h  
 Access: Read/Write  
 Size: 8 bits

This 8-bit register controls main memory DRAM timings. Refer to the DRAM section for details regarding the DRAM timings programmed in this register.

Bit	Description
7:2	Reserved.
1	<b>EDO RAS# Wait State (RWS).</b> When RWS = 1, one additional wait state is inserted before RAS# is asserted for row misses. This provides one clock of additional MAX[13:0] setup time to RAS# assertion. This bit does not affect page misses since the MAX[13:0] lines are setup several clocks in advance of RAS# assertion for page misses. 0 = 1 tASR 1 = 2 tASR
0	<b>EDO CAS# Wait State (CWS).</b> When CWS = 1, one additional wait state is inserted before the assertion of the first CAS# for page hit cycles. This allows one additional clock of MA setup time to the CAS# for the leadoff page hit cycle. Page miss and row miss timings are not affected by this bit. 0 = 1 Tasc 1 = 2 Tasc

### 3.3.17 PAM[6:0]—Programmable Attribute Map Registers (Device 0)

Address Offset: 59h (PAM0) – 5Fh (PAM6)  
 Default Value: 00h  
 Attribute: Read/Write

The 82443BX allows programmable memory attributes on 13 *Legacy* memory segments of various sizes in the 640 KB to 1 MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the Pentium Pro processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

- RE Read Enable.** When RE = 1, the host read accesses to the corresponding memory segment are claimed by the 82443BX and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI.
- WE Write Enable.** When WE = 1, the host write accesses to the corresponding memory segment are claimed by the 82443BX and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM Register controls two regions, typically 16 KB in size. Each of these regions has a 4-bit field. The four bits that control each region have the same encoding and are defined in Table 3-2.

Table 3-2. Attribute Bit Assignment

Bits [7, 3] Reserved	Bits [6, 2] Reserved	Bits [5, 1] WE	Bits [4, 0] RE	Description
x	x	0	0	<b>Disabled.</b> DRAM is disabled and all accesses are directed to PCI. The 82443BX does not respond as a PCI target for any read or write access to this area.
x	x	0	1	<b>Read Only.</b> Reads are forwarded to DRAM and writes are forwarded to PCI for termination. This write protects the corresponding memory segment. The 82443BX will respond as a PCI target for read accesses but not for any write accesses.
x	x	1	0	<b>Write Only.</b> Writes are forwarded to DRAM and reads are forwarded to the PCI for termination. The 82443BX will respond as a PCI target for write accesses but not for any read accesses.
x	x	1	1	<b>Read/Write.</b> This is the normal operating mode of main memory. Both read and write cycles from the host are claimed by the 82443BX and forwarded to DRAM. The 82443BX will respond as a PCI target for both read and write accesses.

As an example, consider a BIOS that is implemented on the expansion bus. During the initialization process, the BIOS can be shadowed in main memory to increase the system performance. When BIOS is shadowed in main memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The host then does a write of the same address, which is directed to main memory. After the BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus. Table 3-3 shows the PAM registers and the associated attribute bits:

Table 3-3. PAM Registers and Associated Memory Segments

PAM Reg	Attribute Bits				Memory Segment	Comments	Offset
PAM0[3:0]	Reserved						59h
PAM0[7:4]	R	R	WE	RE	0F0000h – 0FFFFFh	BIOS Area	59h
PAM1[3:0]	R	R	WE	RE	0C0000h – 0C3FFFh	ISA Add-on BIOS <sup>1</sup>	5Ah
PAM1[7:4]	R	R	WE	RE	0C4000h – 0C7FFFh	ISA Add-on BIOS <sup>1</sup>	5Ah
PAM2[3:0]	R	R	WE	RE	0C8000h – 0CBFFFh	ISA Add-on BIOS <sup>1</sup>	5Bh
PAM2[7:4]	R	R	WE	RE	0CC000h – 0CFFFFh	ISA Add-on BIOS <sup>1</sup>	5Bh
PAM3[3:0]	R	R	WE	RE	0D0000h – 0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	R	WE	RE	0D4000h – 0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	R	WE	RE	0D8000h – 0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	R	WE	RE	0DC000h – 0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	R	WE	RE	0E0000h – 0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	R	WE	RE	0E4000h – 0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	R	WE	RE	0E8000h – 0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	R	WE	RE	0EC000h – 0EFFFFh	BIOS Extension	5Fh

**NOTE:**

1. The C0000h to CFFFFh segment can be used for SMM space if enabled by the SMRAM register

**DOS Application Area (00000h–9FFFFh)**

The DOS area is 640 KB and it is further divided into two parts. The 512 KB area at 0 to 7FFFFh is always mapped to the main memory controlled by the 82443BX, while the 128 KB address range from 080000 to 09FFFFh can be mapped to PCI or to main DRAM. By default this range is mapped to main memory and can be declared as a main memory hole (accesses forwarded to PCI) via 82443BX's FDHC configuration register.

**Video Buffer Area (A0000h–BFFFFh)**

This 128 KB area is not controlled by attribute bits. The host-initiated cycles in this region are always forwarded to either PCI or AGP unless this range is accessed in SMM mode. *Routing of accesses is controlled by the Legacy VGA control mechanism of the "virtual" PCI-to-PCI bridge device embedded within the 82443BX.*

This area can be programmed as SMM area via the SMRAM register. When used as a SMM space this range can not be accessed from PCI or AGP.

**Expansion Area (C0000h–DFFFFh)**

This 128 KB area is divided into eight 16 KB segments which can be assigned with different attributes via PAM control register as defined by Table 3-3.

**Extended System BIOS Area (E0000h–EFFFFh)**

This 64 KB area is divided into four 16 KB segments which can be assigned with different attributes via PAM control register as defined by the Table 3-3.

**System BIOS Area (F0000h–FFFFFh)**

This area is a single 64 KB segment which can be assigned with different attributes via PAM control register as defined by the Table 3-3.

**3.3.18 DRB[0:7]—DRAM Row Boundary Registers (Device 0)**

Address Offset:	60h (DRB0) – 67h (DRB7)
Default Value:	01h
Access:	Read/Write
Size:	8 bits/register

The 82443BX supports 8 physical rows of DRAM. The width of a row is 64 bits. The DRAM Row Boundary Registers define upper and lower addresses for each DRAM row. Contents of these 8-bit registers represent the boundary addresses in 8 MB granularity. For example, a value of 01h indicates 8 MB.

60h	DRB0 = Total memory in row0 (in 8 MB)
61h	DRB1 = Total memory in row0 + row1 (in 8 MB)
62h	DRB2 = Total memory in row0 + row1 + row2 (in 8 MB)
63h	DRB3 = Total memory in row0 + row1 + row2 + row3 (in 8 MB)
64h	DRB4 = Total memory in row0 + row1 + row2 + row3 + row4 (in 8 MB)
65h	DRB5 = Total memory in row0 + row1 + row2 + row3 + row4 + row5 (in 8 MB)
66h	DRB6 = Total memory in row0 + row1 + row2 + row3 + row4 + row5 + row6 (in 8 MB)
67h	DRB7 = Total memory in row0 + row1 + row2 + row3 + row4 + row5 + row6 + row7 (in 8 MB)



The DRAM array can be configured with single or double-sided DIMMs using 2MX8, 4Mx16, or 8Mx8 parts. The array also supports x4 width DRAM components on registered DIMMs. Each register defines an address range that will cause a particular CS# line (or RAS# in the EDO case) to be asserted (e.g., if the first DRAM row is minus 8 MB, then accesses within the 0 to 8 MByte range will cause CSx0#/RASx0# to be asserted). The DRAM Row Boundary (DRB) Registers are programmed with an 8-bit upper address limit value. This upper address limit is compared to bits [30:23] of the requested address, for each row, to determine if DRAM is being targeted.

**Note:** DRAM is selected only if address[31:30] are zero.

Bit	Description
7:0	<b>Row Boundary Address.</b> This 8-bit value is compared against address lines A[30:23] to determine the upper address limit of a particular row (i.e., DRB minus previous DRB = row size). NOTE: When PCIRST# assertion occurs during POS/STR, these bits are not reset to '01h'.

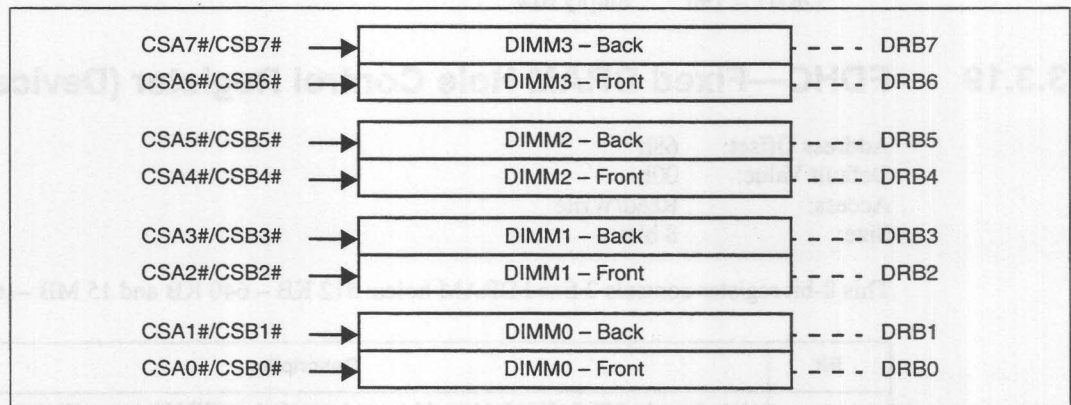
#### Row Boundary Address

These 8 bit values represent the upper address limits of the eight rows (i.e., this row minus previous row = row size). Unpopulated rows have a value equal to the previous row (row size = 0). DRB7 reflects the maximum amount of DRAM in the system. The top of memory is determined by the value written into DRB7.

**Note:** The 82443BX supports a maximum of 1 GB of DRAM using registered SDRAM DIMMs. (an example of this configuration is 4 double-sided registered DIMMs using 16Mx4 parts).

As an example of a general purpose configuration where eight physical rows are configured for either single-sided or double-sided DIMMs, the memory array would be configured like the one shown in Figure 3-2. In this configuration, the 82443BX drives eight CS# signals directly to the DIMM rows. If single-sided DIMMs are populated, the even CS# signals are used and the odd CS#s are not connected. If double-sided DIMMs are used, all four CS# signals are used per DIMM.

**Figure 3-2. SDRAM DIMMs and Corresponding DRB Registers**



The following 2 examples describe how the DRB Registers are programmed for cases of single-sided and double-sided DIMMs on a motherboard.

#### Example #1 Single-sided DIMMs

Assume a total of 16 MB of DRAM are required using single-sided 1MB x 64 DIMMs. In this configuration, two DIMMs are required.

DRB0 = 01h	populated (1 DIMM, 8 Mbyte this row)
DRB1 = 01h	empty row
DRB2 = 02h	populated (1 DIMM, 8 Mbyte this row)
DRB3 = 02h	empty row
DRB4 = 02h	empty row
DRB5 = 02h	empty row
DRB6 = 02h	empty row
DRB7 = 02h	empty row

#### Example #2 Mixed Single-/Double-sided DIMMs

As another example, consider a system that is initially shipped with 8 MB of memory using a 1M x 64 DIMM and that rest of the memory array should be upgradable up to a maximum supported memory of 200 MB. This can be handled by further populating the array with one 16M x 64 single-sided DIMM (one row) and one 8M x 64 double-sided DIMM (two rows), yielding a total of 200 MB of DRAM. The DRB Registers are programmed as follows:

DRB0 = 01h	populated with 8 MB, 1MB x 64 single-sided DIMM
DRB1 = 01h	empty row
DRB2 = 05h	populated with 32 MB, 1/2 of 8M x 64 DIMM
DRB3 = 09h	populated with 32 MB, the other 1/2 of 8M x 64 DIMM
DRB4 = 19h	populated with 128 MB, 16M x 64 single-sided DIMM
DRB5 = 19h	empty row
DRB6 = 19h	empty row
DRB7 = 19h	empty row

### 3.3.19 FDHC—Fixed DRAM Hole Control Register (Device 0)

Address Offset:	68h
Default Value:	00h
Access:	Read/Write
Size:	8 bits

This 8-bit register controls 2 fixed DRAM holes: 512 KB – 640 KB and 15 MB – 16 MB.

Bit	Description
7:6	<b>Hole Enable (HEN).</b> This field enables a memory hole in DRAM space. Host cycles matching an enabled hole are passed on to PCI. PCI cycles matching an enabled hole will be ignored by the 82443BX (no DEVSEL#). NOTE: A selected hole is not remapped. 00 = None 01 = 512 KB–640 KB (128 KB bytes) 10 = 15 MB – 16 MB (1 MB byte) 11 = Reserved
5:0	Reserved.

### 3.3.20 MBSC—Memory Buffer Strength Control Register (Device 0)

Address Offset: 69–6Eh  
Default Value: 000000000000h  
Access: Read/Write  
Size: 48 bits

This register programs the various DRAM interface signal buffer strengths, based on non-mixed memory configurations of DRAM type (EDO or SDRAM), DRAM density (x8, x16, or x32), DRAM technology (16MB or 64 MB), and rows populated. Note that x4 DRAM may only be supported when used on registered DIMMs.

**Note:** The choice of 100 MHz or 66 MHz buffer is independent of bus frequency. It is possible to select a 100 MHz memory buffer even though the bus frequency is 66 MHz (and vice versa).

Bit	Description
47:40	Reserved
39:38	<b>MAA[13:0], WEA#, SRASA#, SCASA# Buffer Strengths.</b> This field sets the buffer strength for the MAA[13:0], WEA#, SRASA#, SCASA# pins. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)
37:36	<b>MAB[12:11, 9:0]# &amp; MAB[13,10], WEB#, SRASB#, SCASB# Buffer Strengths.</b> This field sets the buffer strength for MAB[12:11, 9:0]# & MAB[13,10], WEB#, SRASB#, SCASB# pins. Note that the address's MAB# are inverted copies of MAA, with the exception of MAB[13,10]. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)
35:34	<b>MD [63:0] Buffer Strength Control 2.</b> <b>4 DIMM FET Configuration:</b> This field sets the buffer strength for the MD[63:0] path that is connected to DIMM2 and DIMM3. The buffer strength is programmable based on the SDRAM load in detected in <b>DIMM slots 2&amp;3</b> . This path is enabled when FENA is asserted (High) by the 82443BX. <b>3 DIMM &amp; 4 DIMM non-FET Configuration:</b> This field should be programmed to the same value as MD[63:0] Buffer Strength Control 1. This buffer strength is programmable based upon the SDRAM load detected in all DIMM connectors. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (100 MHz only)
33:32	<b>MD [63:0] Buffer Strength Control 1.</b> <b>4 DIMM FET Configuration:</b> This field sets the buffer strength for the MD[63:0] path that is connected to DIMM0 and DIMM1. The buffer strength is programmable based upon the SDRAM load in detected in <b>DIMM slots 0&amp;1</b> . This path is enabled when FENA is asserted (Low) by the 82443BX. <b>3 DIMM &amp; 4 DIMM non-FET Configurations:</b> The buffer strength is programmable based upon the SDRAM load detected in all DIMM connectors. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (100 MHz only)



Bit	Description
31:30	<p><b>MECC [7:0] Buffer Strength Control 2.</b></p> <p><b>4 DIMM FET Configuration:</b> This field sets the buffer strength for the MECC[7:0] path that is connected to DIMM2 and DIMM3. The buffer strength is programmable based upon the SDRAM ECC load detected in <b>DIMM slots 2&amp;3</b>. This path is enabled when FENA is deasserted (High) by the 82443BX.</p> <p><b>3 DIMM &amp; 4 DIMM non-FET Configurations:</b> This field should be programmed to the same value as MECC[7:0] Buffer Strength Control 1. This buffer strength is programmable based upon the SDRAM ECC load detected in all DIMM connectors.</p> <p>00 = 1x (66 MHz &amp; 100 MHz)  01 = Reserved (Invalid setting)  10 = 2x (66 MHz &amp; 100 MHz)  11 = 3x (100 MHz only)</p>
29:28	<p><b>MECC [7:0] Buffer Strength Control 1.</b></p> <p><b>4 DIMM FET Configuration:</b> This field sets the buffer strength for the MECC[7:0] path that is connected to DIMM0 and DIMM1. The buffer strength is programmable based upon the SDRAM ECC load detected in <b>DIMM slots 0&amp;1</b>. This path is enabled when FENA is deasserted (High) by the 82443BX.</p> <p><b>3 DIMM &amp; 4 DIMM non-FET Configuration:</b> The buffer strength is programmable based upon the SDRAM ECC load detected in all DIMM slots.</p> <p>00 = 1x (66 MHz &amp; 100 MHz)  01 = Reserved (Invalid setting)  10 = 2x (66 MHz &amp; 100 MHz)  11 = 3x (100 MHz only)</p>
27:26	<p><b>CSB7#/CKE5 Buffer Strength.</b> This field sets the buffer strength for CSB7#/CKE5 pins.</p> <p>00 = 1x (66 MHz &amp; 100 MHz)  01 = Reserved (Invalid setting)  10 = 2x (66 MHz &amp; 100 MHz)  11 = 3x (66 MHz &amp; 100 MHz)</p>
25:24	<p><b>CSA7#/CKE3 Buffer Strength.</b> This field sets the buffer strength for CSA7#/CKE3 pins.</p> <p>00 = 1x (66 MHz &amp; 100 MHz)  01 = Reserved (Invalid setting)  10 = 2x (66 MHz &amp; 100 MHz)  11 = 3x (66 MHz &amp; 100 MHz)</p>
23:22	<p><b>CSB6#/CKE4 Buffer Strength.</b> This field sets the buffer strength for CSB6#/CKE4 pins.</p> <p>00 = 1x (66 MHz &amp; 100 MHz)  01 = Reserved (Invalid setting)  10 = 2x (66 MHz &amp; 100 MHz)  11 = 3x (66 MHz &amp; 100 MHz)</p>
21:20	<p><b>CSA6#/CKE2 Buffer Strength.</b> This field sets the buffer strength for CSA6#/CKE2 pins.</p> <p>00 = 1x (66 MHz &amp; 100 MHz)  01 = Reserved (Invalid setting)  10 = 2x (66 MHz &amp; 100 MHz)  11 = 3x (66 MHz &amp; 100 MHz)</p>
19	<p><b>CSA5#/RASA5#, CSB5#/RASB5# Buffer Strength.</b> This field sets the buffer strength for the CSA5#/RASA5#, CSB5#/RASB5# pins.</p> <p>0 = 1x (66 MHz &amp; 100 MHz)  1 = 2x (66 MHz &amp; 100 MHz)</p>
18	<p><b>CSA4#/RASA4#, CSB4#/RASB4# Buffer Strength.</b> This field sets the buffer strength for the CSA4#/RASA4#, CSB4#/RASB4# pins.</p> <p>0 = 1x (66 MHz &amp; 100 MHz)  1 = 2x (66 MHz &amp; 100 MHz)</p>
17	<p><b>CSA3#/RASA3#, CSB3#/RASB3# Buffer Strength.</b> This field sets the buffer strength for the CSA3#/RASA3#, CSB3#/RASB3# pins.</p> <p>0 = 1x (66 MHz &amp; 100 MHz)  1 = 2x (66 MHz &amp; 100 MHz)</p>

Bit	Description
16	<b>CSA2#/RASA2#, CSB2#/RASB2# Buffer Strength.</b> This field sets the buffer strength for the CSA2#/RASA2#, CSB2#/RASB2# pins. 0 = 1x (66 MHz & 100 MHz) 1 = 2x (66 MHz & 100 MHz)
15	<b>CSA1#/RASA1#, CSB1#/RASB1# Buffer Strength.</b> This field sets the buffer strength for the CSA1#/RASA1#, CSB1#/RASB1# pins. 0 = 1x (66 MHz & 100 MHz) 1 = 2x (66 MHz & 100 MHz)
14	<b>CSA0#/RASA0#, CSB0#/RASB0# Buffer Strength.</b> This field sets the buffer strength for the CSA0#/RASA0#, CSB0#/RASB0# pins. 0 = 1x (66 MHz & 100 MHz) 1 = 2x (66 MHz & 100 MHz)
13:12	<b>DQMA5/CASA5# Buffer Strength.</b> This field sets the buffer strength for the DQMA5/CASA5# pins. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz only)
11:10	<b>DQMA1/CASA1# Buffer Strength.</b> This field sets the buffer strength for the DQMA1/CASA1# pin. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)
9:8	<b>DQMB5/CASB5# Buffer Strength.</b> This field sets the buffer strength for the DQMB5/CASB5# pin. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz only)
7:6	<b>DQMB1/CASB1# Buffer Strength.</b> This field sets the buffer strength for the DQMB1/CASB1# pin. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz only)
5:4	<b>DQMA[7:6,4:2,0]/CASA[7:6,4:2,0]# Buffer Strength.</b> This field sets the buffer strength for the DQMA[7:6]/CASA[7:6]#, DQMA[4:2]/CASA[4:2]#, and the DQMA[0]/CASA[0]# pins. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)
3:2	<b>CKE1/GCKE Buffer Strength.</b> This field sets the buffer strength for the CKE1 pin. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)
1:0	<b>CKE0/FENA Buffer Strength.</b> This field sets the buffer strength for the CKE0/FENA pin. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)

### 3.3.21 SMRAM—System Management RAM Control Register (Device 0)

Address Offset: 72h  
 Default Value: 02h  
 Access: Read/Write  
 Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G\_SMROME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

Bit	Description
7	Reserved
6	<b>SMM Space Open (D_OPEN).</b> When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. When D_LCK is set to a 1, D_OPEN is reset to 0 and becomes read only.
5	<b>SMM Space Closed (D_CLS).</b> When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference "through" SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
4	<b>SMM Space Locked (D_LCK).</b> When D_LCK is set to 1 then D_OPEN is reset to 0 and D_LCK, D_OPEN, H_SMRAM_EN, TSEG_SZ, TSEG_EN and DRB7 become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a power-on reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	<b>Global SMRAM Enable (G_SMROME).</b> If G_SMROME is set to a 1 and H_SMRAM_EN is set to 0, then Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADS# with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details.  Once D_LCK is set, this bit becomes read only.
2:0	<b>Compatible SMM Space Base Segment (C_BASE_SEG) (RO).</b> This field programs the location of SMM space. "SMM DRAM" is not remapped. It is simply "made visible" if the conditions are right to access SMM space, otherwise the access is forwarded to PCI.  010 = Hardwired to 010 to indicate that the 82443BX supports the SMM space at A0000h-BFFFFh.



### 3.3.22 ESMRAMC—Extended System Management RAM Control Register (Device 0)

Address Offset: 73h  
Default Value: 38h  
Access: Read/Write  
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E\_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 Mbyte.

Bit	Description
7	<b>H_SMRAM_EN (H_SMRAME).</b> Controls the SMM memory space location (i.e above 1 Mbyte or below 1 Mbyte). 1 = When G_SMRAME is 1 and H_SMRAME is set to 1, the High SMRAM memory space is enabled, the Compatible SMRAM memory is disabled, and accesses in the 0A0000h to 0FFFFFFh range are forwarded to PCI, while SMRAM accesses from 100A0000h to 100FFFFFFh are remapped to DRAM address A0000h to FFFFFFFh 0 = When G_SMRAME is set to a 1 and H_SMRAM_EN is set to 0, then the Compatible SMRAM space is enabled. Once D_LCK is set, this bit becomes read only.
6	<b>E_SMRAM_ERR (E_SMERR).</b> 1 = This bit is set when CPU accesses the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. 0 = It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	<b>SMRAM_Cache (SM_CACHE).</b> This bit is forced to '1' by 82443BX.
4	<b>SMRAM_L1_EN (SM_L1).</b> This bit is forced to '1' by 82443BX.
3	<b>SMRAM_L2_EN (SM_L2).</b> This bit is forced to '1' by 82443BX.
2:1	<b>TSEG_SZ[1:0] (T_SZ).</b> Selects the size of the TSEG memory block, if enabled. This memory is taken from the top of DRAM space (i.e., TOM - TSEG_SZ), which is no longer claimed by the memory controller (all accesses to this space are sent to the PCI bus if TSEG_EN is set). The physical address for the extended SMRAM memory appears is from (256M + TOM - TSEG_SZ) to (256M + TOM). This address is remapped to DRAM address (TOM - TSEG_SZ) to TOM. This field decodes as follows: 00 = (TOM-128KB) to TOM 01 = (TOM-256KB) to TOM 10 = (TOM-512KB) to TOM 11 = (TOM-1MB) to TOM Once D_LCK is set, this bit becomes read only.
0	<b>TSEG_EN (T_EN).</b> Enabling of SMRAM memory (TSEG, 128 KB, 256 KB, 512 KB or 1 MB of additional SMRAM memory) for Extended SMRAM space only. When G_SMRAME = 1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Once D_LCK is set, this bit becomes read only.

### 3.3.23 RPS—SDRAM Row Page Size Register (Device 0)

Address Offset: 74h–75h  
 Default Value: 0000h  
 Access: Read/Write  
 Size: 16 bits

This register sets the row page size for SDRAM only. For EDO memory, the page size is fixed at 2 KB.

Bit	Description																		
	<b>Page Size (PS).</b> Each pair of bits in this register indicate the page size used for one row of DRAM. The encoding of the two bit fields.																		
	<table> <tr> <th>Bits[1:0]</th><th>Page Size</th></tr> <tr> <td>00</td><td>2 KB</td></tr> <tr> <td>01</td><td>4 KB</td></tr> <tr> <td>10</td><td>8 KB</td></tr> <tr> <td>11</td><td>Reserved</td></tr> </table>	Bits[1:0]	Page Size	00	2 KB	01	4 KB	10	8 KB	11	Reserved								
Bits[1:0]	Page Size																		
00	2 KB																		
01	4 KB																		
10	8 KB																		
11	Reserved																		
15:0	<table> <tr> <th>RPS bits</th><th>Corresponding DRB register</th></tr> <tr> <td>1:0</td><td>DRB[0], row 0</td></tr> <tr> <td>3:2</td><td>DRB[1], row 1</td></tr> <tr> <td>5:4</td><td>DRB[2], row 2</td></tr> <tr> <td>7:6</td><td>DRB[3], row 3</td></tr> <tr> <td>9:8</td><td>DRB[4], row 4</td></tr> <tr> <td>11:10</td><td>DRB[5], row 5</td></tr> <tr> <td>13:12</td><td>DRB[6], row 6</td></tr> <tr> <td>15:14</td><td>DRB[7], row 7</td></tr> </table>	RPS bits	Corresponding DRB register	1:0	DRB[0], row 0	3:2	DRB[1], row 1	5:4	DRB[2], row 2	7:6	DRB[3], row 3	9:8	DRB[4], row 4	11:10	DRB[5], row 5	13:12	DRB[6], row 6	15:14	DRB[7], row 7
RPS bits	Corresponding DRB register																		
1:0	DRB[0], row 0																		
3:2	DRB[1], row 1																		
5:4	DRB[2], row 2																		
7:6	DRB[3], row 3																		
9:8	DRB[4], row 4																		
11:10	DRB[5], row 5																		
13:12	DRB[6], row 6																		
15:14	DRB[7], row 7																		

### 3.3.24 SDRAMC—SDRAM Control Register (Device 0)

Address Offset: 76h–77h  
 Default Value: 00h  
 Access: Read/Write  
 Size: 16 bits

Bit	Description
15:10	Reserved
9:8	<b>Idle/Pipeline DRAM Leadoff Timing (IPDLT).</b> Adds a clock delay to the lead-off clock count when bits 9:8 are set to 01. All other settings are illegal.

Bit	Description
7:5	<p><b>SDRAM Mode Select (SMS).</b> These bits allow the 82443BX to drive various commands to the SDRAMs. These special modes are intended for initialization at power up.</p> <p><b>SMS Mode</b></p> <p>000 <b>Normal SDRAM Operation.</b> (default)</p> <p>001 <b>NOP Command Enable.</b> In this mode all CPU cycles to SDRAM result in NOP Command on the SDRAM interface.</p> <p>010 <b>All Banks Precharge Enable.</b> In this mode all CPU cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface.</p> <p>011 <b>Mode Register Set Enable.</b> In this mode all CPU cycles to SDRAM result in a mode register set command on the SDRAM interface. The Command is driven on the MAX[13:0] lines. MAX[2:0] must always be driven to 010 for burst of 4 mode. MA3 must be driven to 1 for interleave wrap type. MAX4 needs to be driven to the value programmed in the CAS# Latency bit. MAX[6:5] should always be driven to 01. MAX[12:7] must be driven to 000000. BIOS must calculate and drive the correct host address for each row of memory such that the correct command is driven on the MAX[12:0] lines.</p> <p>100 <b>CBR Enable.</b> In this mode all CPU cycles to SDRAM result in a CBR cycle on the SDRAM interface.</p> <p>101 <b>Reserved.</b></p> <p>110 <b>Reserved.</b></p> <p>111 <b>Reserved.</b></p> <p>Note: BIOS must take into consideration MAB inversion when programming for 3 and 4 DIMM.</p>
4	<p><b>SDRAMPWR.</b> The SDRAMPWR bit controls how the CKE signals are driven for different DRAM configurations. For a 3 DIMM configuration, SDRAMPWR should be set to '0'. For a 4 DIMM configuration, SDRAMPWR should be set to '1'. In this case the 82443BX drives a single CKE signal (GCKE). The combination of SDRAMPWR and MMCONFIG (DRAMC register) determine the functioning of the CKE signals. Refer to the DRAMC register (Section 3.3.15, "DRAMC—DRAM Control Register (Device 0)" on page 3-19) for more details.</p> <p>Note: When PCIRST# assertion occurs during POS/STR, these bits are not reset to 0.</p>
3	<p><b>Leadoff Command Timing (LCT).</b> These bits control when the SDRAM command pins (SRASx#, SCASx# and WEx#) and CSx# are considered valid on leadoffs for CPU cycles.</p> <p>0 = 4 CS# Clock</p> <p>1 = 3 CS# Clock</p> <p>The LCT Bit should be initialized by BIOS as recommended below:</p> <ul style="list-style-type: none"> <li>Desktop platforms running at 100 MHz should leave the LCT bit set to its default value of 0.</li> <li>Desktop platforms running at 66 MHz should leave the LCT bit set to its default value of 0, if load on either MAA or MAB signals is &gt; 9. Otherwise, set the LCT bit to 1, if load on both MAA and MAB is ≤ 9.</li> <li>Mobile platforms will be run at 66MHz and should set the LCT bit to 1.</li> </ul>
2	<p><b>CAS# Latency (CL).</b> This bit controls the number of CLKs between when a read command is sampled by the SDRAMs and when the 82443BX samples read data from the SDRAMs. If a given row is populated with a registered SDRAM DIMM, an extra clock is inserted between the read command and when the 82443BX samples read data. For a registered DIMM with CL=2, this bit should be set to 1.</p> <p>0 = 3 DCLK CAS# latency.</p> <p>1 = 2 DCLK CAS# latency.</p>
1	<p><b>SDRAM RAS# to CAS# Delay (SRCD).</b> This bit controls the number of DCLKs from a Row Activate command to a read or write command.</p> <p>0 = 3 clocks will be inserted between a row activate command and either a read or write command.</p> <p>1 = 2 clocks will be inserted between a row activate and either a read or write command.</p>
0	<p><b>SDRAM RAS# Precharge (SRP).</b> This bit controls the number of DCLKs for RAS# precharge.</p> <p>0 = 3 clocks of RAS# precharge.</p> <p>1 = 2 clocks of RAS# precharge.</p>



### 3.3.25 PGPOL—Paging Policy Register (Device 0)

Address Offset: 78–79h  
 Default Value: 0000h  
 Access: Read/Write  
 Size: 16 bits

Bit	Description
15:8	<b>Banks per Row (BPR).</b> Each bit in this field corresponds to one row of the memory array. Bit 15 corresponds to row 7 while bit 8 corresponds to row 0. These bits are defined only for SDRAM systems and define whether the corresponding row has a two bank implementation or a four bank implementation. Those with two banks (bit=0) can have up to two pages open at any given time. Those with four banks (bit=1) can have up to four pages open at any time. Note that the bits referencing empty rows are 'don't care'. 0 = 2 banks 1 = 4 banks
7:5	Reserved.
4	Intel Reserved.
3:0	<b>DRAM Idle Timer (DIT).</b> This field determines the number of clocks that the DRAM controller will remain in the idle state before precharging all pages. This field is used for both EDO and SDRAM memory systems. 0000 = 0 clocks 0001 = 2 clocks 0010 = 4 clocks 0011 = 8 clocks 0100 = 10 clocks 0101 = 12 clocks 0110 = 16 clocks 0111 = 32 clocks 1XXX = Infinite (pages are not closed for idle condition).

### 3.3.26 PMCR—Power Management Control Register (Device 0)

Address Offset: 7Ah  
Default Value: 0000\_S0S0b  
Access: Read/Write  
Size: 8 Bits

Bit	Description
7	<b>Power Down SDRAM Enable (PDSE).</b> 1 = Enable. When PDSE=1, an SDRAM row in idle state will be issued a power down command. The SDRAM row will exit power down mode only when there is a request to access this particular row. 0 = Disable
6	<b>ACPI Control Register Enable (SCRE).</b> 1 = Enable. The ACPI control register in the 82443BX is enabled, and all CPU cycles to IO address 0022h are handled by the 82443BX and are not forwarded to PCI. 0 = Disable (default). All CPU cycles to IO address 0022h are passed on to the PCI bus.
5	<b>Suspend Refresh Type (SRT).</b> This bit determines what type of EDO DRAM refresh is used during Power On Suspend (POS/STR) or Suspend to RAM modes. SRT has no effect on SDRAM refresh. 1 = Self refresh mode 0 = CBR fresh mode NOTE: When PCIRST# assertion occurs during POS/STR, this bit is not reset to '0'.
4	<b>Normal Refresh Enable (NREF_EN).</b> This bit is used to enable normal refresh operation following a POS/STR state. After coming out of reset the software must set this bit before doing an access to memory. 1 = Enable 0 = Disable
3	<b>Quick Start Mode (QSTART) (RO).</b> 1 = Quick start mode of operation is enabled for the processor. This mode is entered using a strapping option that is sampled by the 82443BX and the CPU during reset. This register bit is Read Only and a configuration write to it is ignored.
2	<b>Gated Clock Enable (GCLKEN).</b> GCLKEN enables internal dynamic clock gating in the 82443BX when a AGPset "IDLE" state occurs. This happens when the 82443BX detects an idle state on all its buses. 1 = Enable 0 = Disable
1	<b>AGP Disable (AGP_DIS).</b> This register bit is Read Only and a configuration write to it is ignored. 1 = Disable. The AGP interface and the clocks of AGP associated logic are permanently disabled. This mode is entered using a strapping option that is sampled by the 82443BX during reset. 0 = Enable
0	<b>CPU reset without PCIRST enable (CRst_En).</b> This bit enables the 82443BX to assert CPU reset without an incoming PCIRST#. This option allows the reset of the processor when the system is coming out of POS state. Defaults to '0' upon PCIRST# assertion. 1 = Enable 0 = Disable NOTE: When PCIRST# assertion occurs during POS/STR, this bit is not reset to '0'.

### 3.3.27 SCRR—Suspend CBR Refresh Rate Register (Device 0)

Address Offset: 7Bh–7Ch  
 Default Value: 0038h  
 Access: Read/Write  
 Size: 16 Bits

Bit	Description
15:13	Reserved.
12	<p><b>Suspend CBR refresh Rate Auto Adjust Enable (SRRAEN).</b> SRRAEN bit is cleared to its default during cold reset only. It is not affected by PCIRST# during resume from suspend.</p> <p>0 = Disable (default). Indicates that the suspend CBR refresh rate is not updated by the 82443BX hardware to track the system operating conditions. In this case, it is expected that BIOS will set the SRR to reflect the worst case operating conditions so that minimum refresh rate will be provided.</p> <p>1 = Enable. Indicates that the 82443BX hardware adjusts the suspend refresh rate according to system operating conditions by comparing the number of OSCCLKs in a given time. This mode allows the system to dynamically adjust the refresh rate and thus minimize suspend power consumption while guaranteeing required refresh rate.</p>
11:0	<p><b>Suspend CBR Refresh Rate (SRR).</b> The rate is loaded into the counter which counts down on OSCCLK rising edges. When it expires, a suspend CBR refresh request is triggered. This bit field may be loaded by BIOS to reflect the desirable refresh rate. In addition, the 82443BX will update it automatically, when the above SRRAEN = 1. In either case, the register is accessible for read and write operation at all times.</p> <ul style="list-style-type: none"> <li>This 12-bit field provides a dynamic range greater than the maximum CBR refresh rate that is supported of 249.6uSEC.</li> <li>SRR bit field is cleared to its default during cold reset only. It is not affected by PCIRST# during resume from suspend.</li> <li>The default value of this register is 038h, or 56 decimal. It represents a 15.5uS time between refreshes with the slowest corner OSCCLK cycle time of 270nS.</li> </ul>



### 3.3.28 EAP—Error Address Pointer Register (Device 0)

Address Offset: 80–83h  
 Default Value: 00000000h  
 Access: Read Only, Read/Write-Clear  
 Size: 32 Bits

Bit	Description
31:12	<b>Error Address Pointer (EAP) (RO).</b> This field is used to store the 4 KB block of main memory of which an error (single bit or multi-bit error) has occurred. Note that this field represents the address of the first error occurrence after bits 1:0 have been cleared by software. Once bits 1:0 are set to a value different than 00b, as a result of an error, this bit field is locked and doesn't change as a result of a new error.
11:2	Reserved.
1	<b>Multiple Bit Error (MBE) (R/WC).</b> This bit indicates that a multi-bit ECC error has occurred, and the address has been logged in bits 31:12. The EAP register is locked until the CPU clears this bit by writing a 1. Software uses bits 1:0 to detect whether the logged error address is for Single or Multi bit error, since both Single and Multiple Error bits of the Error Status register can be set. Once software completes the error processing, a value of '1' is written to this bit field to clear the value (back to 0) and unlock the error logging mechanism. Note: Any ECC errors received during initialization should be ignored.
0	<b>Single Bit Error (SBE) (R/WC).</b> 1 = Indicates that a single bit ECC error has occurred, and the address has been logged in bits 31:12. The EAP register is locked until the CPU clears this bit by writing a 1. Note: Any ECC errors received during initialization should be ignored.

### 3.3.29 ERRCMD—Error Command Register (Device 0)

Address Offset: 90h  
 Default Value: 80h  
 Access: Read/Write  
 Size: 8 bits

This 8-bit register controls the 82443BX responses to various system errors. The actual assertion of SERR# is enabled via the PCI Command register.

Bit	Description
7	<b>SERR# on AGP Non-Snoopable Access Outside of Graphics Aperture.</b> When enabled and bit 10 of ERRSTS registers transitions from 0 to 1 (during an AGP access to the address outside of the graphics aperture) then an SERR# assertion event will be generated. 1 = Enable (default). 0 = Disable.
6	<b>SERR# on Invalid AGP DRAM Access.</b> AGP non-snoopable READ accesses to locations outside the graphics aperture and outside the main DRAM range (i.e., in 640 KB – 1 MB range or above top of memory) are invalid. When this bit is set, bit 9 of the ERRSTS will be set and SERR# will be asserted, read accesses are not directed to main memory or the aperture range. 1 = Enable. 0 = Disable reporting of this condition via SERR#.
5	<b>SERR# on Access to Invalid Graphics Aperture Translation Table Entry.</b> When enabled, the 82443BX sets bit 8 of the ERRSTS and asserts SERR# following a read or write access to an invalid entry in the Graphics Aperture Translation Table residing in main memory. 1 = Enable. 0 = Disable reporting of this condition via SERR#.
4	<b>SERR# on Receiving Target Abort.</b> 1 = Enable. The 82443BX asserts SERR# on receiving a target abort on either the PCI or AGP. 0 = Disable. The 82443BX does not assert SERR# on receipt of a target abort.
3	<b>SERR# on Detected Thermal Throttling Condition.</b> 1 = Enable. The 82443BX asserts SERR# when thermal throttling condition is detected for either the read or the write function. 0 = The 82443BX does not assert SERR# for thermal throttling.
2	<b>SERR# Assertion Mode.</b> 1 = SERR# is a level mode signal. Systems that connect SERR# to EXTSMI# for error reporting should set this bit to 1. 0 = SERR# is asserted for 1 PCI clock (normal PCI mode). (default)
1	<b>SERR# on Receiving Multiple-Bit ECC/Parity Error.</b> When enabled, the 82443BX asserts SERR# when it detects a multiple-bit error reported by the DRAM controller. For systems not supporting ECC this bit must be disabled. 1 = Enable. 0 = Disable. Note: Any ECC errors received during initialization should be ignored.
0	<b>SERR# on Receiving Single-bit ECC Error.</b> When enabled, the 82443BX asserts SERR# when it detects a single-bit ECC error. For systems not supporting ECC, this bit must be disabled. 1 = Enable. 0 = Disable. Note: Any ECC errors received during initialization should be ignored.

### 3.3.30 ERRSTS—Error Status Register (Device 0)

Address Offset: 91–92h  
Default Value: 0000h  
Access: Read Only, Read/Write Clear  
Size: 16 bits

This 16-bit register is used to report error conditions via the SERR# mechanism. SERR# is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD register).

Bit	Description
15:13	Reserved.
12	<b>Read thermal Throttling Condition.</b> 1 = Read thermal throttling condition occurred. 0 = Software writes “1” to clear this bit. Default=0
11	<b>Write Thermal Throttling Condition.</b> 1 = Write thermal throttling condition occurred. 0 = Software writes “1” to clear this bit. Default=0
10	<b>AGP non-snoopable access outside of Graphics Aperture.</b> 1 = AGP access occurred to the address that is outside of the graphics aperture range. 0 = Software writes “1” to clear this bit. Default=0
9	<b>Invalid AGP non-snoopable DRAM read access (R/WC).</b> 1 = AGP non-snoopable READ access was attempted outside of the graphics aperture and outside of main memory (i.e., in 640 KB – 1 MB range or above top of memory). 0 = Software must write a “1” to clear this status bit.
8	<b>Access to Invalid Graphics Aperture Translation Table Entry (AIGATT) (R/WC).</b> 1 = An invalid translation table entry was returned in response to a graphics aperture read or write access. 0 = Software must write a “1” to clear this bit.
7:5	<b>Multi-bit First Error (MBFRE) (RO).</b> This field contains the encoded value of the DRAM row in which the first multi-bit error occurred. A simple binary encoding is used to indicate the row containing the multi-bit error. When an error is detected, this field is updated and the MEF bit is set. This field will then be locked (no further updates) until the MEF flag has been reset. If MEF is 0, the value in this field is undefined. 000 = Row 0 001 = Row 1 ... 111 = Row 7
4	<b>Multiple-bit ECC (uncorrectable) Error Flag (MEF) (R/WC).</b> 1 = Memory data transfer had an uncorrectable error(i.e., multiple-bit error). When enabled, a multiple bit error is reported by the DRAM controller and propagated to the SERR# pin, if enabled by bit 1 in the ERRCMD register. 0 = BIOS writes a 1 to clear this bit and unlock the MBFRE field. (Default = 0).
3:1	<b>Single-bit First Row Error (SBFRE) (RO).</b> This field contains the encoded value of the DRAM row in which the first single-bit error occurred. A simple binary encoding is used to indicate the row containing the single-bit error. When an error is detected, this field is updated and SEF is set. This field is then locked (no further updates) until the SEF flag has been reset. If SEF is 0, the value in this field is undefined. 000 = Row 0 001 = Row 1 ... 111 = Row 7
0	<b>Single-bit (correctable) ECC Error Flag (SEF) (R/WC).</b> 1 = Memory data transfer had a single-bit correctable error and the corrected data was sent for the access. When ECC is enabled, a single bit error is reported and propagated to the SERR# pin, if enabled by bit 0 in the ERRCMD register. 0 = BIOS writes a 1 to clear this bit and unlock the SBFRE field.



### 3.3.31 ACAPID—AGP Capability Identifier Register (Device 0)

Address Offset: A0–A3h  
 Default Value: 00100002h/00000000h  
 Access: Read Only  
 Size: 32 bits

This register provides normal identifier for AGP capability.

Bit	Description
31:24	Reserved
23:20	<b>Major AGP Revision Number.</b> This field provides a major revision number of AGP specification to which this version of the 82443BX conforms. When the AGP DIS bit (PMCR[1]) is set to 0, this number is set to value of "0001b" (i.e., implying Rev 1.x). When the AGP DIS bit (PMCR[1]) is set to 1, This number is set to "0000b".
19:16	<b>Minor AGP Revision Number.</b> These bits provide a minor revision number of AGP specification to which this version of 82443BX conforms. This number is hardwired to value of "0000" (i.e., implying Rev x.0). Together with major revision number this field identifies 82443BX as an AGP REV 1.0 compliant device.
15:8	<b>Next Capability Pointer.</b> AGP capability is the first and the last capability described via the capability pointer mechanism. 0s = Hardwired to 0s to indicate the end of the capability linked list.
7:0	<b>AGP Capability ID.</b> This field identifies the linked list item as containing AGP registers. When the AGP DIS bit (PMCR[1]) is set to 0, this field has a value of 0000_0010b assigned by the PCI SIG. When the AGP DIS bit (PMCR[1]) is set to 1, this field has a value of 00h.

### 3.3.32 AGPSTAT—AGP Status Register (Device 0)

Address Offset: A4–A7h  
 Default Value: 1F000203h  
 Access: Read Only  
 Size: 32 bits

This register reports AGP compliant device capability/status.

Bit	Description
31:24	<b>AGP Maximum Request Queue Depth (RO).</b> This field is hardwired to 1Fh to indicate a maximum of 32 outstanding AGP command requests can be handled by the 82443BX.
23:10	Reserved
9	<b>AGP Side Band Addressing Supported.</b> This bit indicates that the 82443BX supports side band addressing. It is hardwired to 1.
8:2	Reserved
1:0	<b>AGP Data Transfer Type Supported (R/W).</b> Bit 0 identifies if AGP compliant device supports 1x data transfer mode and bit 1 identifies if AGP compliant device supports 2x data transfer mode. Configuration software will update this field by setting only one bit that corresponds to the capability of AGP master (after that capability has been verified by accessing the same functional register within the AGP masters configuration space). 00 = Not allowed 01 = 1x data transfer mode supported 10 = 2x data transfer mode supported 11 = (default) NOTE: The selected data transfer mode apply to both AD bus and SBA bus.

### 3.3.33 AGPCMD—AGP Command Register (Device 0)

Address Offset: A8–ABh  
 Default Value: 00000000h  
 Access: Read/Write  
 Size: 32 bits

This register provides control of the AGP operational parameters.

Bit	Description
31:10	Reserved.
9	<b>AGP Side Band Enable.</b> This bit enables the side band addressing mechanism. 1 = Enable. 0 = Disable.
8	<b>AGP Enable.</b> When disabled, the 82443BX ignores all AGP operations, including the sync cycle. Any AGP operations received while this bit is set to 1 is serviced even if this bit is reset to 0. If this bit transitions from a 1 to a 0 on a clock edge in the middle of an SBA command being delivered in 1X mode the command will be issued. When this bit is set to 1 the 82443BX will respond to AGP operations delivered via PIPE#, or to operations delivered via SBA if the AGP Side Band Enable bit is also set to 1. The AGP parameters in the AGPCMD and AGPCTRL registers must be set prior to setting this bit '1'. With the exception of the GTLB_ENABLE (bit 7, AGPCTRL), and ATTBASE register (offset B8h), which can be modified dynamically. 1 = Enable. 0 = Disable.
7:2	Reserved.
1:0	<b>AGP Data Transfer Rate.</b> One (and only one) bit in this field must be set to indicate the desired data transfer rate (Bit 0 for 1X, Bit 1 for 2X). The same bit must be set on both master and target. Configuration software will update this field by setting only one bit that corresponds to the capability of AGP master (after that capability has been verified by accessing the same functional register within the AGP masters configuration space.) 00 = default 01 = 1x data transfer rate. 10 = 2x data transfer rate. 11 = Illegal NOTE: This field applies to AD and SBA buses.

### 3.3.34 AGPCTRL—AGP Control Register (Device 0)

Address Offset: B0–B3h  
 Default Value: 00000000h  
 Access: Read/Write  
 Size: 32 bits

This register provides for additional control of the AGP interface.

Bit	Description															
31:16	Reserved.															
15	<p><b>Snoopable Writes In Order With AGP Reads Disable (AGPDCD).</b> When set to 0 (default), the 82443BX maintains ordering between snoopable write cycles and AGP reads. When set to 1, the 82443BX handles the AGP reads and snoopable writes as independent streams.</p> <table><tr><th>AGPDCD (Bit 15)</th><th>AGPRSE (Bit 13)</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>DWB is visible to AGP reads. DWB flushes only when address hit.</td></tr><tr><td>0</td><td>1</td><td>Illegal.</td></tr><tr><td>1</td><td>0</td><td>Illegal</td></tr><tr><td>1</td><td>1</td><td>DWB flushes when write to AGP occurs</td></tr></table>	AGPDCD (Bit 15)	AGPRSE (Bit 13)	Description	0	0	DWB is visible to AGP reads. DWB flushes only when address hit.	0	1	Illegal.	1	0	Illegal	1	1	DWB flushes when write to AGP occurs
AGPDCD (Bit 15)	AGPRSE (Bit 13)	Description														
0	0	DWB is visible to AGP reads. DWB flushes only when address hit.														
0	1	Illegal.														
1	0	Illegal														
1	1	DWB flushes when write to AGP occurs														
14	Reserved															
13	<p><b>Graphics Aperture Write-AGP Read Synchronization Enable (AGPRSE).</b> When this bit is set the 82443BX will ensure that all writes posted in the Global Write Buffer to the Graphics Aperture are retired to DRAM before the 82443BX will initiate any CPU-to-AGP cycle. This can be used to ensure synchronization between the CPU and AGP master. The AGPDCD bit description defines the interaction between the AGPRSE bit and the AGPDCD bit.</p> <p>1 = Enable 0 = Disable (Default)</p>															
12:8	Reserved															
7	<p><b>GTLB Enable (and GTLB Flush Control).</b></p> <p>1 = Enable. Normal operations of the Graphics Translation Lookaside Buffer. 0 = Disable (default). The GTLB is flushed by clearing the valid bits associated with each entry.</p>															
6:0	Reserved.															



### 3.3.35 APSIZE—Aperture Size Register (Device 0)

Address Offset: B4h  
Default Value: 00h  
Access: Read/Write  
Size: 8 bits

This register determines the effective size of the Graphics Aperture used for a particular 82443BX configuration. This register can be updated by the 82443BX-specific BIOS configuration sequence before the PCI normal bus enumeration sequence takes place. If the register is not updated, a default value selects an aperture of maximum size (i.e., 256 MB). The size of the table that will correspond to a 256 MB aperture is not practical for most applications and, therefore, these bits must be programmed to a smaller practical value that forces adequate address range to be requested via the APBASE register from the PCI configuration software.

Bit	Description
7:6	Reserved.
5:0	<p><b>Graphics Aperture Size (APSIZE) (R/W).</b> Each bit in APSIZE[5:0] operates on similarly ordered bits in APBASE[27:22] of the Aperture Base configuration register. When a particular bit of this field is "0", it forces the similarly ordered bit in APBASE[27:22] to behave as "hardwired" to 0. When a particular bit of this field is set to "1", it allows corresponding bit of the APBASE[27:22] to be read/write accessible. Only the following combinations are allowed:</p> <p>11 1111 = 4 MB  11 1110 = 8 MB  11 1100 = 16 MB  11 1000 = 32 MB  11 0000 = 64 MB  10 0000 = 128 MB  00 0000 = 256MB</p> <p>Default for APSIZE[5:0]=000000b forces default APBASE[27:22] =000000b (i.e., all bits respond as "hardwired" to 0). This provides maximum aperture size of 256 MB. As another example, programming APSIZE[5:0]=111000b hardwires APBASE[24:22]=000b and while enabling APBASE[27:25] as read/write programmable.</p>

### 3.3.36 ATTBASE—Aperture Translation Table Base Register (Device 0)

Address Offset: B8-BBh  
Default Value: 00000000h  
Access: Read/Write  
Size: 32 bits

This register provides the starting address of the Graphics Aperture Translation Table base located in the main DRAM. The ATTBASE register may be dynamically changed.

**Note:** The address provided via ATTBASE is 4KB aligned.

Bit	Description
31:12	<b>Aperture Translation Table Base Address.</b> Bits 31:12 correspond to address bits 31:12, respectively. This field contains a pointer to the base of the translation table used to map memory space addresses in the aperture range to addresses in main memory.
11:0	Reserved.

### 3.3.37 MBFS—Memory Buffer Frequency Select Register (Device 0)

Address Offset: CA–CCh  
 Default Value: 000000h  
 Access: Read/Write  
 Size: 24 bits

The settings in this register enable the 100 MHz or 66 MHz buffers for each of the following signal groups.

**Note:** The choice of 100 MHz or 66 MHz buffer is independent of bus frequency. It is possible to select a 100 MHz memory buffer even though the bus frequency is 66 MHz (and vice versa).

Bit	Description
23	Reserved
22	<b>MAA[13:0], WEA#, SRASA#, SCASA# (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for MAA[13:0], WEA#, SRASA#, SCASA#. 0 = 66 MHz 1 = 100 MHz
21	<b>MAB[12:11, 9:0]# &amp; MAB[13,10], WEB#, SRASB#, SCASB# (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for MAB[12:11, 9:0]# & MAB[13,10], WEB#, SRASB#, SCASB#. Note that the address's MABx# are inverted copies of MAA, with the exception of MAB[13,10]. 0 = 66 MHz 1 = 100 MHz
20	<b>MD [63:0] (100 MHz/66 MHz buffer select bit [Control 2]).</b> This bit enables either 100 MHz or 66 MHz buffers for MD [63:0] [Control 2]. (Refer to the corresponding MBSC register for programming details). 0 = 66 MHz 1 = 100 MHz
19	<b>MD [63:0] (100 MHz/66 MHz buffer select bit [Control 1]).</b> This bit enables either 100 MHz or 66 MHz buffers for MD [63:0] [Control 1]. (Refer to the corresponding MBSC register for programming details). 0 = 66 MHz 1 = 100 MHz
18	<b>MECC [7:0] (100 MHz/66 MHz buffer select bit [Control 2]).</b> This bit enables either 100 MHz or 66 MHz buffers for MECC [7:0] [Control 2]. (Refer to the corresponding MBSC register for programming details). 0 = 66 MHz 1 = 100 MHz
17	<b>MECC [7:0] (100 MHz/66 MHz buffer select bit [Control 1]).</b> This bit enables either 100 MHz or 66 MHz buffers for MECC [7:0] [Control 1]. (Refer to the corresponding MBSC register for programming details). 0 = 66 MHz 1 = 100 MHz
16	<b>CSB7#/CKE5 (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for CSB7#/CKE5. 0 = 66 MHz 1 = 100 MHz

Bit	Description
15	<b>CSA7#/CKE3 (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for CSA7#/CKE3. 0 = 66 MHz 1 = 100 MHz
14	<b>CSB6#/CKE4 (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for CSB6#/CKE4. 0 = 66 MHz 1 = 100 MHz
13	<b>CSA6#/CKE2 (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for CSA6#/CKE2. 0 = 66 MHz 1 = 100 MHz
12	<b>CSA5#/RASA5#, CSB5#/RASB5# (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for CSA5#/RASA5#, CSB5#/RASB5#. 0 = 66 MHz 1 = 100 MHz
11	<b>CSA4#/RASA4#, CSB4#/RASB4# (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for CSA4#/RASA4#, CSB4#/RASB4#. 0 = 66 MHz 1 = 100 MHz
10	<b>CSA3#/RASA3#, CSB3#/RASB3# (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for CSA3#/RASA3#, CSB3#/RASB3#. 0 = 66 MHz 1 = 100 MHz
9	<b>CSA2#/RASA2#, CSB2#/RASB2# (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for CSA2#/RASA2#, CSB2#/RASB2#. 0 = 66 MHz 1 = 100 MHz
8	<b>CSA1#/RASA1#, CSB1#/RASB1# (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for CSA1#/RASA1#, CSB1#/RASB1#. 0 = 66 MHz 1 = 100 MHz
7	<b>CSA0#/RASA0#, CSB0#/RASB0# (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for CSA0#/RASA0#, CSB0#/RASB0#. 0 = 66 MHz 1 = 100 MHz
6	<b>DQMA5/CASA5# (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for DQMA5/CASA5#. 0 = 66 MHz 1 = 100 MHz
5	<b>DQMA1/CASA1# (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for DQMA1/CASA1#. 0 = 66 MHz 1 = 100 MHz
4	<b>DQMB5/CASB5# (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for DQMB5/CASB5#. 0 = 66 MHz 1 = 100 MHz



Bit	Description
3	<b>DQMB1/CASB1# (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for DQMB1/CASB1#. 0 = 66 MHz 1 = 100 MHz
2	<b>DQMA[7:6,4:2,0]/CASA[7:6,4:2,0]# (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for DQMA[7:6]/CASA[7:6]#, DQMA[4:2]/CASA[4:2]#, and the DQMA[0]/CASA[0]#. 0 = 66 MHz 1 = 100 MHz
1	<b>CKE1/GCKE (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for CKE1. 0 = 66 MHz 1 = 100 MHz
0	<b>CKE0/FENA (100 MHz/66 MHz buffer select bit).</b> This bit enables either 100 MHz or 66 MHz buffers for CKE0/FENA. 0 = 66 MHz 1 = 100 MHz

### 3.3.38 BSPAD—BIOS Scratch Pad Register (Device 0)

Address Offset: D0–D7h  
 Default Value: 0000-0000-0000-0000h  
 Access: Read/Write  
 Size: 64 bits

This register provides 8 bytes general purpose read/write registers for the BIOS to perform the configuration routine. The 82443BX will provide this 8 byte register in the PCI configuration space of the 82443BX device0 on bus 0. The registers in this range will be defined as read/write and will be initialized to all 0's after PCIRST#. The BIOS will can access these registers through the normal PCI configuration register mechanism, accessing 1,2 or 4 bytes in every data access.

Bit	Description
64:0	<b>BIOS Work Space.</b>

### 3.3.39 DWTC—DRAM Write Thermal Throttling Control Register (Device 0)

Offset: E0h–E7h  
Default: 0000\_0000\_0000\_0000h  
Access: Read/Write/Lock  
Size: 64 bits

A locking mechanism is included to protect contents of this register as well as the DRAM Read Thermal Throttling Control register described below.

Bits	Description
63	<b>Throttle Lock (TLOCK).</b> This bit secures the DRAM thermal throttling control registers. 1 = All configuration register bits in E0h–E7h and E8h–EFh (read throttle control) become read-only. 0 = Default
62:46	Reserved
45:38	<b>Global DRAM Write Sampling Window (GDWSW).</b> This 8-bit value is multiplied by 4 to define the length of time in milliseconds (0–1020) over which the number of QWords written is counted.
37:26	<b>Global QWord Threshold (GQT).</b> The 12-bit value held in this field is multiplied by 215 to arrive at the number of QWords that must be written within the Global DRAM Write Sampling Window in order to cause the thermal throttling mechanism to be invoked.
25:20	<b>Throttle Time (TT).</b> This value provides a multiplier between 0 and 63 which specifies how long thermal throttling remains in effect as a number of Global DRAM Write Sampling Windows. For example, if GDWSW is programmed to 1000_0000b and TT is set to 01_0000b, then thermal throttling will be performed for ~2 seconds once invoked (128 ms * 16).
19:13	<b>Throttle Monitoring Window (TMW).</b> The value in this register is padded with four 0's to specify a window of 0–2047 DRAM CLKs with 16 clock granularity. While the thermal throttling mechanism is invoked, DRAM writes are monitored during this window—if the number of QWords written during the window reaches the Throttle QWord Maximum, then write requests are blocked for the remainder of the window.
12:3	<b>Throttle QWord Maximum (TQM).</b> The Throttle QWord Maximum defines the maximum number of QWords between 0–1023 which are permitted to be written to DRAM within one Throttle Monitoring Window while the thermal throttling mechanism is in effect.
2:0	<b>DRAM Write Throttle Mode.</b> Normal DRAM write monitoring and thermal throttling operation are enabled when bits 2:0 are set to 100. All other combinations are Intel Reserved. 000–011 = Intel Reserved 100 = Normal Operations 101–111 = Intel Reserved

### 3.3.40 DRTC—DRAM Read Thermal Throttling Control Register (Device 0)

Offset: E8h–EFh  
 Default: 0000\_0000\_0000\_0000h  
 Access: Read/Write/Lock  
 Size: 64 Bits

The contents of this register are protected by making the bits read-only once a '1' is written to the Throttle Lock bit (bit 63 of configuration register E0–E7h)

Bits	Description
63:46	Reserved
45:38	<b>Global DRAM Read Sampling Window (GDRSW).</b> This 8-bit value is multiplied by 4 to define the length of time in milliseconds (0–1020) over which the number of QWords read from DRAM is counted.
37:26	<b>Global Read QWord Threshold (GRQT).</b> The 12-bit value held in this field is multiplied by 215 to arrive at the number of QWords that must be written within the Global DRAM Read Sampling Window in order to cause the thermal throttling mechanism to be invoked.
25:20	<b>Read Throttle Time (RTT).</b> This value provides a multiplier between 0 and 63 which specifies how long read thermal throttling remains in effect as a number of Global DRAM Read Sampling Windows. For example, if GDRSW is programmed to 1000_0000b and RTT is set to 01_0000b, then read thermal throttling will be performed for ~2 seconds once invoked (128 ms * 16).
19:13	<b>Read Throttle Monitoring Window (RTMW).</b> The value in this register is padded with 4 0's to specify a window of 0–2047 DRAM CLKs with 16 clock granularity. While the thermal throttling mechanism is invoked, DRAM reads are monitored during this window—if the number of QWords read during the window reaches the Throttle QWord Maximum, then Host and PCI read requests, as well as all AGP requests, are blocked for the remainder of the window.
12:3	<b>Read Throttle QWord Maximum (RTQM).</b> The Read Throttle QWord Maximum defines the maximum number of QWords between 0–1023 which are permitted to be read from DRAM within one Read Throttle Monitoring Window while thermal throttling mechanism is in effect.
2:0	<b>DRAM Read Throttle Mode.</b> Normal DRAM read monitoring and thermal throttling operation are enabled when bits 2:0 are set to 100. All other combinations are Intel Reserved. 000–011 = Intel Reserved 100 = Normal Operations 101–111 = Intel Reserved



### 3.3.41 BUFFC—Buffer Control Register (Device 0)

Offset: F0–F1h  
Default: 0000h  
Access: Read/Write  
Size: 16 bits

The Jam Latch design provides the AGP sub-system with a variable strength, to better accommodate the clamping requirements.

The Jam Latch Register should be enabled by the BIOS during the resume sequence from STR, if these Jam Latch control bits had been enabled before the STR was executed.

Bit	Description
15:10	Reserved.
9:6	<b>AGP Jam Latch Strength Select.</b> Bit 9 = 1; Enable strong pull-up Bit 8 = 1; Enable weak pull-up Bit 7 = 1; Enable strong pull-down Bit 6 = 1; Enable weak pull-down
5:0	Intel Reserved.

### 3.4 PCI-to-PCI Bridge Registers (Device 1)

The configuration space for device #1 is controlled by the AGP\_DIS bit in the PMCR register.

**Note:** When AGP\_DIS = 0, the configuration space for device #1 is enabled, and the registers defined below are accessible through the configuration mechanism defined in the first section of this document.

**Note:** When the AGP\_DIS = 1, the configuration space for device #1 is disabled. All configuration cycles (reads and writes) to device #1 of bus 0 will cause the master abort status bit for device #0/ bus 0 to be set. Configuration read cycles will return data of all 1's. Configuration write cycles will have no effect on the registers.

**Table 3-4. 82443BX Configuration Space—Device 1**

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID1	Vendor Identification	8086h	RO
02–03h	DID1	Device Identification	7191h	RO
04–05h	PCICMD1	PCI Command Register	0000h	R/W
06–07h	PCISTS1	PCI Status Register	0220h	RO, R/WC
08h	RID1	Revision Identification	00/01h	RO
09h	—	Reserved	00h	—
0Ah	SUBC1	Sub-Class Code	04h	RO
0Bh	BCC1	Base Class Code	06h	RO
0Ch	—	Reserved	00h	—
0Dh	MLT1	Master Latency Timer	00h	R/W
0Eh	HDR1	Header Type	01h	RO
0F–17h	—	Reserved	00h	—
18h	PBUSN	Primary Bus Number	00h	RO
19h	SBUSN	Secondary Bus Number	00h	R/W
1Ah	SUBUSN	Subordinate Bus Number	00h	R/W
1Bh	SMLT	Secondary Bus Master Latency Timer	00h	R/W
1Ch	IOBASE	I/O Base Address Register	F0h	R/W
1Dh	IOLIMIT	I/O Limit Address Register	00h	R/W
1E–1Fh	SSTS	Secondary PCI-to-PCI Status Register	02A0h	R/WC, RO
20–21h	MBASE	Memory Base Address Register	FFF0h	R/W
22–23h	MLIMIT	Memory Limit Address Register	0000h	R/W
24–25h	PMBASE	Prefetchable Memory Base Address Reg.	FFF0h	R/W
26–27h	PMLIMIT	Prefetchable Memory Limit Address Reg.	0000h	R/W
28–3Dh	—	Reserved	0	c
3Eh	BCTRL	Bridge Control Register	80h	R/W
3F–FFh	—	Reserved	00h	—

### 3.4.1 VID1—Vendor Identification Register (Device 1)

Address Offset: 00–01h  
Default Value: 8086h  
Attribute: Read Only  
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identify any PCI device. Writes to this register have no effect.

Bit	Description
15:0	<b>Vendor Identification Number.</b> This is a 16-bit value assigned to Intel. Intel VID = 8086h.

### 3.4.2 DID1—Device Identification Register (Device 1)

Address Offset: 02–03h  
Default Value: 7191h  
Attribute: Read Only  
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	<b>Device Identification Number.</b> This is a 16 bit value assigned to the 82443BX device #1. 82443BX device #1 DID =7191h.



### 3.4.3 PCICMD1—PCI-to-PCI Command Register (Device 1)

Address Offset: 04–05h  
 Default: 0000h  
 Access: Read/Write  
 Size: 16 bits

Bit	Descriptions
15:10	Reserved.
9	<b>Fast Back-to-Back:</b> Not Applicable. Hardwired to 0.
8	<b>SERR# Enable (SERRE1).</b> When enabled the SERR# signal driver (common for PCI and AGP) is enabled for error conditions that occur on AGP. If both SERRE and SERRE1 are reset to 0, then SERR# is never driven by the 82443BX. Also, if this bit is set and the Parity Error Response Enable Bit (Dev 01h, Register 3Eh, Bit 0) is set, then the 82443BX will report ADDRESS and DATA parity errors on AGP. 1 = Enable. 0 = Disable.
7	<b>Address/Data Stepping.</b> Not applicable. Hardwired to 0.
6	<b>Parity Error Enable (PERRE1).</b> Hardwired to 0.
5	Reserved.
4	<b>Memory Write and Invalidate Enable: Not applicable.</b> However, supported as a read/write bit to avoid the problems with normal PCI-to-PCI Bridge configuration software.
3	<b>Special Cycle Enable: Not applicable.</b> However, supported as a read/write bit to avoid the problems with normal PCI-to-PCI Bridge configuration software.
2	<b>Bus Master Enable (BME1): Not applicable.</b> However, supported as a read/write bit to avoid the problems with normal PCI-to-PCI Bridge configuration software.
1	<b>Memory Access Enable (MAE1): Not applicable.</b> However, supported as a read/write bit to avoid the problems with normal PCI-to-PCI Bridge configuration software.
0	<b>I/O Access Enable (IOAE1): Not applicable.</b> However, supported as a read/write bit to avoid the problems with normal PCI-to-PCI Bridge configuration software.

### 3.4.4 PCISTS1—PCI-to-PCI Status Register (Device 1)

Address Offset: 06–07h  
Default Value: 0220h  
Access: Read Only, Read/Write Clear  
Size: 16 bits

PCISTS1 is a 16-bit status register that reports the occurrence of error conditions associated with primary side of the “virtual” PCI-to-PCI bridge embedded within the 82443BX.

Bit	Descriptions
15	<b>Detected Parity Error (DPE1).</b> Not Applicable. Hardwired to 0.
14	Reserved.
13	<b>Received Master Abort Status (RMAS1).</b> Not Applicable. Hardwired to 0.
12	<b>Received Target Abort Status (RTAS1).</b> Not Applicable. Hardwired to 0.
11	<b>Signaled Target Abort Status (STAS1).</b> Not Applicable. Hardwired to 0.
10:9	<b>DEVSEL# Timing (DEVT1).</b> Not Applicable. Hardwired to “01b”.
8	<b>Data Parity Detected (DPD1).</b> Not Applicable. Hardwired to 0.
7	<b>Fast Back-to-Back (FB2B1).</b> Not Applicable. Hardwired to 0.
6	Reserved.
5	<b>66/60 MHz Capability.</b> Hardwired to “1”.
4:0	Reserved.

### 3.4.5 RID1—Revision Identification Register (Device 1)

Address Offset: 08h  
Default Value: 00/01h  
Access: Read Only  
Size: 8 bits

This register contains the revision number of the 82443BX device #1. These bits are read only and writes to this register have no effect. For the A-0 Stepping, this value is 00h.

Bit	Description
7:0	<b>Revision Identification Number.</b> This is an 8-bit value that indicates the revision identification number for the 82443BX device #1. 02h = B1 stepping

### 3.4.6 SUBC1—Sub-Class Code Register (Device 1)

Address Offset: 0Ah  
 Default Value: 04h  
 Access: Read Only  
 Size: 8 bits

This register contains the Sub-Class Code for the 82443BX device #1. This code is 04h indicating a PCI-to-PCI Bridge device. The register is read only.

Bit	Description
7:0	<b>Sub-Class Code (SUBC1).</b> This is an 8-bit value that indicates the category of Bridge into which the 82443BX falls. 04h = Host Bridge.

### 3.4.7 BCC1—Base Class Code Register (Device 1)

Address Offset: 0Bh  
 Default Value: 06h  
 Access: Read Only  
 Size: 8 bits

This register contains the Base Class Code of the 82443BX device #1. This code is 06h indicating a Bridge device. This register is read only.

Bit	Description
7:0	<b>Base Class Code (BASCC).</b> This is an 8-bit value that indicates the Base Class Code for the 82443BX device #1. 06h = Bridge device.

### 3.4.8 MLT1—Master Latency Timer Register (Device 1)

Address Offset: 0Dh  
 Default Value: 00h  
 Access: Read/Write  
 Size: 8 bits

This functionality is not applicable. It is described here since these bits should be implemented as a read/write to comply with the normal PCI-to-PCI bridge configuration software.

Bit	Description
7:3	<b>Not applicable but support read/write operations.</b> (Reads return previously written data.)
2:0	Reserved.



### 3.4.9 HDR1—Header Type Register (Device 1)

Offset: 0Eh  
 Default: 01h  
 Access: Read Only  
 Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	<b>Header Type (HEADT).</b> This read only field always returns 01h when read. Writes have no effect.

### 3.4.10 PBUSN—Primary Bus Number Register (Device 1)

Offset: 18h  
 Default: 00h  
 Access: Read Only  
 Size: 8 bits

This register identifies that “virtual” PCI-to-PCI bridge is connected to bus #0.

Bit	Descriptions
7:0	<b>Bus Number.</b> Hardwired to “0”.

### 3.4.11 SBUSN—Secondary Bus Number Register (Device 1)

Offset: 19h  
 Default: 00h  
 Access: Read /Write  
 Size: 8 bits

This register identifies the bus number assigned to the second bus side of the “virtual” PCI-to-PCI bridge i.e. to AGP. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to AGP.

Bit	Descriptions
7:0	<b>Bus Number.</b> Programmable Default “0”.

### 3.4.12 SUBUSN—Subordinate Bus Number Register (Device 1)

Offset: 1Ah  
 Default: 00h  
 Access: Read /Write  
 Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below AGP. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to AGP.

Bit	Descriptions
7:0	<b>Bus Number.</b> Programmable.

### 3.4.13 SMLT—Secondary Master Latency Timer Register (Device 1)

Address Offset: 1Bh  
 Default Value: 00h  
 Access: Read/Write  
 Size: 8 bits

This register control the bus tenure of the 82443BX on AGP the same way the Device 0 MLT controls the access to the PCI bus.

Bit	Description
7:3	<b>Secondary MLT Counter Value.</b> The default is 0s (i.e., SMLT disabled)
2:0	Reserved.

### 3.4.14 IOBASE—I/O Base Address Register (Device 1)

Address Offset: 1Ch  
 Default Value: F0h  
 Access: Read/Write  
 Size: 8 bits

This register control the CPU to AGP I/O access routing based on the following formula:

$$\text{IO\_BASE} = \text{address} \ll \text{IO\_LIMIT}$$

Bit	Description
7:4	<b>I/O Address Base.</b> Corresponds to A[15:12] of the I/O address. Default = Fh
3:0	Reserved.

### 3.4.15 IOLIMIT—I/O Limit Address Register (Device 1)

Address Offset: 1Dh  
 Default Value: 00h  
 Access: Read/Write  
 Size: 8 bits

This register controls the CPU to AGP I/O access routing based on the following formula:

$$\text{IO\_BASE} \leq \text{address} \leq \text{IO\_LIMIT}$$

Bit	Description
7:4	<b>I/O Address Limit.</b> Corresponds to A[15:12] of the I/O address. Default=0
3:0	<b>Reserved.</b> (Only 16 bit addressing supported.)



### 3.4.16 SSTS—Secondary PCI-to-PCI Status Register (Device 1)

Address Offset: 1E–1Fh  
 Default Value: 02A0h  
 Access: Read Only, Read/Write Clear  
 Size: 16 bits

SSTS is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e. AGP side) of the “virtual” PCI-to-PCI bridge embedded within 82443BX.

Bit	Descriptions
15	<b>Detected Parity Error (DPE1).</b> Note that the PERRE1 bit does not affect the function of this bit. Also the PERR# is not implemented in the 82443BX. 1 = 82443BX detected of a parity error in the address or data phase of AGP bus transactions. 0 = Software sets DPE1 to 0 by writing a 1 to this bit.
14	<b>Received System Error (SSE1).</b> 1 = 82443BX asserted SERR# for any enabled error condition under device 1. Device 1 error conditions are enabled in the SSTS and BCTRL registers. 0 = Software clears SSE1 to 0 by writing a 1 to this bit.
13	<b>Received Master Abort Status (RMAS1).</b> 1 = 82443BX terminates a Host-to-AGP with an unexpected master abort. 0 = Software resets this bit to 0 by writing a 1 to it.
12	<b>Received Target Abort Status (RTAS1).</b> 1 = 82443BX-initiated transaction on AGP is terminated with a target abort. 0 = Software resets RTAS1 to 0 by writing a 1 to it.
11	<b>Signaled Target Abort Status (STAS1).</b> STAS1 is hardwired to a 0, since the 82443BX does not generate target abort on AGP.
10:9	<b>DEVSEL# Timing (DEVT1).</b> This 2-bit field indicates the timing of the DEVSEL# signal when the 82443BX responds as a target on AGP, and is hard-wired to the value 01b (medium) to indicate the time when a valid DEVSEL# can be sampled by the initiator of the PCI cycle. 01 = Medium. (hardwired)
8	<b>Data Parity Detected (DPD1).</b> Hardwired to 0. 82443BX does not implement G_PERR# function. However, data parity errors are still detected and reported on SERR# (if enabled by SERRE, SERRE1 and the BCTRL register, bit 0).
7	<b>Fast Back-to-Back (FB2B1).</b> This bit is hardwired to 1. The 82443BX as a target supports fast back-to-back transactions on AGP.
6	Reserved.
5	<b>66/60MHZ Capability.</b> Hardwired to 1.
4:0	Reserved.

### 3.4.17 MBASE—Memory Base Address Register (Device 1)

Address Offset: 20–21h  
 Default Value: FFF0h  
 Access: Read/Write  
 Size: 16 bits

This register controls the CPU to AGP non-prefetchable memory access routing based on the following formula:

$$\text{MEMORY\_BASE} = \text{address} = \text{MEMORY\_LIMIT}$$

This register must be initialized by the configuration software.

Bit	Description
15: 4	<b>Memory Address Base (MEM_BASE)</b> . Corresponds to A[31:20] of the memory address. Default=FFF0h
3:0	Reserved.

### 3.4.18 MLIMIT—Memory Limit Address Register (Device 1)

Address Offset: 22–23h  
 Default Value: 0000h  
 Access: Read/Write  
 Size: 16 bits

This register controls the CPU to AGP non-prefetchable memory access routing based on the following formula:

$$\text{MEMORY\_BASE} = \text{address} = \text{MEMORY\_LIMIT}$$

This register must be initialized by the configuration software.

**Note:** Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable AGP address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved CPU-AGP memory access performance.

**Note:** The configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges i.e. prevent overlap with each other and/or with the ranges covered with the main memory. There is no provision in the 82443BX hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

Bit	Description
15: 4	<b>Memory Address Limit (MEM_LIMIT)</b> . Corresponds to A[31:20] of the memory address. Default=0
3:0	Reserved.

### 3.4.19 PMBASE—Prefetchable Memory Base Address Register (Device 1)

Address Offset: 24–25h  
 Default Value: FFF0h  
 Access: Read/Write  
 Size: 16 bits

This register controls the CPU to AGP prefetchable memory accesses routing based on the following formula:

$$\text{PREFETCHABLE\_MEMORY\_BASE} = \text{address} = \text{PREFETCHABLE\_MEMORY\_LIMIT}$$

This register must be initialized by the configuration software.

Bit	Description
15: 4	<b>Prefetchable Memory Address Base (PMEM_BASE).</b> Corresponds to A[31:20] of the memory address. Default=FFF0h
3:0	Reserved.

### 3.4.20 PMLIMIT—Prefetchable Memory Limit Address Register (Device 1)

Address Offset: 26–27h  
 Default Value: 0000h  
 Access: Read/Write  
 Size: 16 bits

This register controls the CPU to AGP prefetchable memory accesses routing based on the following formula:

$$\text{PREFETCHABLE\_MEMORY\_BASE} = \text{address} = \text{PREFETCHABLE\_MEMORY\_LIMIT}$$

This register must be initialized by the configuration software.

**Note:** The prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as Uncachable and the ones that can be designated as a USWC (i.e. prefetchable) from the CPU perspective.

Bit	Description
15: 4	<b>Prefetchable Memory Address Limit (PMEM_LIMIT).</b> Corresponds to A[31:20] of the memory address. Default=0
3:0	Reserved.



### 3.4.21 BCTRL—PCI-to-PCI Bridge Control Register (Device 1)

Address Offset: 3Eh  
Default: 80h  
Access: Read/Write  
Size: 8 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-to-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., AGP) as well as some bits that affect the overall behavior of the “virtual” PCI-to-PCI bridge in the 82443BX (e.g., VGA compatible address ranges mapping).

Bit	Descriptions
7	<b>Fast Back to Back Enable.</b> 82443BX supports fast back-to-back cycles on AGP, and therefore this bit is hardwired to 1.
6	<b>Secondary Bus Reset:</b> 82443BX does not support generation of reset via this bit on the AGP and therefore this bit is hardwired to 0. NOTE: The only way to perform a hard reset of the AGP is via the system reset either initiated by software or hardware via PIIX4E.
5	<b>Master Abort Mode.</b> Not applicable. Hardwired to 0. (This means when acting as a master on AGP the 82443BX will drop writes on the “floor” and return all 1s during reads.)
4	Reserved.
3	<b>VGA Enable.</b> Controls the routing of CPU-initiated transactions targeting VGA compatible I/O and memory address ranges. 1 = 82443BX will forward the following CPU accesses to AGP: <ul style="list-style-type: none"> <li>memory accesses in the range 0A0000h to 0BFFFFh</li> <li>I/O addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases - A[15:10] are not decoded)</li> </ul> When this bit is set, forwarding of these accesses issued by the CPU is independent of the I/O address and memory address ranges defined by the previously defined base and limit registers. Forwarding of these accesses is also independent of the settings of bit 2 (ISA Enable) of this register or of bit 5 (VGA Palette Snoop Enable) of the PCICMD1 register if this bit is 1. 0 = VGA compatible memory and I/O range accesses are mapped to PCI unless they are redirected to AGP via I/O and memory range registers defined above (IOBASE, IOLIMIT, MBASE, MLIMIT, PMBASE, PMLIMIT). (default)
2	<b>ISA Enable.</b> Modifies the response by the 82443BX to an I/O access issued by the CPU that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 1 = When this bit is set to 1 82443BX will not forward to AGP any I/O transactions addressing the last 768 bytes in each 1KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead going to AGP these cycles will be forwarded to PCI where they can be subtractively or positively claimed by the ISA bridge. 0 = All addresses defined by the IOBASE and IOLIMIT for CPU I/O transactions will be mapped to AGP. (default)
1	Reserved.
0	<b>Parity Error Response Enable.</b> Controls 82443BX's response to data phase parity errors on AGP. G_PERR# is not implemented by the 82443BX. However, when this bit is set to 1, address and data parity errors on AGP are reported via SERR# mechanism, if enabled by SERRE1 and SERRE. If this bit is reset to 0, then address and data parity errors on AGP are not reported via the 82443BX SERR# signal. Other types of error conditions can still be signaled via SERR# independent of this bit's state. 1 = Enable. 0 = Disable.



# Functional Description

# 4

This chapter describes the 82443BX interfaces on-chip functional units. Section 4.1, "System Address Map" on page 4-1 provides a system-level address memory map and describes the memory space controls provided by the 82443BX. This section also describes the I/O address map. Note that 82443BX register maps are provided in Chapter 3, "Register Description".

The 82443BX Host-to-PCI Bridge functions are described Host, PCI, and AGP interfaces are described in Section 4.2, "Host Interface" on page 4-10, Section 4.4, "PCI Interface" on page 4-24, and Section 4.5, "AGP Interface" on page 4-24.

The DRAM interface including supported DRAM types, organizations, configurations, and register programming considerations is provided in Section 4.3, "DRAM Interface" on page 4-14. Data integrity support on the Host bus, PCI bus, and DRAM interface is described in Section 4.6, "Data Integrity Support" on page 4-25.

System clocking requirements is provided in Section 4.7, "System Clocking" on page 4-28.

The 82443BX has various power management capabilities. Suspend resume, clock control, SDRAM power down, and SMRAM functions are described in Section 4.8, "Power Management" on page 4-28. This section also contains information on the 82443BX reset operations.

## 4.1 System Address Map

A Pentium® Pro processor-based system with the Intel® 440BX AGPset supports 4 GB of addressable memory space and 64 KB + 3 of addressable I/O space. (The Pentium® Pro processor bus I/O addressability is 64 KB + 3). There is a programmable memory address space under the 1 MB region which is divided into regions which can be individually controlled with programmable attributes such as Disable, Read/Write, Write Only, or Read Only. Attribute programming is described in the Register Description section. This section focuses on how the memory space is partitioned and what these separate memory regions are used for. The I/O address space requires much simpler mapping and it is explained at the end of this section.

The Pentium Pro processor family supports addressing of memory ranges larger than 4 GB. The 82443BX Host Bridge claims any access over 4 GB by terminating transaction (without forwarding it to PCI or AGP). Writes are terminated simply by dropping the data and for reads the 82443BX returns all zeros on the host bus. Note that the 82443BX as a target does not support the PCI Dual Address Cycle Mechanism (DAC) which allows addressing of >4GB on either the PCI or AGP interface.

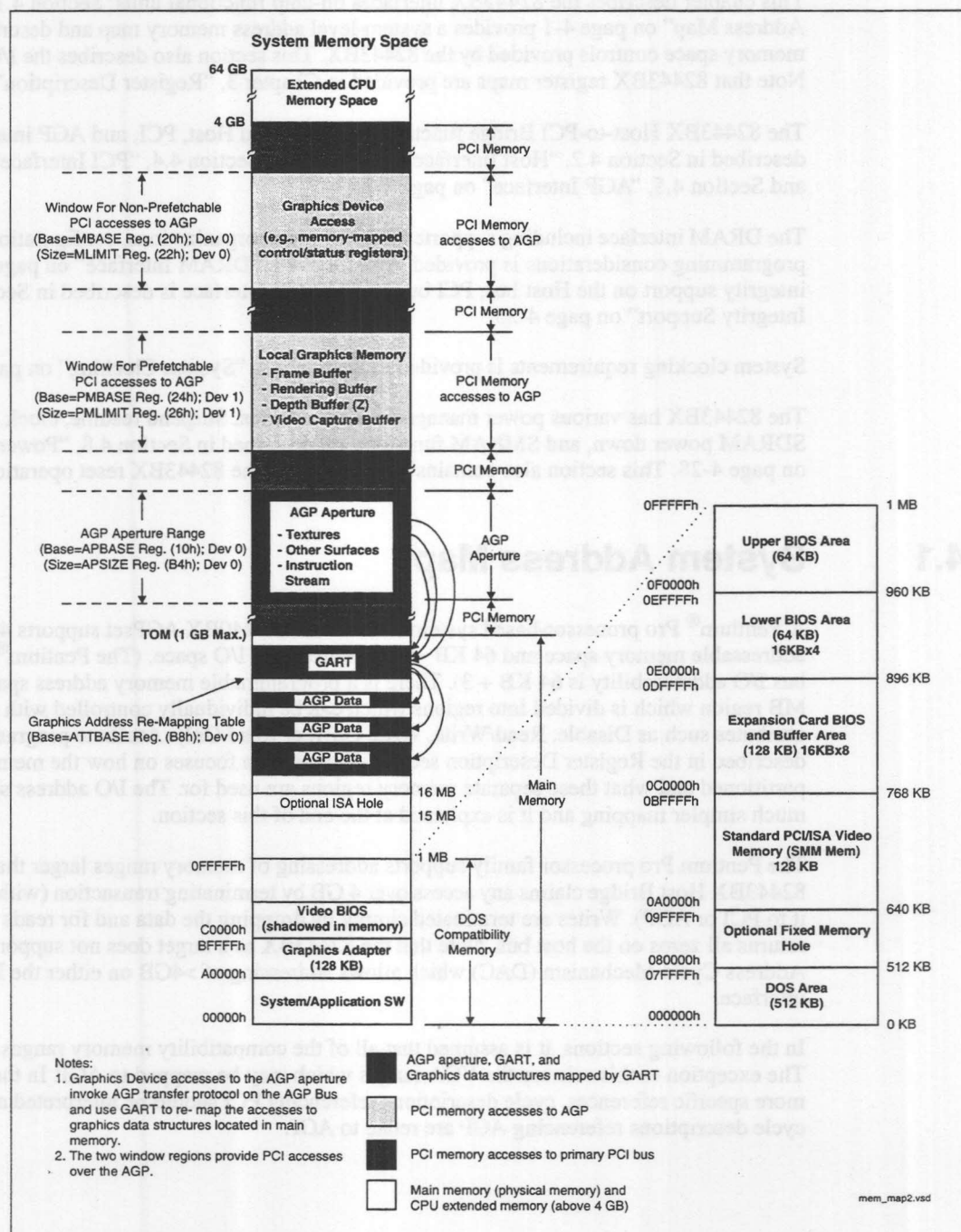
In the following sections, it is assumed that all of the compatibility memory ranges reside on PCI. The exception to this rule are the VGA ranges which may be mapped to AGP. In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as PCI, while cycle descriptions referencing AGP are relate to AGP.



### 4.1.1 Memory Address Ranges

Figure 4-1 provides a detailed 82443BX memory map indicating specific memory regions defined by AGP and supported by the Intel® 440BX AGPset.

### Figure 4-1. Memory System Address Space



### 4.1.1.1 Compatibility Area

This area is divided into the following address regions:

- 0–512 KB DOS Area
- 512 KB – 640 KB DOS Area - Optional ISA/PCI Memory
- 640KB – 768 KB Video Buffer Area
- 768 KB – 896 KB in 16KB sections (total of 8 sections) - Expansion Area
- 896KB – 960 KB in 16KB sections (total of 4 sections) - Extended System BIOS Area
- 960 KB – 1 MB Memory (BIOS Area) - System BIOS Area

There are sixteen memory segments in the compatibility area. Thirteen of the memory ranges can be enabled or disabled independently for both read and write cycles. One segment (512 KB–640 KB) which can be mapped to either main DRAM or PCI.

**Table 4-1. Memory Segments and their Attributes**

Memory Segments	Attributes	Comments
000000h–07FFFFh	fixed - always mapped to main DRAM	0 – 512 KB; DOS Region
080000h–09FFFFh	configurable as PCI or main DRAM	512 KB – 640 KB; DOS Region
0A0000h–0BFFFFh	mapped to PCI - configurable as SMM space	Video Buffer (physical DRAM configurable as SMM space)
0C0000h–0C3FFFh	WE; RE	Add-on BIOS
0C4000h–0C7FFFh	WE; RE	Add-on BIOS
0C8000h–0CBFFFh	WE; RE	Add-on BIOS
0CC000h–0CFFFFh	WE; RE	Add-on BIOS
0D0000h–0D3FFFh	WE; RE	Add-on BIOS
0D4000h–0D7FFFh	WE; RE	Add-on BIOS
0D8000h–0DBFFFh	WE; RE	Add-on BIOS
0DC000h–0DFFFFh	WE; RE	Add-on BIOS
0E0000h–0E3FFFh	WE; RE	BIOS Extension
0E4000h–0E7FFFh	WE; RE	BIOS Extension
0E8000h–0EBFFFh	WE; RE	BIOS Extension
0EC000h–0EFFFFh	WE; RE	BIOS Extension
0F0000h–0FFFFFFh	WE; RE	BIOS Area

#### DOS Area (00000h–9FFFFh)

The DOS area is 640 KB and it is further divided into two parts. The 512 KB area at 0 to 7FFFFh is always mapped to the main memory controlled by the 82443BX, while the 128 KB address range from 080000 to 09FFFFh can be mapped to PCI or to main DRAM. By default this range is mapped to main memory and can be declared as a main memory hole (accesses forwarded to PCI) via the 82443BX's FDHC configuration register.

#### Video Buffer Area (A0000h–BFFFFh)

The 128 KB graphics adapter memory region is normally mapped to a legacy video device on PCI (typically VGA controller). This area is not controlled by attribute bits and CPU-initiated cycles in this region are forwarded to PCI or AGP for termination. This region is also the default region for SMM space.

The SMRAM Control register controls how SMM accesses to this space are treated.

**Monochrome Adapter (MDA) Range (B0000h–B7FFFh)**

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. In an AGP system, accesses in the normal VGA range are forwarded to the AGP bus. Since the monochrome adapter may be on the PCI (or ISA) bus, the 82443BX must decode cycles in the MDA range and forward them to PCI.

**Expansion Area (C0000h–DFFFFh)**

This 128 KB ISA Expansion region is divided into eight 16 KB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through the Host-to-PCI bridge and are subtractively decoded to ISA space. Memory that is disabled is not remapped.

**Extended System BIOS Area (E0000h–EFFFFh)**

This 64 KB area is divided into four 16 KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to PCI. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

**System BIOS Area (F0000h–FFFFFh)**

This area is a single 64 KB segment. This segment can be assigned read and write attributes. It is by default (after reset) Read/Write disabled and cycles are forwarded to PCI. By manipulating the Read/Write attributes, the 82443BX can “shadow” BIOS into the main DRAM. When disabled, this segment is not remapped.

**4.1.1.2 Extended Memory Area**

This memory area covers 100000h (1 MB) to FFFFFFFFh (4 GB-1) address range and it is divided into the following regions:

- Main DRAM Memory from 1 MB to the Top of Memory; maximum of 256 MB using 16M DRAM technology or 1 GB using 64M technology
- PCI Memory space from the Top of Memory to 4 GB with two specific ranges:
  - APIC Configuration Space from FEC0\_0000h (4 GB-20 MB) to FECF\_FFFFh and EE0\_0000h to FEEF\_FFFFh
  - High BIOS area from 4 GB to 4 GB – 2 MB

**Main DRAM Address Range (0010\_0000h to Top of Main Memory)**

The address range from 1 MB to the top of main memory is mapped to main DRAM address range controlled by the 82443BX. All accesses to addresses within this range will be forwarded by the 82443BX to the DRAM unless a hole in this range is created using the fixed hole as controlled by the FDHC register. Accesses within this hole are forwarded to PCI.

The range of physical DRAM memory disabled by opening the hole is not remapped to the Top of the Memory.

**Extended SMRAM Address Range (Top of Main Memory – TSEG)**

An extended SMRAM space of up to 1 MB can be defined in the address range at the top of memory. The size of the SMRAM space is determined by the TSEG value in the ESMRAMC register. When the extended SMRAM space is enabled, non-SMM CPU accesses and all PCI and



AGP accesses in this range are forwarded to PCI. When SMM is enabled the amount of memory available to the system is equal to the amount of physical DRAM minus the value in the TSEG register.

**Note:** When extended SMRAM is used, the maximum amount of DRAM supported is limited to 256 MB.

### PCI Memory Address Range (Top of Main Memory to 4 GB)

The address range from the top of main DRAM to 4 GB (top of physical memory space supported by the Intel® 440BX AGPset) is normally mapped to PCI. There are two exceptions to this rule:

- Addresses decoded to the AGP Memory Window defined by the MBASE, MLIMIT, PMBASE, and PMLIMIT registers are mapped to AGP.
- Addresses decoded to the Graphics Aperture range defined by the APBASE and APSIZE registers are mapped to the main DRAM.

There are two sub-ranges within the PCI Memory address range defined as APIC Configuration Space and High BIOS Address Range. The AGP Memory Window and Graphics Aperture Window **MUST NOT** overlap with these two ranges. These ranges are described in detail in the following paragraphs.

### APIC Configuration Space (FEC0\_0000h -FECF\_FFFFh, FEE0\_0000h- FEEF\_FFFFh)

This range is reserved for APIC configuration space which includes the default I/O APIC configuration space. The default Local APIC configuration space is FEE0\_0000h to FEEF\_0FFFh.

CPU accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the CPU. However, a MTRR must be programmed to make the Local APIC range uncacheable (UC). The Local APIC base address in each CPU should be relocated to the FEC0\_0000h (4 GB – 20 MB) to FECF\_FFFFh range so that one MTRR can be programmed to 64 KB for the Local and I/O APICs. The I/O APIC(s) usually reside in the I/O Bridge portion of the AGPset or as a stand-alone component(s). For Intel® 440BX AGPset systems using the PIIX4E, the I/O APIC is supported as a stand-alone component residing on the X-Bus.

I/O APIC units will be located beginning at the default address FEC0\_0000h. The first I/O APIC will be located at FEC0\_0000h. Each I/O APIC unit is located at FEC0\_x000h where x is I/O APIC unit number 0 through F (hex). This address range will be normally mapped to PCI.

**Note:** There is no provision to support an I/O APIC device on AGP. Also the I/O APIC is not supported in a mobile platform.

The address range between the APIC configuration space and the High BIOS (FED0\_0000h to FEDF\_FFFFh) is always mapped to the PCI.

### High BIOS Area (FFE0\_0000h –FFFF\_FFFFh)

The top 2 MB of the Extended Memory Region is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. CPU begins execution from the High BIOS after reset. This region is mapped to PCI so that the upper subset of this region aliases to 16 MB–256 KB range. The actual address space required for the BIOS is less than 2 MB but the minimum CPU MTRR range for this region is 2 MB so that full 2 MB must be considered. The PIIX4E supports a maximum of 1 MB in the High BIOS range.

### 4.1.1.3 AGP Memory Address Range

The 82443BX can be programmed to direct memory accesses to the AGP bus interface when addresses are within either of two ranges specified via registers in 82443BX Device #1 configuration space. The first range is controlled via the Memory Base Register (MBASE) and Memory Limit Register (MLIMIT) registers. The second range is controlled via the Prefetchable Memory Base (PMBASE) and Prefetchable Memory Limit (PMLIMIT) registers

The 82443BX positively decodes memory accesses to AGP memory address space as defined by the following equations:

$$\text{Memory\_Base\_Address} \leq \text{Address} \leq \text{Memory\_Limit\_Address}$$

$$\text{Prefetchable\_Memory\_Base\_Address} \leq \text{Address} \leq \text{Prefetchable\_Memory\_Limit\_Address}$$

The effective size of the range is programmed by the plug-and-play configuration software and it depends on the size of memory claimed by the AGP compliant device. Normally, these ranges reside above the Top-of-Main-DRAM and below High BIOS and APIC address ranges.

**Note:** The 82443BX Device #1 memory range registers described above are used to allocate memory address space for any devices on AGP that require such a window. These devices include the AGP compliant device, and multifunctional AGP compliant devices where one or more functions are implemented as PCI devices.

### 4.1.1.4 AGP DRAM Graphics Aperture

Memory-mapped, graphics data structures can reside in a *Graphics Aperture* to main DRAM memory. This aperture is an address range defined by the APBASE configuration register of the 82443BX Host Bridge. The APBASE register follows the normal base address register template as defined by the PCI 2.1 specification. The size of the range claimed by the APBASE is programmed via “back-end” register APSIZE (programmed by the chip-set specific BIOS before plug-and-play session is performed). APSIZE allows selection of the aperture size of 4 MB, 8 MB, 16 MB, 32 MB, 64 MB, 128 MB and 256 MB. By programming APSIZE to a specific size, the corresponding lower bits of APBASE are forced to “0” (behave as hardwired). Default value of APSIZE forces aperture size of 256 MB. Aperture address range is naturally aligned.

Although this aperture appears to be established in PCI memory space, in fact the 82443BX forwards accesses within the aperture range to the main DRAM subsystem. The originally issued addresses are translated (within 82443BX’s DRAM controller subsystem) via a translation table maintained in main memory. Translation table entries may be partially cached in a Graphics Translation Look-aside Buffer (GTLB) implemented within the 82443BX’s DRAM subsystem. The aperture range will not be cacheable in the processor caches.

### 4.1.1.5 System Management Mode (SMM) Memory Range

82443BX supports the use of main memory as System Management RAM (SMRAM) enabling the use of System Management Mode. The 82443BX supports two SMRAM options: Compatible SMRAM (C\_SMRAM) and Extended SMRAM (E\_SMRAM). System Management RAM (SMRAM) space provides a memory area that is available for the SMI handler’s and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. The 82443BX provides three SMRAM options:

- Below 1 MB option that supports compatible SMI handlers.
- Above 1 MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional larger write-back cacheable T\_SEG area from 128KB to 1MB in size above 1 MB that is reserved from the highest area in system DRAM memory. The above 1 MB solutions require changes to compatible SMRAM handlers code to properly execute above 1 MB.

Table 4-2 summarizes the operation of SMRAM space cycles targeting the SMI space addresses.

**Table 4-2. SMRAM Decoding**

Name of Range	Transaction Address	DRAM Address
compatible (Range A)	A0000–BFFFFh	A0000–BFFFFh
HI-SMRAM (RANGE H)	256M + A0000h to 256M + FFFFFh	A0000–FFFFFh
TSEG (RANGE T)	256M + TOM to 256M + TOM - TSEG_SIZE	TOM to TOM - TSEG_SIZE

**Table 4-3. SMRAM Range Decode**

Global SMRAM	H_SMFRAME	TSEG_EN	A Range	H Range	T Range
0	x	x	Disable	Disable	Disable
1	0	0	Enable	Disable	Disable
1	0	1	Enable	Disable	Enable
1	1	0	Disabled	Enable	Disable
1	1	1	Disabled	Enable	Enable

**NOTE:**

1. 1 = Enabled and 0 = Disabled

Table 4-4 defines the control of the decode for all code fetches and data fetches to SMRAM ranges (as defined by Table 4-3). The G\_SMFRAME bit provides a global disable for all SMRAM memory. The D\_OPEN bit allows software to write to the SMRAM ranges without being in SMM. BIOS software can use this bit to initialize SMM code at Power up. The D\_LCK bit limits the SMRAM range access to only SMM mode accesses. The D\_CLS bit causes SMM data accesses to be forwarded to PCI. The SMM software can use this bit to write to video memory while running code out of DRAM.

**Table 4-4. SMRAM Decode Control**

G_SMFRAME	D_LCK	D_CLS	D_OPEN	SMM Mode	SMM Code Fetch	SMM Data Fetch
0	x	x	x	x	Disable	Disable
1	0	x	0	0	Disable	Disable
1	0	0	0	1	Enable	Enable
1	0	0	1	x	Enable	Enable
1	0	1	0	1	Enable	Disable
1	0	1	1	x	Invalid	Invalid
1	1	x	x	0	Disable	Disable
1	1	0	x	1	Enable	Enable
1	1	1	x	1	Enable	Disable

**NOTE:**

1. 1 = Enabled and 0 = Disabled



Refer to Section 4.8, “Power Management” on page 4-28 for more details on SMRAM support.

Reiteration:

- Only un-cacheable SMM regions may overlap PCI or AGP Windows.
- SMM regions will not overlap the AGP aperture.
- Software (not in SMM) will not access PCI memory behind cacheable SMM regions.
- PCI or AGP masters cannot access the SMM space.

### 4.1.2 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into 82443BX DRAM memory. Typically, this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as a read-only during the copy process while DRAM at the same time is designated write-only. After copying, the DRAM is designated read-only so that ROM is shadowed. CPU bus transactions are routed accordingly.

### 4.1.3 I/O Address Space

The 82443BX does not support the existence of any other I/O devices besides itself on the CPU bus. The 82443BX generates either PCI or AGP bus cycles for all CPU I/O accesses. The 82443BX contains three internal registers in the CPU I/O space, Configuration Address Register (CONFIG\_ADDRESS) and the Configuration Data Register (CONFIG\_DATA) and Power Management Control Register. These locations are used to implement PCI configuration space access mechanism and as described in Section 3.1, “I/O Mapped Registers” on page 3-2.

The CPU allows 64K+3 bytes to be addressed within the I/O space. The 82443BX propagates the CPU I/O address without any translation on to the destination bus and therefore provides addressability for 64K+3 byte locations. Note that the upper 3 locations can be accessed only during I/O address wrap-around when CPU bus A16# address signal is asserted. A16# is asserted on the CPU bus whenever an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. A16# is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

The I/O accesses (other than ones used for PCI configuration space access) are forwarded normally to the PCI bus unless they fall within the PCI/AGP I/O address range as defined by the mechanisms in Section 4.1.4. The 82443BX will not post I/O write cycles to IDE.

### 4.1.4 AGP I/O Address Mapping

The 82443BX can be programmed to direct non-memory (I/O) accesses to the AGP bus interface when CPU-initiated I/O cycle addresses are within the AGP I/O address range. This range is controlled via the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in 82443BX Device #1 configuration space.

The 82443BX positively decodes I/O accesses to AGP I/O address space as defined by the following equation:

$$\text{I/O\_Base\_Address} \leq \text{CPU I/O Cycle Address} \leq \text{I/O\_Limit\_Address}$$

The effective size of the range is programmed by the plug-and-play configuration software and it depends on the size of I/O space claimed by the AGP compliant device.

Note that the 82443BX Device #1 I/O address range registers defined above are used for all I/O space allocation for any devices requiring such a window on AGP. These devices would include the AGP compliant device and multifunctional AGP compliant devices where one or more functions are implemented as PCI devices.

### 4.1.5 Decode Rules and Cross-Bridge Address Mapping

The address map described above applies globally to accesses arriving on any of the three interfaces (i.e., Host bus, PCI or AGP).

#### 4.1.5.1 PCI Interface Decode Rules

The 82443BX accepts accesses from PCI to the following address ranges:

- All memory read and write accesses to Main DRAM
- Memory Write accesses to AGP memory range defined by MBASE, MLIMIT, PMBASE, and PMLIMIT. 82443BX will not respond to memory read accesses to this range.
- Memory read/write accesses to the Graphics Aperture defined by APBASE and APSIZE.

PCI accesses that fall elsewhere within the PCI memory range will not be accepted. PCI cycles not explicitly claimed by the 82443BX are either subtractively decoded or master-aborted on PCI.

#### 4.1.5.2 AGP Interface Decode Rules

##### Cycles Initiated Using PCI Protocol

Accesses between AGP and PCI are limited to memory writes using the PCI protocol. Write cycles are forwarded to PCI if the addresses are not within main DRAM range, AGP memory ranges, or Graphics Aperture range.

The 82443BX will claim AGP initiated memory read transactions decoded to the main DRAM range or the Graphics Aperture range. All other memory read requests will be master-aborted by the AGP initiator as a consequence of 82443BX not responding to a transaction.

If agent on AGP issues an I/O, PCI Configuration or PCI Special Cycle transaction, the 82443BX will not respond and cycle will result in a master-abort.

##### Cycles Initiated Using AGP Protocol

All cycles must reference main memory (i.e., main DRAM address range or Graphics Aperture range which is also physically mapped within DRAM but using different address range). AGP-initiated cycles that target DRAM are not snooped on the host bus, even if they fall outside of the AGP aperture range.

If cycle is outside of main memory range then it will terminate as follows:

- Reads: return random value
- Writes: dropped "on the floor" i.e. terminated internally without affecting any buffers or main memory
- ECC errors that occur on reads outside of DRAM are not reported or scrubbed.

### 4.1.5.3 Legacy VGA Ranges

The legacy VGA memory range A0000h–BFFFFh is mapped either to PCI or to AGP depending on the programming of the BCTRL configuration register in 82443BX Device #1 configuration space, and the NBXCONF (MDAP bit) configuration register in Device #0 configuration space. The same registers control mapping of VGA I/O address ranges. VGA I/O range is defined as addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases - A[15:10] are not decoded).

Topic	Definition
AGP IO range	The AGP bus can be allocated with 1 block of IO space with a granularity of 4KB. The IO base address register points to the beginning of the AGP IO range while IO limit address register points to the end of this range. The IO range definition is based on the PCI to PCI specification.
ISA_EN	<p>The ISA_EN bit in the 82443BX device1 is necessary in ISA bus based systems where there is a need to allocate IO space to AGP bus devices. This is necessary since legacy ISA devices decode IO range of address [9:0] only and thus the IO address of the devices are aliased for every 1 KB of the 64 KB IO range. Therefore, to provide IO range to AGP bus and maintain the ISA IO legacy rules, the ISA_EN is set. As a result, all CPU cycles in the address ranges: "xxxx_xx01_0000_0000"b to "xxxx_xx11_1111_1111"b, that is the top 768 bytes of each 1KB aligned block, are sent to the PCI bus independent of whether this particular address is inside or outside the range allocated to the AGP bus.</p> <p>The above is relevant only to CPU-initiated cycles, as PCI and AGP master IO cycles are never claimed by the 82443BX. The ISA_EN functional definition is based on the PCI to PCI specification.</p>
VGA_EN	VGA IO range is defined in the following ranges: 3B0-3BBh, 3C0-3DFh. When the VGA_EN is set, all CPU initiated IO cycles in the VGA IO range are forwarded to the AGP bus, independent of whether the ISA_EN bit is set or not. Thus the VGA_EN bit setting takes precedence relative to the setting of the ISA_EN bit. The VGA_EN functional definition is based on the PCI to PCI specification.
MDAP	<p>The MDA IO range includes the ports 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh. Once the VGA_EN is set, it is legal to set the MDAP bit to indicate that a second CRT controller (Monochrome Display Adapter) resides in the PCI or ISA bus. In this case, all the CPU-initiated IO cycles in the VGA range that are not in the above ports are sent to AGP bus while the cycles to the above six IO ports (and to all the aliased ports) are sent to PCI bus.</p> <p>Note that the CPU IO cycles to the above ports are sent to AGP bus independent of the AGP IO range and ISA_EN setting.</p>

## 4.2 Host Interface

The host interface of the 82443BX is optimized to support the Pentium II processor with bus clock frequencies of 100 MHz and 66/60 MHz. The 82443BX implements the host address, control, and data bus interfaces within a single device. Host bus addresses are decoded by the 82443BX for accesses to main memory, PCI memory, PCI I/O, PCI configuration space and AGP space (memory, I/O and configuration). The 82443BX takes advantage of the pipelined addressing capability of the Pentium II processor to improve the overall system performance.

### 4.2.1 Host Bus Device Support

The 82443BX recognizes and supports a large subset of the transaction types that are defined for the Pentium Pro processor bus interface. However, each of these transaction types have a multitude of response types, some of which are not supported by this controller. All transactions are processed in the order that they are received on the Pentium® Pro processor bus. Table 4-5 summarizes the transactions supported by the 82443BX.



Table 4-5. Host Bus Transactions Supported By 82443BX

Transaction	REQA[4:0]#	REQB[4:0]#	82443BX Support
Deferred Reply	0 0 0 0 0	X X X X X	The 82443BX initiates a deferred reply for a previously deferred transaction.
Reserved	0 0 0 0 1	X X X X X	Reserved
Interrupt Acknowledge	0 1 0 0 0	0 0 0 0 0	Interrupt acknowledge cycles are forwarded to the PCI bus.
Special Transactions	0 1 0 0 0	0 0 0 0 1	See separate table in Special Cycles section.
Reserved	0 1 0 0 0	0 0 0 1 x	Reserved
Reserved	0 1 0 0 0	0 0 1 x x	Reserved
Branch Trace Message	0 1 0 0 1	0 0 0 0 0	The 82443BX terminates a branch trace message without latching data.
Reserved	0 1 0 0 1	0 0 0 0 1	Reserved
Reserved	0 1 0 0 1	0 0 0 1 x	Reserved
Reserved	0 1 0 0 1	0 0 1 x x	Reserved
I/O Read	1 0 0 0 0	0 0 x LEN#	I/O read cycles are forwarded to PCI or AGP. I/O cycles which are in the 82443BX configuration space are not forwarded to PCI.
I/O Write	1 0 0 0 1	0 0 x LEN#	I/O write cycles are forwarded to PCI or AGP. I/O cycles which are in the 82443BX configuration space are not forwarded to PCI.
Reserved	1 1 0 0 x	0 0 x x x	Reserved
Memory Read & Invalidate	0 0 0 1 0	0 0 x LEN#	Host initiated memory read cycles are forwarded to DRAM or the PCI/1 bus. The 82443BX initiates an MRI cycle for a PCI/1 initiated write cycle to DRAM.
Reserved	0 0 0 1 1	0 0 x LEN#	Reserved
Memory Code Read	0 0 1 0 0	0 0 x LEN#	Memory code read cycles are forwarded to DRAM or PCI/1.
Memory Data Read	0 0 1 1 0	0 0 x LEN#	Host initiated memory read cycles are forwarded to DRAM or the PCI/1 bus. The 82443BX initiates a memory read cycle for a PCI/1 initiated read cycle to DRAM.
Memory Write (no retry)	0 0 1 0 1	0 0 x LEN#	This memory write is a writeback cycle and cannot be retried. The 82443BX forwards the write to DRAM.
Memory Write (can be retried)	0 0 1 1 1	0 0 x LEN#	The normal memory write cycle is forwarded to DRAM or PCI/1.

**NOTE:**

1. For Memory cycles, REQA[4:3]# = ASZ#. The 82443BX only supports ASZ# = 00 (32 bit address).
2. REQb[4:3]# = DSZ#. For the Pentium® Pro processor, DSZ# = 00 (64 bit data bus size).
3. LEN# = data transfer length as follows:

**LEN#      Data length**

- |    |  |
|----|--|
| 00 | ≤ 8 bytes (BE[7:0]# specify granularity) |
| 01 | Length = 16 bytes BE[7:0]# all active    |
| 10 | Length = 32 bytes BE[7:0]# all active    |
| 11 | Reserved                                 |

Table 4-6. Host Responses supported by the 82443BX

RS2#	RS1#	RS0#	Description	82443BX Support
0	0	0	idle	
0	0	1	Retry Response	To avoid deadlock, this response is generated when a resource cannot currently be accessed by the processor. PCI-directed reads, writes, DRAM locked reads, AGP reads and writes can be retried.
0	1	0	Deferred Response	This response can be returned for all transactions that can be executed 'out of order.' PCI-directed reads (memory, I/O and Interrupt Acknowledge) and writes (I/O only), and AGP directed reads (memory and I/O) and writes (I/O only) can be deferred.
0	1	1	Reserved	Reserved
1	0	0	Hard Failure	Not supported.
1	0	1	No Data Response	This is for transactions where the data has already been transferred or for transactions where no data is transferred. Writes and zero length reads receive this response.
1	1	0	Implicit Writeback	This response is given for those transactions where the initial transactions snoop hits on a modified cache line.
1	1	1	Normal Data Response	This response is for transactions where data accompanies the response phase. Reads receive this response.

### Special Cycles

A Special Cycle is defined when REQa[4:0] = 01000 and REQb[4:0] = xx001. The first address phase Aa[35:3]# is undefined and can be driven to any value. The second address phase, Ab[15:8]# defines the type of Special Cycle issued by the processor.

Table 4-3 specifies the cycle type and definition as well as the action taken by the 82443BX when the corresponding cycles are identified.

Table 4-7. Host Special Cycles with 82443BX

BE[7:0]#	Special Cycle Type	Action Taken
0000 0000	NOP	This transaction has no side-effects.
0000 0001	Shutdown	This transaction is issued when an agent detects a severe software error that prevents further processing. This cycle is claimed by the 82443BX. The 82443BX issues a shutdown special cycle on the PCI bus. This cycle is retired on the CPU bus after it is terminated on the PCI via a master abort mechanism.
0000 0010	Flush	This transaction is issued when an agent has invalidated its internal caches without writing back any modified lines. The 82443BX claims this cycle and retires it.
0000 0011	Halt	This transaction is issued when an agent executes a HLT instruction and stops program execution. This cycle is claimed by the 82443BX and propagated to PCI as a Special Halt Cycle. This cycle is retired on the CPU bus after it is terminated on the PCI via a master abort mechanism.
0000 0100	Sync	This transaction is issued when an agent has written back all modified lines and has invalidated its internal caches. The 82443BX claims this cycle and retires it.

Table 4-7. Host Special Cycles with 82443BX

BE[7:0]#	Special Cycle Type	Action Taken
0000 0101	Flush Acknowledge	This transaction is issued when an agent has completed a cache sync and flush operation in response to an earlier FLUSH# signal assertion. The 82443BX claims this cycle and retires it.
0000 0110	Stop Clock Acknowledge	This transaction is issued when an agent enters Stop Clock mode. This cycle is claimed by the 82443BX and propagated to the PCI as a Special Stop Grant Cycle. This cycle is completed on the CPU bus after it is terminated on the PCI via a master abort mechanism.
0000 0111	SMI Acknowledge	This transaction is first issued when an agent enters the System Management Mode (SMM).
all others	Reserved	

**NOTE:**

1. None of the host bus special cycles is propagated to the AGP interface.

## 4.2.2 Symmetric Multiprocessor (SMP) Protocol Support

The Intel® 440BX AGPset is optimized for uniprocessor system and also supports the symmetrical multiprocessor configurations of up to two CPUs on the host bus.

When configured for dual-processor, the Intel® 440BX AGPset-based platform must integrate an I/O APIC functionality and WSC# signaling mechanism must be enabled.

## 4.2.3 In-Order Queue Pipelining

The 82443BX interface to the CPU bus includes a four deep in-order queue to track pipelined bus transactions.

## 4.2.4 Frame Buffer Memory Support (USWC)

To allow for high speed write capability for graphics, the Pentium Pro processor family has introduced USWC memory type. The USWC (uncacheable, speculative, write-combining) memory type provides a write-combining buffering mechanism for write operations. A high percentage of graphics transactions are writes to the memory-mapped graphics region, normally known as the linear frame buffer. Reads and writes to USWC are non-cached and can have no side effects.

In the case of graphics, current 32-bit drivers (without modifications) would use Partial Write protocol to update the frame buffer. The highest performance write transaction on the CPU bus is the Line Write.



## 4.3 DRAM Interface

The 82443BX integrates a main memory DRAM controller that supports a 64-bit or 72-bit (64-bit memory data plus 8 ECC) DRAM array. The DRAM types supported are Synchronous (SDRAM) and Extended Data Out (EDO). The 82443BX does not support mixing of SDRAM and EDO. When the CPU bus is running at 100 MHz, the 82443BX DRAM interface runs at 100 MHz (SDRAM only). When the CPU bus is operating at 66 MHz, the 82443BX DRAM interface runs at 66 MHz (SDRAM or EDO). EDO DRAM technology is supported in mobile designs only at 66 MHz. The DRAM controller interface is fully configurable through a set of control registers. Complete descriptions of these registers are given in the Register Section. A brief overview of the registers which configure the DRAM interface is provided in this section.

The 82443BX supports industry standard 64/72-bit wide DIMM modules with SDRAM and EDO DRAM devices. The fourteen multiplexed address lines, MA[13:0], allow the 82443BX to support 1M, 2M, 4M, 8M, and 16M x72/64 DIMMs. Both symmetric and asymmetric addressing is supported. The 82443BX has sixteen CS# lines, used in pairs enabling the support of up to eight 64/72-bit rows of DRAM. For write operations of less than a QWord in size, the 82443BX will either perform a byte-wise write (non-ECC protected configuration) or a read-modify-write cycle by merging the write data on a byte basis with the previously read data (ECC or EC configurations). The 82443BX targets 60 ns EDO DRAMs and SDRAM with CL2 and CL3 and supports both single and double-sided DIMMs. When using EDO DRAM, up to 6 rows of memory are supported. The 82443BX provides refresh functionality with programmable rate (normal DRAM rate is 1 refresh/15.6ms). When using SDRAMs the 82443BX can be configured via the Paging Policy Register to keep multiple pages open within the memory array. Pages can be kept open in all rows of memory. When 4 bank SDRAM devices (64Mb technology) are used for a particular row, up to 4 pages can be kept open within that row.

The DRAM interface of the 82443BX is configured by the DRAM Control Register, DRAM Timing Register, SDRAM Control Register, bits in the NBXCFG and the eight DRAM Row Boundary (DRB) Registers. The DRAM configuration registers noted above control the DRAM interface to select EDO or SDRAM DRAMs, RAS timings, and CAS rates. The eight DRB Registers define the size of each row in the memory array, enabling the 82443BX to assert the proper CSA/B# pair for accesses to the array.

### 4.3.1 DRAM Organization and Configuration

The 82443BX supports 64/72-bit DRAM configurations. In the following discussion the term *row* refers to a set of memory devices that are simultaneously selected by a CSA/B# or RASA/B# pair. The 82443BX will support a maximum of 8 rows of memory when using SDRAMs in a desktop configuration. Up to 6 rows of memory are supported when using EDO DRAM. A row may be composed of discrete DRAM devices, single-sided or double-sided DIMMs.

The 82443BX has multiple copies of many of the signals interfacing to memory. The interface consists of the following pins.

- Multiple copies
  - MAA[13:0], MAB[12:11,9:0]# and MAB[13,10]
  - CSA[7:0]#, CSB[7:0]#
  - SRASA#, SRASB#
  - SCASA#, SCASB#
  - WEA#, WEB#
  - DQMA[7:0], DQMB[5,1]
  - CKE[5:0] (for 3 DIMM configuration)

- Single Copy
  - MD[63:0]
  - MECC[7:0]
  - GCKE (for 4 DIMM configuration)
  - FENA (FET switch control for 4 DIMM configuration)

The CS# pins function as RAS# pins in the case of EDO DRAMs. The DQM pins function as CAS# pins in the case of EDO DRAMs. Two CS# lines are provided per row. These are functionally equivalent. The extra copy is provided for loading reasons. The two SRAS#'s, SCAS#'s and WE#'s are also functionally equivalent and each copy drives two rows of DRAM. Most pins utilize programmable strength output buffers (refer to Register Section). When a row contains 16Mb SDRAMs, MAA11 and MAB11 function as Bank Select lines. When a row contains 64Mb SDRAMs, MAA/B[12:11] function as Bank Addresses (BA[1:0], or Bank Selects).

The entire memory array may be configured as either normal SDRAM, registered SDRAM or EDO DRAM. Mixing DRAM types within one system is not supported. DIMMs may be populated in any order. That is, any combination of rows may be populated. Registered SDRAM DIMMs allow for support of x4 SDRAM components.

Table 4-8 illustrates a sample of the possible DIMM socket configurations along with corresponding DRB programming.

**Table 4-8. Sample Of Possible Mix And Match Options For 6 Row/3 DIMM Configurations**

DIMM0\	DIMM1	DIMM2	DRB 0	DRB 1	DRB 2	DRB 3	DRB 4	DRB 5	DRB 6	DRB 7	Total Memory
0	0	1MB x 72/S	00h	00h	00h	00h	01h	01h	01h	01h	8 MB
1MBx72/S	0	0	01h	01h	01h	01h	01h	01h	01h	01h	8 MB
2MBx72/S	0	0	02h	02h	02h	02h	02h	02h	02h	02h	16 MB
1Mx72/S	1Mx72/S	0	01h	01h	02h	02h	02h	02h	02h	02h	16 MB
0	4Mx72/S	0	00h	00h	04h	04h	04h	04h	04h	04h	32 MB
2Mx72/D	2Mx72/D	2Mx72/D	01h	02h	03h	04h	05h	06h	06h	06h	48 MB
4Mx72/S	0	2Mx72/D	04h	04h	04h	04h	05h	06h	06h	06h	48 MB
4Mx72/S	0	4Mx72/S	04h	04h	04h	04h	08h	08h	08h	08h	64 MB
4Mx72/S	4Mx72/S	2Mx72/D	04h	04h	08h	08h	09h	10h	10h	10h	80 MB
8Mx72/D	0	4Mx72/S	04h	08h	08h	08h	0Ch	0Ch	0Ch	0Ch	96 MB
8Mx72/D	8Mx72/D	8Mx72/D	04h	08h	0Ch	10h	14h	18h	18h	18h	192 MB
16Mx72/S	16Mx72/S	0	10h	10h	20h	20h	20h	20h	20h	20h	256 MB
8Mx72/D	16Mx72/S	8Mx72/D	04h	08h	18h	18h	1Ch	20h	20h	20h	256 MB
0	32Mx72/D	16Mx72/S	00h	00h	10h	20h	30h	30h	30h	30h	384 MB
32Mx72/D	32Mx72/D	16Mx72/S	10h	20h	30h	40h	50h	50h	50h	50h	640 MB

**NOTE:**

1. "S" denotes single-sided DIMM's, "D" denotes double-sided DIMM's.

Figure 4-2 depicts the 82443BX connections for an SDRAM memory array and shows how the copies of the signals are distributed to the array. If cross bar switches are used, the unused input must be pulled down through a resistor. In an EDO memory array, the CSA/B[5:0]# signals would be RASA/B[5:0]# lines and the DQMA/B[7:0] signals would be CASA/B[7:0]# lines. GCKE requires external logic (not shown). For a 3 DIMM solution, separate CKE lines are provided for each row (CKE[5:0]).

Figure 4-2. Four-DIMM Configuration with FET switches

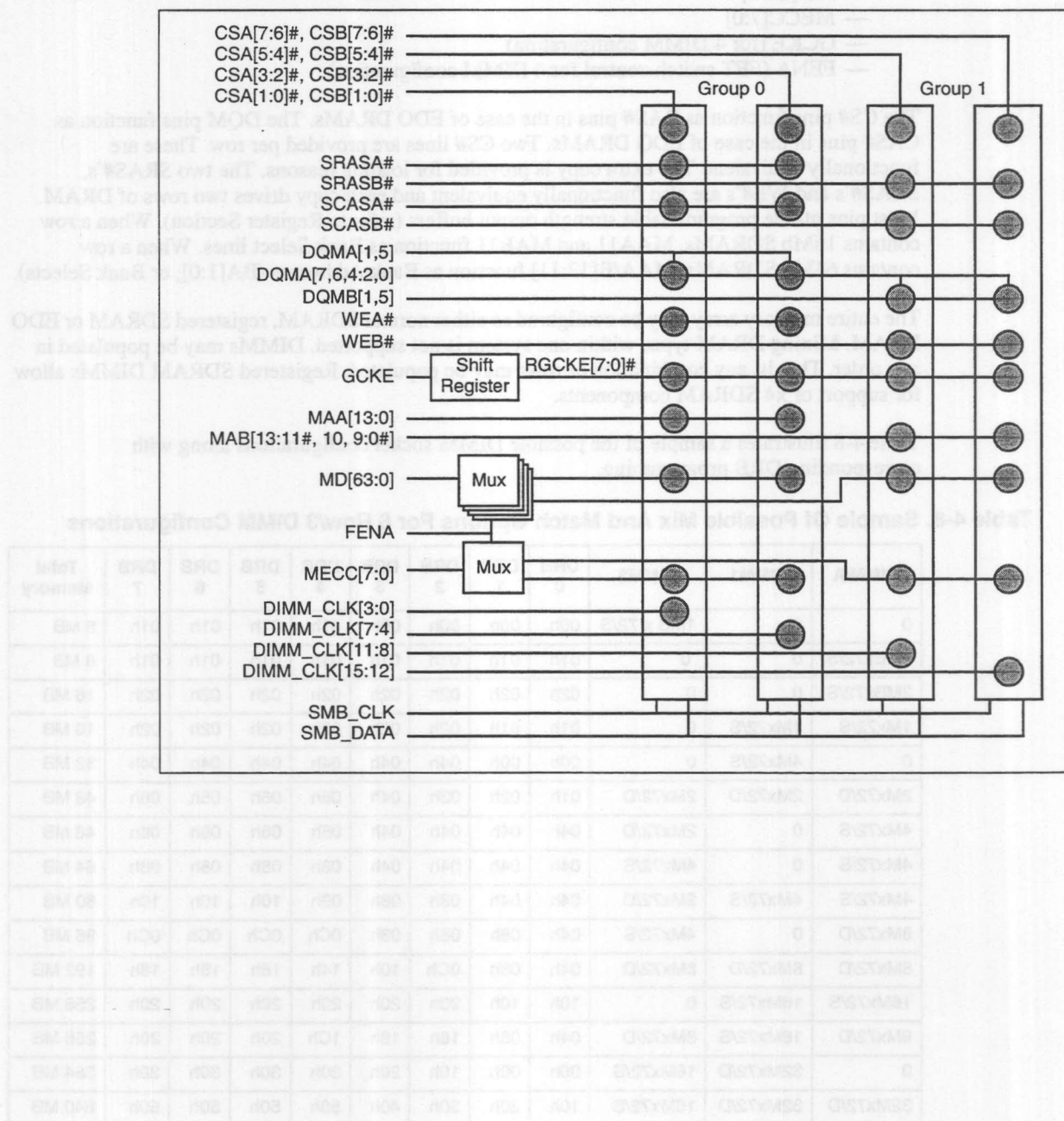




Figure 4-3. Three-DIMM SDRAM Configuration

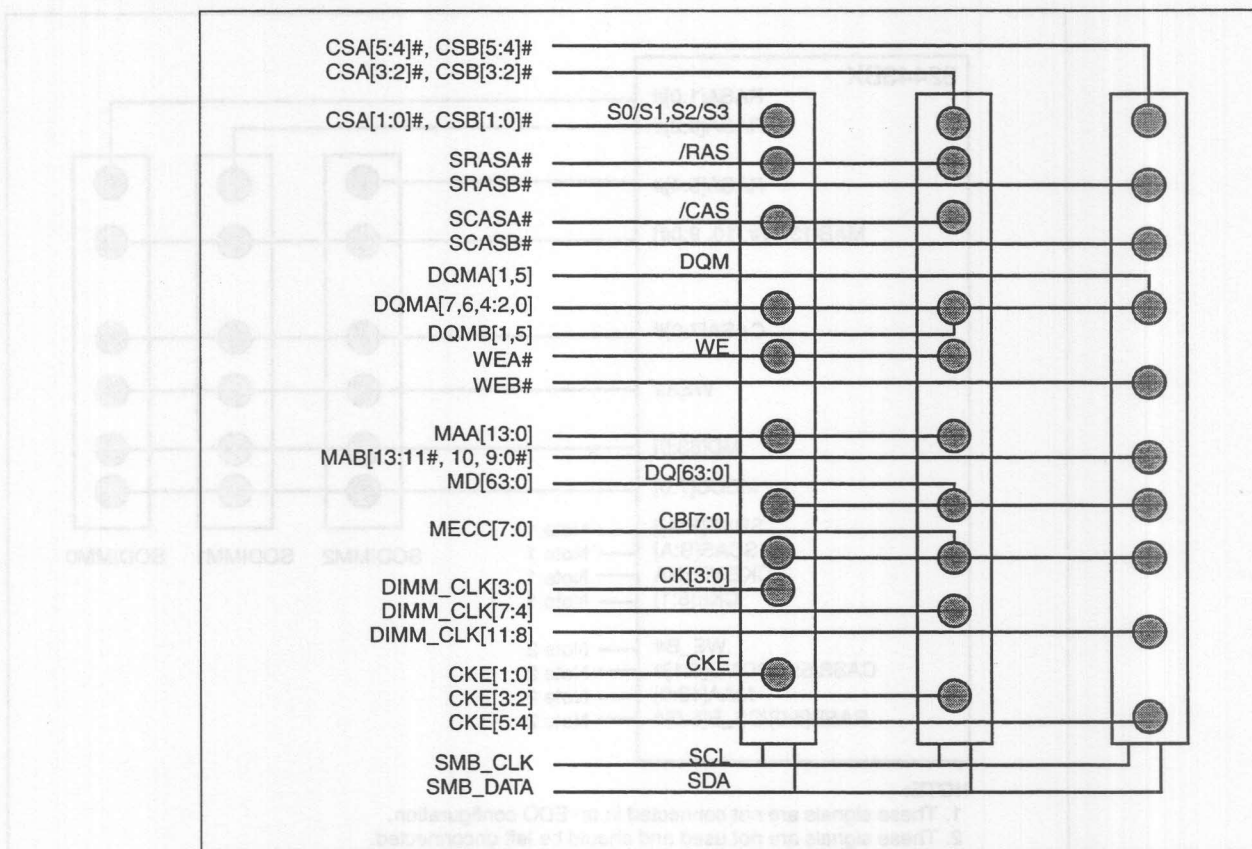


Figure 4-4. Three-SODIMMs EDO Configuration

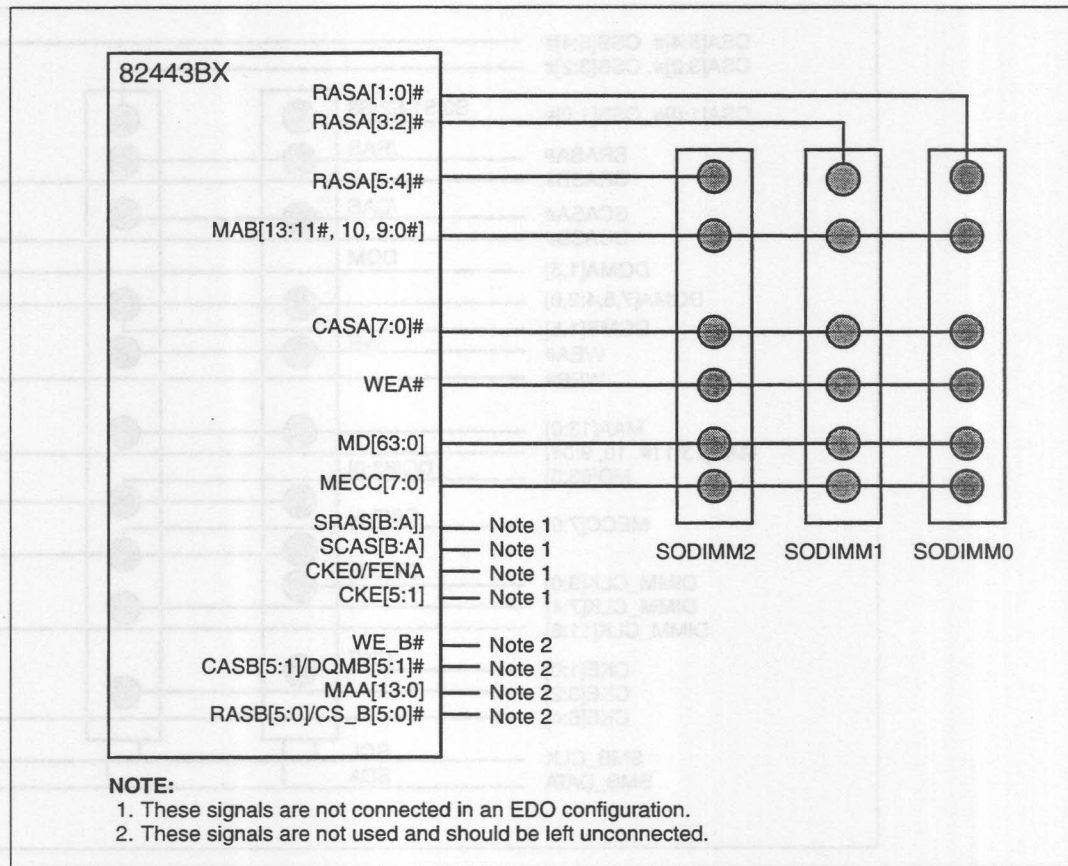
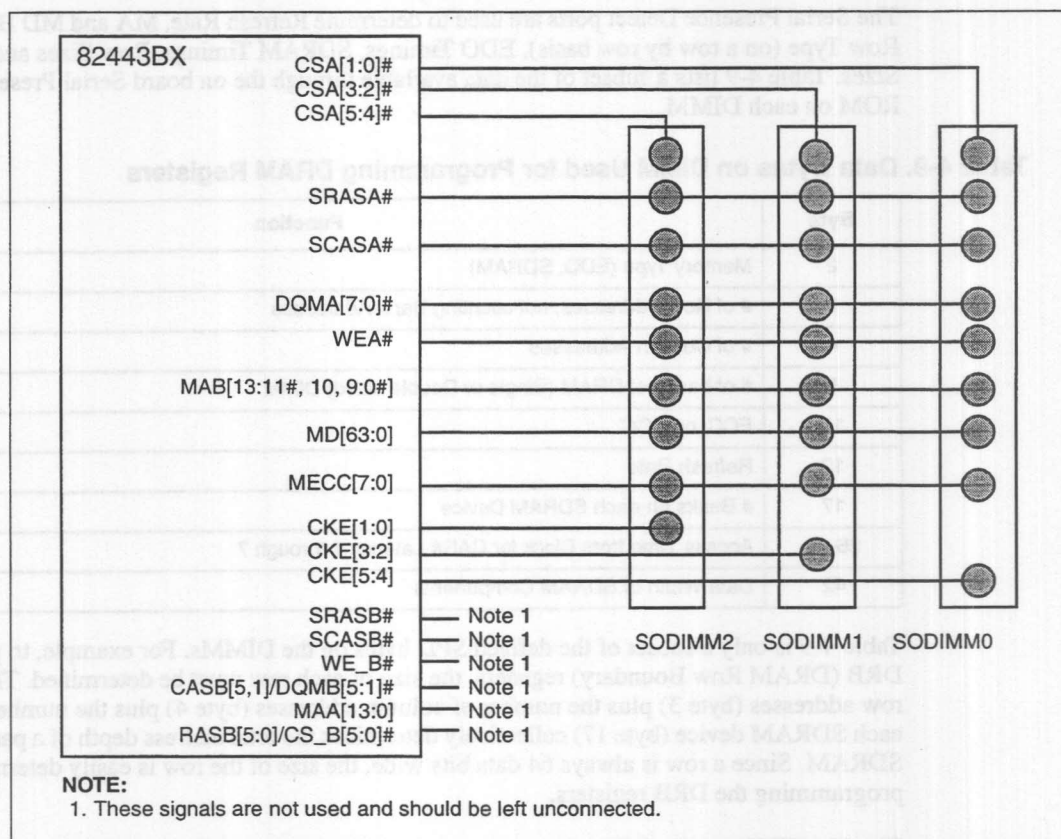


Figure 4-5. Three-SODIMMs SDRAM Configuration



#### 4.3.1.1 Configuration Mechanism For DIMMS

Detection of the type of DRAM installed on the DIMM is supported via Serial Presence Detect mechanism as defined in the JEDEC 168-pin DIMM standard. This standard uses the SCL, SDA and SA[2:0] pins on the DIMMs to detect the type and size of the installed DIMMs. No special programmable modes are provided on the 82443BX for detecting the size and type of memory installed. Type and size detection must be done via the serial presence detection pins.

##### Memory Detection and Initialization

Before any cycles to the memory interface can be supported, the 82443BX DRAM registers must be initialized. The 82443BX must be configured for operation with the installed memory types. Detection of memory type and size is done via the System Management Bus (SMB) interface on the PIIX4E. This two wire bus is used to extract the DRAM type and size information from the serial presence detect port on the DRAM DIMMs.

DRAM DIMMs contain a 5 pin serial presence detect interface, including SCL (serial clock), SDA (serial data) and SA[2:0]. Devices on the SMBus have a seven bit address. For the DRAM DIMMs, the upper four bits are fixed at 1010. The lower three bits are strapped on the SA[2:0] pins. SCL and SDA are connected directly to the System Management Bus on the PIIX4E. Thus data is read from the Serial Presence Detect port on the DIMMs via a series of IO cycles to the south bridge. BIOS essentially needs to determine the size and type of memory used for each of the eight rows of memory in order to properly configure the 82443BX memory interface.



### DRAM Register Programming

The Serial Presence Detect ports are used to determine Refresh Rate, MA and MD Buffer Strength, Row Type (on a row by row basis), EDO Timings, SDRAM Timings, Row Sizes and Row Page Sizes. Table 4-9 lists a subset of the data available through the on board Serial Presence Detect ROM on each DIMM.

**Table 4-9. Data Bytes on DIMM Used for Programming DRAM Registers**

Byte	Function
2	Memory Type (EDO, SDRAM)
3	# of Row Addresses, not counting Bank Addresses
4	# of Column Addresses
5	# of banks of DRAM (Single or Double sided) DIMM
11	ECC, no ECC
12	Refresh Rate
17	# Banks on each SDRAM Device
36-41	Access Time from Clock for CAS# Latency 1 through 7
42	Data Width of SDRAM Components

Table 4-9 is only a subset of the defined SPD bytes on the DIMMs. For example, to program the DRB (DRAM Row Boundary) registers, the size of each row must be determined. The number of row addresses (byte 3) plus the number of column addresses (byte 4) plus the number of banks on each SDRAM device (byte 17) collectively determines the total address depth of a particular row of SDRAM. Since a row is always 64 data bits wide, the size of the row is easily determined for programming the DRB registers.

The 82443BX uses the DRAM Row Type information in conjunction with the DRAM timings set in the DRAM Timing Register to configure DRAM accesses optimally.

## 4.3.2 DRAM Address Translation and Decoding

The 82443BX supports 16 and 64 Mbit DRAM devices. The 82443BX supports a 2 KB, 4 KB and 8 KB page sizes (for SDRAM only). Page size varies per row depending on how many column address lines are used for a given row. Rows containing SDRAMs with 8 column lines have a 2 KB page size. Those with 9 column lines have a 4 KB page size and those with 10 column address lines have an 8 KB page size. In systems with EDO memory, a fixed 2 KB page size is used. The multiplexed row/column address to the DRAM memory array is provided by the MA[13:0] signals.

Row and Column address multiplexing on the MA[13:0] lines is determined on a row by row basis allowing for three possible page sizes. SDRAMs have either 8, 9 or 10 column lines allowing for 2 KB, 4 KB or 8 KB page sizes. The 82443BX supports only a 2 KB page size with EDO DRAMs. The page size is determined primarily by the row size and type (SDRAM).

When EDO DRAM is used, the 82443BX will open at most one page at a time. That is, one RAS# line will be asserted at any time. When SDRAM is used, either 2 or 4 pages can be open at any time within any row. If a row contains SDRAMs based on 16Mb technology (i.e., 12x8/9/10 devices) then two pages can be open at a time within that row. If a row contains SDRAMs based on 64Mb technology, (i.e., 14x8/9/10 devices) then four pages can be open at a time within that row.

This address multiplexing scheme is derived from Table 4-11 which depicts the addressing requirements for each of the row/column organizations for each row size. The SDRAM components used for the options shown in the table are as follows:

Option	SDRAM Component Type
2 (16MB)	2Mx8
3 (32MB)	4Mx16 or 4Mx4 (Registered DIMM only)
4 (64MB)	8Mx8
5 (128MB)	16Mx4 (Registered DIMM only)

**Note:** Both 4Mx4 and 16Mx4 SDRAM devices are supported in the form of Registered DIMMs only.

**Table 4-10. Supported Memory Configurations**

DRAM Attributes				DRAM DIMM		DRAM Addressing	MA			DRAM Size
Type	Tech	Depth	Width	SS x64	DS x64		Row	Col	Banks	Min (1 row)
EDO	4M	1M	4	1M	2M	Symmetric	10	10	NA	8 MB
		1M	4	1M	2M	Asymmetric	11	9	NA	8 MB
EDO	16M	2M	8	2M	4M	Asymmetric	11	10	NA	16 MB
		2M	8	2M	4M	Asymmetric	12	9	NA	16 MB
		2M	8	2M	4M	Asymmetric	13	8	NA	16 MB
		4M	4	4M	8M	Symmetric	11	11	NA	32 MB
		4M	4	4M	8M	Asymmetric	12	10	NA	32 MB
		4M	4	4M	8M	Asymmetric	14	8	NA	32 MB
EDO	64M	4M	16	4M	8M	Symmetric	11	11	NA	32 MB
		4M	16	4M	8M	Asymmetric	12	10	NA	32 MB
		4M	16	4M	8M	Asymmetric	14	8	NA	32 MB
		8M	8	8M	16M	Asymmetric	12	11	NA	64 MB
		16M	4	16M	32M	Symmetric	12	12	NA	128 MB
SDRAM	16M	2M	8	2M	4M	Asymmetric	12	9	2	16 MB
		2M	8	2M	4M	Asymmetric	13	8	2	16 MB
		4M	4	4M	8M	Asymmetric	12	10	2	32 MB
		4M	4	4M	8M	Asymmetric	14	8	2	32 MB
SDRAM	64M 4 bank	4M	16	4M	8M	Asymmetric	14	8	4	32 MB
		8M	8	8M	16M	Asymmetric	14	9	4	64 MB
		16M	4	16M	32M	Asymmetric	14	10	4	128 MB

Table 4-11. MA Muxing vs. DRAM Address Split

	Split	Row/ Col	SDRAM A11	BA1	BA0	A10/ AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Option 1 8 MB	12x8*	Row			11	12	14	13	22	21	20	19	18	17	16	15
		Col			11	AP			10	9	8	7	6	5	4	3
	11x9	Row				12	14	13	22	21	20	19	18	17	16	15
		Col						11	10	9	8	7	6	5	4	3
	10x10	Row					14	13	22	21	20	19	18	17	16	15
		Col					12	11	10	9	8	7	6	5	4	3
	12x8	Row			11	12	14	13	22	21	20	19	18	17	16	15
		Col							10	9	8	7	6	5	4	3
Option 2 16 MB	12x9*	Row			12	23	14	13	22	21	20	19	18	17	16	15
		Col			12	AP		11	10	9	8	7	6	5	4	3
	13x8*	Row		12	11	23	14	13	22	21	20	19	18	17	16	15
		Col		12	11	AP			10	9	8	7	6	5	4	3
	11x10	Row				23	14	13	22	21	20	19	18	17	16	15
		Col					12	11	10	9	8	7	6	5	4	3
	12x9	Row			12	23	14	13	22	21	20	19	18	17	16	15
		Col						11	10	9	8	7	6	5	4	3
Option 3 32 MB	12x10*	Row			13	23	14	24	22	21	20	19	18	17	16	15
		Col			13	AP	12	11	10	9	8	7	6	5	4	3
	14x8*	Row	13	12	11	23	14	24	22	21	20	19	18	17	16	15
		Col		12	11	AP			10	9	8	7	6	5	4	3
	11x11	Row				23	14	24	22	21	20	19	18	17	16	15
		Col				13	12	11	10	9	8	7	6	5	4	3
	12x10	Row			13	23	14	24	22	21	20	19	18	17	16	15
		Col					12	11	10	9	8	7	6	5	4	3
Option 4 64 MB	14x9*	Row	25	13	12	23	14	24	22	21	20	19	18	17	16	15
		Col		13	12	AP		11	10	9	8	7	6	5	4	3
	13x10	Row		13	25	23	14	24	22	21	20	19	18	17	16	15
		Col					12	11	10	9	8	7	6	5	4	3
	12x11	Row			25	23	14	24	22	21	20	19	18	17	16	15
		Col				13	12	11	10	9	8	7	6	5	4	3
Option 5 128 MB	14x10*	Row	25	14	13	23	26	24	22	21	20	19	18	17	16	15
		Col		14	13	AP	12	11	10	9	8	7	6	5	4	3
	13x11	Row		14	25	23	26	24	22	21	20	19	18	17	16	15
		Col				13	12	11	10	9	8	7	6	5	4	3
	12x12	Row			25	23	26	24	22	21	20	19	18	17	16	15
		Col			14	13	12	11	10	9	8	7	6	5	4	3

**NOTE:**

1. \* Indicates SDRAM organization



### 4.3.3 SDRAMC Register Programming

Several timing parameters are programmable when using SDRAM in a Intel® 440BX AGPset system. The following table summarizes the programmable parameters.

**Table 4-12. Programmable SDRAM Timing Parameters**

Parameter	SDRAMC Bit	Values (DCLKs)
CAS# Latency	CL	2,3
RAS# to CAS# Delay	SRCD	2,3
RAS# Precharge	SRP	2,3
Leadoff CS# assertion	LCT	3,4

The 82443BX can support any combination of CAS# Latency, RAS# to CAS# Delay and RAS# Precharge. Two additional bits are provided for controlling CS# assertion. The first is the Leadoff Timing bits which effectively control when the command lines (SRAS#, SCAS# and WE#) are considered valid on the interface and hence when CS# can be asserted for CPU read leadoff cycles. In the fastest timing mode, CS# can be asserted in clock three. This enables a 7 clock page hit performance with CAS# Latency two devices and one clock MD to HD delay. This field controls when the first assertion of CS# occurs for read cycles initiated by the CPU. This assertion may be for a read, row activate or precharge command. The MA lines along with the command lines (SRAS#, SCAS# and WE#) are driven in clock two, however the clock to output delay timing is slower than the other modes. Use of this mode may require a lightly loaded SDRAM interface.

### 4.3.4 DRAMT Register Programming

Various EDO timing parameters are programmable in the 82443BX. The ranges provide support for the various loading configurations at 66 MHz. These are programmed via the DRAMT (DRAM Timing) register. Only 60 ns EDO DRAMs are supported and at 66 MHz only. Thus, certain parameters are fixed and are not programmable.

**Table 4-13. EDO DRAM Timing Parameters**

Parameter	60 ns EDO Spec (ns)	66 MHz CLKs
RAS# Precharge	40	3
RAS# Pulse Width	60	5
RAS# to CAS# Delay	20–45	3
CAS# Precharge	10	1
CAS# Pulse Width	15	1
WE# Setup to CAS# Falling	0	1
WE# Hold from CAS# Falling	10	1
MA Setup to RAS#/CAS#	0	1 or 2
MA Hold from RAS#/CAS#	10	1
MD Setup to CAS#	0	1
MD Hold from CAS#	10	1

### 4.3.5 SDRAM Paging Policy

Open page arbitration is a paging policy which leaves pages open when handing off ownership of DRAM among masters, and places no restrictions on the number of rows which may have open pages at any given time.

Features include:

- 1) Pipelined arbitration allows row/bank/page operations for next cycle to occur while current DRAM access is performed.
- 2) Maintaining 2, or 4 banks open at once, in up to 8 rows at a time.

### 4.4 PCI Interface

The 82443BX Host Bridge provides a PCI bus interface that is compliant with the PCI Local Bus Specification, Revision 2.1. The implementation is optimized for high-performance data streaming when the 82443BX is acting as either the target or the initiator on the PCI bus. The 82443BX supports the conventional PCI interface referred to as PCI and AGP/PCI interface referred to as AGP for PCI transactions and AGP for PCI transactions using the AGP enhanced protocols. AGP cycles using the enhanced protocols are non-snooperable cycles targeted at DRAM.

### 4.5 AGP Interface

The 82443BX Host Bridge provides a AGP bus interface that is compliant with the *A.G.P. Interface Specification, Revision 1.0*. The 82443BX supports AGP/PCI interface referred to as AGP for PCI transactions and AGP for PCI transactions using the AGP enhanced protocols.

Table 4-13. EDO DRAM Timing Parameters

Parameter	EDO DRAM (ns)	EDO DRAM (ns)
RAS Precharge	40	55
RAS Pulse Width	10	10
RAS to CAS Delay	20-45	20-45
CAS Precharge	10	10
CAS Pulse Width	10	10
WEH Setup to CAS Falling	0	0
WEH Hold from CAS Falling	10	10
MA Setup to RAS/CAS	0	0
MA Hold from RAS/CAS	10	10
MD Setup to CAS	0	0
MD Hold from CAS	10	10

## 4.6 Data Integrity Support

The 82443BX supports ECC (Error Checking and Correcting) or EC (Error Checking) data integrity modes on the 64-bit DRAM interface. The Intel® 440BX AGPset does not support the Pentium, Pro processor bus ECC protection. This mechanism is defined in the context of the Pentium Pro processor bus specification to support building of mission critical fault-tolerant systems. The ECC generation capability is essential for the high-end multiprocessor platforms where robustness of the system depends on the complexity of the routing of the Pentium Pro processor bus signals and operational bus frequency. UP/DP platforms based on the Intel® 440BX AGPset do not have the same requirements and therefore, the 82443BX does not support Pentium Pro processor bus ECC. Both the EC mode and the ECC mode are supported with either SDRAM or EDO DRAM.

### 4.6.1 Data Integrity Mode Selection

The 82443BX supports three modes of data integrity on the memory interface.

- No ECC with Byte-wise write support
- EC Mode (Error Checking only, no correction)
- ECC Mode (Error Checking and Correcting)

These modes are selected via the DRAM Data Integrity Mode (DDIM) field in the NBXCFG register.

#### 4.6.1.1 Non-ECC (Default Mode of Operation)

After CPURST#, the 82443BX ECC control logic is set in the default mode, no data integrity or Non-ECC. This is the highest performance mode for the memory interface. Reads from memory are not delayed for error checking and correcting and writes of less than a QWord are performed without any overhead.

#### 4.6.1.2 EC Mode

When the NBXCFG Register, bits 8:7 (DDIM) are set to 01, the 82443BX DRAM Controller is in EC mode. In this mode, the 82443BX external signals MECC[7:0] are driven with a protection code on writes and are checked with an internally generated code on reads. Writes of less than a QWord are performed as read-merge-write operations.

In EC mode, the 82443BX checks for errors on reads; however, it does not correct the data that is returned to the requesting agent. Also memory scrubbing is not performed. Note that the ECC code always protects or covers an entire QWord of data. When a write of less than a QWord is initiated, the QWord which is targeted by the write must be read, the new write data merged and the entire new QWord must then be written back to memory. Partial writes (writes of less than a QWord) are slowed since this read-merge-write operation is required.

#### 4.6.1.3 ECC Mode

Selection between ECC and EC mode is performed entirely by software. If the system designer decides to select ECC protection for the 72-bit memory array (64bit memory data bus plus 8 ECC check bits), then MECC[7:0] signals carry ECC information to the 82443BX. The 82443BX generates/checks ECC as described in detail the following sections.



#### 4.6.1.4 ECC Generation and Error Detection/Correction and Reporting

The 82443BX ECC logic implements the ECC code which is compatible with the algorithm used for the Pentium Pro processor data bus ECC protection. The code is described in the Pentium Pro processor bus specification.

##### ECC Generation

When enabled, the DRAM ECC mechanism allows automatic generation of an 8-bit protection code for the 64-bit (QWord) of data during DRAM write operations. If the originally requested write operation transfers single or multiple QWords, then the ECC-protected DRAM writes are completed with no overhead. That is, ECC code is calculated and written along with the data. If the originally requested write operation transfers less than 64bits of data (less than a QWord), then the 82443BX performs a READ-MERGE-WRITE operation.

##### ECC Checking and Correction

When enabled, the ECC mechanism allows a detection of single-bit and multiple-bit errors and recovery of single-bit errors. During DRAM read operations, a full QWord of data (8 bytes) is always transferred from DRAM to the 82443BX regardless of the size of the originally requested data. Both 64-bit data and 8-bit ECC code are transferred simultaneously from DRAM to the 82443BX. The ECC checking logic in the 82443BX generates a new ECC code for the received 64-bit data and compares it with received ECC code. If a single-bit error is detected the ECC logic generates a new "recovered" 64-bit QWord with a pattern which corresponds to the originally received 8-bit ECC protection code. The corrected data is returned to the requester (the CPU, PCI master or AGP master). Additionally, the 82443BX ensures that the data is corrected in main memory so that accumulation of errors is prevented. Another error within the same QWord would result in a double-bit error which is unrecoverable. This is known as hardware scrubbing since it requires no software intervention to correct the data in memory.

##### ECC Error Reporting

For single-bit error indication, the SEF flag is set by the 82443BX in the ERRSTS (Error Status) register, along with the row number associated with the first single-bit error. The row number where the error occurred is stored in the Single-bit First Row Error (SBFRE) field in the Error Status Register. Similarly, for multiple bit error indication, the MEF flag is set in the ERRSTS register along with the row number associated with the first multiple bit error. In the case of a multi-bit error the row number is stored in the Multi-bit First Row Error (MBFRE) field in the Error Status register. In both single-bit and multiple-bit error cases, after logging the first error, the Error Status register is locked until the software writes to the respective flags and clears the SEF and MEF bits. This error condition can also be optionally reported to the system via the SERR# mechanism. This functionality is controlled by the ERRCMD (Error Command) register. When bit 1 of the Error Command register is set to 1, an occurrence of a multiple bit error is signaled by the assertion of SERR#. When bit 0 of the Error Command register is set to 1, an occurrence of a single bit error is signaled by the assertion of SERR#. Reporting of single bit errors via SERR# is not critical since these errors are not only corrected as data is delivered to the requester and the error is automatically corrected in memory. However, system software may monitor the occurrence of single bit errors to indicate the presence of an unreliable DIMM when single bit errors frequently occur.

**Note:** Any ECC errors received during initialization should be ignored.

After a single-bit correctable ECC error has occurred, it is reported either via hardware mechanism or via software mechanism (periodic polling of the ERRSTS register). After a single bit error has occurred, the 82443BX then initiates a write to the location where the error occurred with the

corrected data. This feature is known as hardware scrubbing and eliminates the need for software scrubbing routines. Note that information in the ERRSTS register can be used later to point to a faulty DRAM DIMM if the single-bit errors continually occur during access to that DIMM.

Multi-bit uncorrectable errors are fatal system errors and will cause the 82443BX to assert the SERR# signal, if bit 1 of the ERRCMD register is set to 1. When an uncorrectable error is detected, the 82443BX will latch the row # where the error occurred Multi-bit First Row Error (MBFRE) bit in the ERRSTS register. This information can be used later to point to a faulty DRAM DIMM.

**Note:** When ECC is enabled, the whole DRAM array MUST be first initialized by doing writes before the DRAM read operations can be performed. This will establish the correlation between 64-bit data and associated 8-bit ECC code which does not exist after power-on.

#### 4.6.1.5 Optimum ECC Coverage

Note that the 82443BX requirement is only that the memory array is 72 bits (64 bit memory data bus plus 8 ECC check bits) wide to select ECC or EC protection. The 82443BX does not assume any specific configuration or ordering of memory bits.

#### 4.6.2 DRAM ECC Error Signaling Mechanism

When ECC is enabled and ERRCMD is used to set SERR# functionality, ECC errors are signaled to the system via the SERR# pin. The 82443BX can be programmed to signal SERR# on uncorrectable errors, correctable errors, or both. The type of error condition is latched until cleared by software (regardless of SERR# signaling).

When a single-bit error is detected, the offending DRAM row ID is latched in the Single-bit First Row Error (SBFRE) field in the ERRSTS register and the SEF (Single-bit Error Flag) bit is set to 1. The latched row value is held until software explicitly clears the error status flag (SEF bit). When a multiple-bit (uncorrectable) error is detected, the offending DRAM row ID is latched in the Multi-bit First Row Error (MBFRE) field in the ERRSTS register and the MEF (Multi-bit Error Flag) is set to 1. The latched row value is held until software explicitly clears the error status flag (MEF bit).

#### 4.6.3 CPU Bus Integrity

The Intel® 440BX AGPset does not support the Pentium Pro processor bus integrity mechanisms. It does not provide support for data protection via ECC, and address/request signal protection via parity, nor does it support bus protocol error checking or reporting.

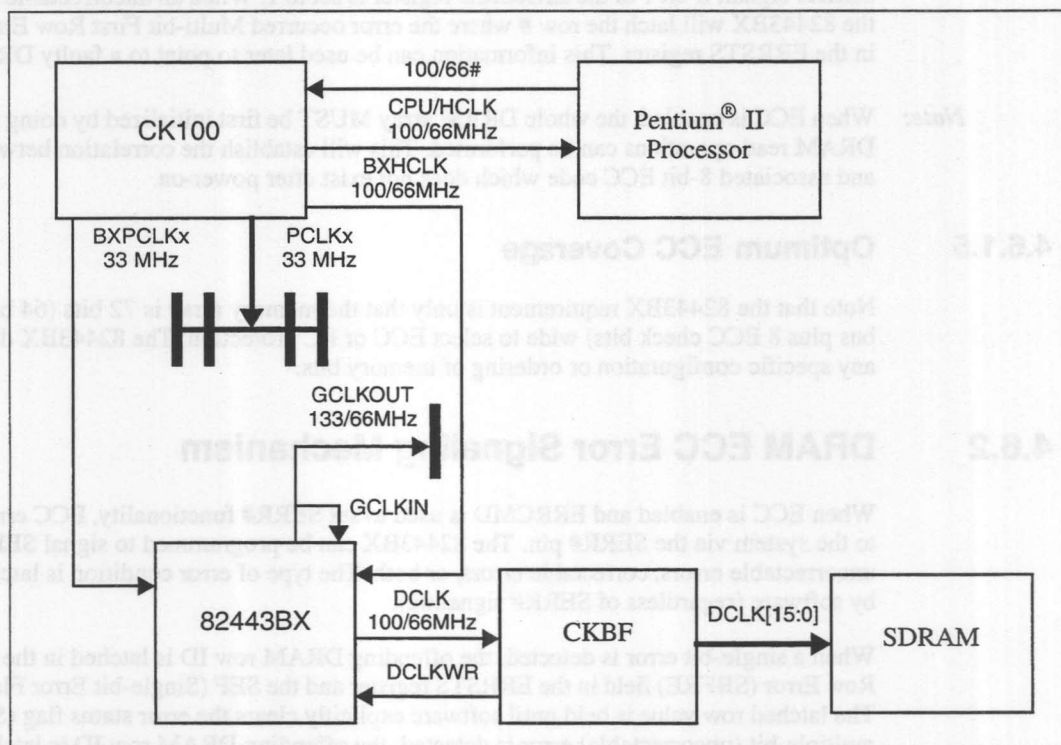
#### 4.6.4 PCI Bus Integrity

The 82443BX implements Parity generation on the PAR pin as defined by the PCI Rev. 2.1 Specification for both Primary and Secondary PCI bus. The 82443BX does not contain the PERR# pin, however the 82443BX will check and report data parity errors on either the Primary or Secondary PCI buses. Data and address parity errors are reported on SERR#.

## 4.7 System Clocking

Figure 4-6 shows the clock architecture for a typical Intel® 440BX AGPset system.

**Figure 4-6. Typical Intel® 440BX AGPset System Clocking**



## 4.8 Power Management

This section focuses on the 82443BX power management features only. The PIIX4E datasheet along with this section provide the complete system power management description.

### 4.8.1 Overview

#### Power Management Features Supported by the 82443BX

- Suspend Resume
- Clock Control
- SDRAM Power Down Mode
- SMRAM
- ACPI and PCI-PM



### Low-Power Modes Supported by the 82443BX

The 82443BX supports a variety of system-wide low power modes using the following functions:

- Hardware interface with PIIX4E is used to indicate:
  - Suspend mode entry.
  - Resume from suspend.
  - Whether to reset “resume logic” during resume from Suspend to Disk (STD).
  - Whether to automatically switch from suspend to normal refresh
- Automatic transition from normal to suspend refresh.
- Optional automatic transition from suspend to normal refresh.
- Optional CPU reset during resume from Power On Suspend (POS).
- Variety of Suspend refresh types:
  - Self Refresh for SDRAMs.
  - Optional Self Refresh for EDO.
  - Optional CAS Before RAS (CBR) refresh for EDO. Integrated Ring oscillator is used to provide the time base for the associated logic.
  - Programmable slow refresh, relevant for CBR refresh only.
- I/O pins isolation to significantly reduce power consumption while in POS and STR modes.

Based on the above functions, the 82443BX distinguishes the following system-wide low power modes:

- STR and POS suspend entry and exit are generally handled in the same manner. The following exceptions are related to POS:
  - POS resume sequence may or may not include CPU reset. STR, with PCIRST# active always includes CPU reset.
  - POS resume sequence requires hardware transition from suspend to normal refresh. STR, with PCIRST# active requires software initiated transition.
- STD resume is handled the same as power on sequence, including complete reset of 82443BX state.

### Clock Control Functions Supported by 82443BX

- Internal clock gating: this function allows the 82443BX to gate the clock to the majority of its logic while there is no pending events to handle.
- The Primary PCI bus includes the support of the CLKRUN#, which enables the PIIX4E to dynamically disable the primary PCICLK and for the 82443BX and PCI peripheral to re-enable the clock when it is needed to perform a transaction.
- When an AGP port is not available on the system, a strapping option allows the 82443BX to permanently disable all clocks associated with AGP logic.

### SDRAM Power Down Mode

The 82443BX supports SDRAM power down mode. The 82443BX also provides a capability to dynamically enter the SDRAM into low power mode when DRAM rows are idle and resume DRAM activity when transactions request the access to DRAM.

### SMRAM Functions

The 82443BX provides the normal SMRAM range mapping, in the areas below 1MB, as well as extended SMRAM ranges that are mapped in cacheable ranges above 1MB. In addition, the 82443BX provides the normal control mechanism to initialize, close for data accesses and lock the SMRAM range.

### Summary of ACPI Functions

The 82443BX provides an optional decoding of pm2\_control register in IO port 22h. This IO port can be used to disable the 82443BX arbiters for PCI and AGP initiated cycles.

### Desktop vs. Mobile Power Management Functions

In general, all mobile functions of the 82443BX are available in the desktop configuration. Due to system design limitations, however, certain functions are not supported in a desktop environment (i.e., POS/C3 state).

In Mobile systems, when system exits low power modes such as deep sleep or POS, the AGP devices should not generate a request, using AGP semantics, for a duration of at least 33 usec.

### System Power Modes

Table 4-14 provides an overview of how the above features map into system-wide low power modes.

Table 4-14. Low Power Mode

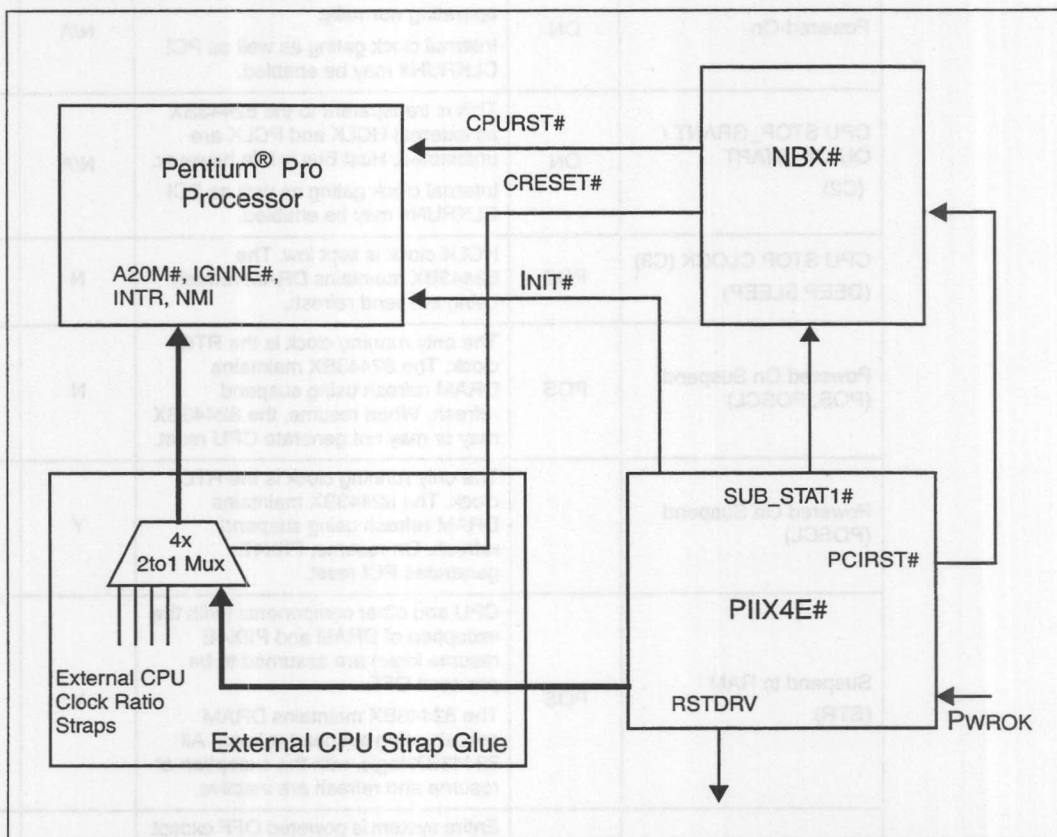
System Suspend State	82443BX State	Description	POS Exit PCIRST	External Clk HCLK PCLK	
				HCLK	PCLK
Powered-On	ON	The 82443BX is fully on and operating normally. Internal clock gating as well as PCI CLKRUN# may be enabled.	N/A	Active	Active
CPU STOP_GRANT / QUICK_START (C2)	ON	This is transparent to the 82443BX as external HCLK and PCLK are unaffected. Host Bus is Idle however. Internal clock gating as well as PCI CLKRUN# may be enabled.	N/A	Active	Active
CPU STOP CLOCK (C3) (DEEP SLEEP)	POS	HCLK clock is kept low. The 82443BX maintains DRAM refresh using suspend refresh.	N	Low	Low or Active
Powered On Suspend (POS, POSCL)	POS	The only running clock is the RTC clock. The 82443BX maintains DRAM refresh using suspend refresh. When resume, the 82443BX may or may not generate CPU reset.	N	Low	Low
Powered On Suspend (POSCL)		The only running clock is the RTC clock. The 82443BX maintains DRAM refresh using suspend refresh. On resume, PIIX4E generates PCI reset.	Y	Low	Low
Suspend to RAM (STR)	POS	CPU and other components (with the exception of DRAM and PIIX4E resume logic) are assumed to be powered OFF. The 82443BX maintains DRAM refresh using suspend refresh. All 82443BX logic, with the exception of resume and refresh are inactive.	Y	Low	Low
Suspend -to-Disk (STD) or Powered-Off	OFF	Entire system is powered OFF except for PIIX4E resume and RTC wells. Upon resume, the 82443BX resets its entire state.	N/A	X	X



## 4.8.2 82443BX Reset

The 82443BX reset function is an integral part of the suspend resume functions. The 82443BX supports the normal reset function in a desktop platform, as well as the various power-up reset and resume reset functions in the mobile platform. In this section, the power-up reset is described. The resume from suspend sequences are described in the following section.

**Table 4-15. AGPset Reset**



**Table 4-16. Reset Signals**

Signal	Asserted with PCIRST#	System Devices or Buses Affected	Signal Source	Description
PCIRST#	-	PCI bus, 82443BX NB, PIIX4E	PIIX4E	PCIRST# is used in power-up sequence as well as resume from STR or STD.
CPURST#	Always	CPU	82443BX	CPU reset signal. CPURST# pin resides in 82443BX.
RSTDRV	Always	ISA bus / X-Bus devices	PIIX4E	ISA bus reset. Directly derived from PCIRST#. Resides in PIIX4E main voltage well.
SUS_STAT#	N/A		PIIX4E only	SUS_STAT# signals a suspend mode entry and exit. Both signals originate from PIIX4E in its suspend voltage well.
INIT#	No	CPU	PIIX4E	CPU Soft Reset generated by PIIX4E.

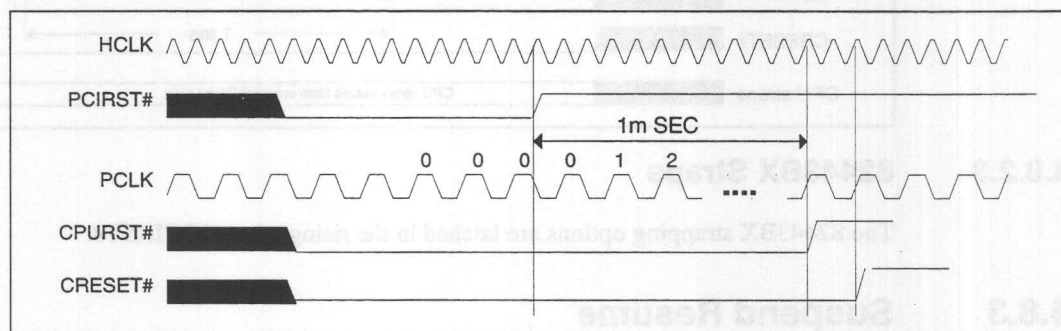
### 4.8.2.1 CPU Reset

The CPU reset is generated by the 82443BX in the following case:

- CPURST# is always asserted if PCIRST# is asserted.
- CPURST# is asserted during resume sequence from POS CRst\_En= 1.

The 82443BX deasserts CPURST# 1 ms after detecting the rising edge of PCIRST#. The CPURST# is synchronous to host bus clock.

**Figure 4-7. Reset CPURST# in a Desktop or Mobile System When PCIRST# Asserted**



PCIRST# must be asserted when the system resumes from low power mode of which power is removed, including resume from STR or STD and power up sequence. In these cases, CPURST# is activated with the assumption that CPU power is removed as well and in order to enforce correct resume sequence.

When resuming from POS, the PCIRST# and CPURST# are typically not used, to speed up the resume sequence. The option to reset the CPU, in this case, is available by using the CRst\_En configuration bit option.

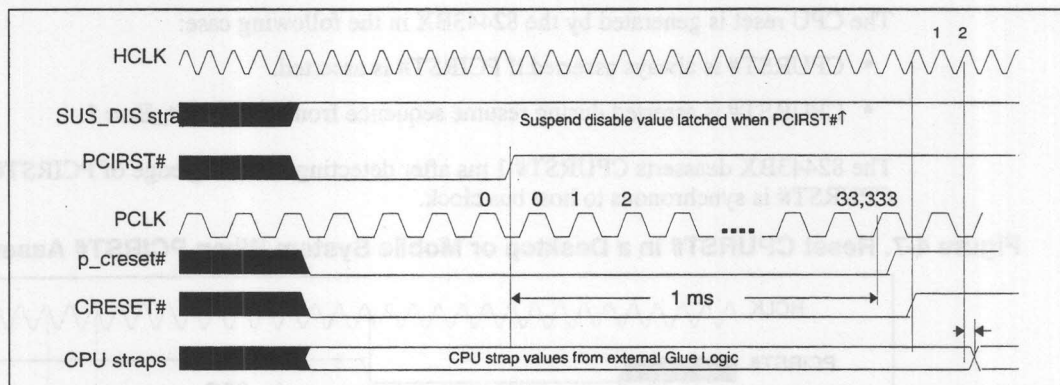
When the user performs a soft reset, the PIIX4E drives SUSTAT# to the 82443BX. This forces the 82443BX to switch to a suspend refresh state. When the BIOS attempts to execute cycles to DRAM, the 82443BX will not accept these cycles because it believes that it is in a suspend state. After coming out of reset, software must set the Normal refresh enable bit (bit4, Power Management Control register at Offset 7Ah) in the 82443BX before doing an access to memory.

### 4.8.2.2 CPU Clock Ratio Straps

The Pentium Pro processors require their internal clock ratio to be set up via strapping pins multiplexed onto signals A20M#, IGNE#, INTR, and NMI. These signals should reflect the strapping values during the deasserted edge of CPURST# signal and be held stable for between 2 to 20 clocks. HCLKs after CPURST# is deasserted.

The 82443BX is designed to support CPU strapping options with external logic, when PIIX4E is used. Figure 4-8 illustrates the strapping pin timing when using the external glue logic (necessary for PIIX4E). The external mux is switched via the CRESET# signal which is a 2 clock delayed version of CPURST#.

Figure 4-8. External Glue Logic Drives CPU Clock Ratio Straps



#### 4.8.2.3 82443BX Straps

The 82443BX strapping options are latched in the rising edge of PCIRST#.

### 4.8.3 Suspend Resume

#### 4.8.3.1 Suspend Resume protocols

The suspend resume sequences are indicated to the 82443BX by the PIIX4E, using SUS\_STAT#, and PCIRST#. In addition, the 82443BX contains NREF\_EN and CRst\_En configuration bits that participate in the suspend resume sequences. As a result of suspend resume, the 82443BX performs the following activities: Changing its refresh mode, performing internal and CPU reset and Isolate or re-enable normal IO buffers.

Table 4-17. Suspend / Resume Events and Activities

State	SUSTAT#	PCIRST#	CrstEn	RESET	REFRESH	IO BUFFERS
ON	assert	inactive	-	-	switch to suspend refresh	isolate
POSCL/STR	deassert	active	-	reset exclude resume/ref logic	suspend refresh NREF_EN remains inactive	enable
POS	deassert	inactive	0	no resets	auto switch to normal ref NREF_EN is set	enable
POSCCL	deassert	inactive	1	reset CPU only	auto switch to normal ref NREF_EN is set	enable

#### 4.8.3.2 Suspend Refresh

##### Suspend Refresh Modes

The 82443BX supports suspend refresh by providing a mechanism to transition in and out of suspend. The supported suspend refresh types are:

- Self Refresh when SDRAM are used
- Self Refresh when EDO -DRAMs are used
- CBR Refresh when EDO-DRAMs are used



### SDRAM Suspend Refresh

When the 82443BX is configured for 3 DIMMs, six CKE signals are provided. When the 82443BX is configured for 4 DIMMs, a single GCKE (global CKE) is provided to allow an external device to correctly drive the external CKE signals to the SDRAM devices. An additional 3 DIMM configuration is where only CKE0 is provided. A detailed description of the DRAM signal functions is given in the Chapter 2, "Signal Description".

For the Registered DIMMs the CKE function is not supported. The stacking technology used for registered DIMMs prohibits the use of the CKE function. For registered DIMMs, components are stacked on top of one another. The stacked components are **physically** in the same row, but **logically** in separate rows. The stacked components connect all pins together, except for the CS# pin, in order to address components in different rows. Since the CKE pins for the components are connected together, and the components are **logically** in different rows, the CKE function is not supported.

**Table 4-18. SDRAM Suspend Refresh Configuration Modes**

MM CONFIG	SDRAM PWR	FUNCTION
0	0	3 DIMM, CKE[5:0] driven, self-refresh entry staggered. SDRAM dynamic power down available.
1	X	3 DIMM, CKE0 only, self-refresh entry not staggered. SDRAM dynamic power down unavailable.
0	1	4 DIMM, GCKE only, self-refresh entry staggered. SDRAM dynamic power down unavailable.

### EDO DRAM Suspend Refresh

The 82443BX NB supports two modes of EDO refresh during suspend: CAS-before-RAS and Self-refresh. The refresh mode is dependent on the Suspend Refresh type bit (SRT) in the Miscellaneous Control Register.

## 4.8.4 Clock Control Functions

The 82443BX implements an independent Clock Gating power savings feature to reduce its own average power consumption. The 82443BX clock gating functions works along with the primary PCI bus CLKRUN# function.

The Clock Gating function is enabled by setting the GCLKEN Configuration bit. This function default value is 0. The AGP interface's clock domain can be permanently disabled by the AGP\_DIS configuration bit. This allows further power savings in systems that AGP is not used.

### CLKRUN Clocking States

There are three states in the CLKRUN# protocol:

- **Clock Running:** The clock is running and the bus is operational.
- **Clock Stop Request:** The central resource has indicated on the CLKRUN# line that the clock is about to stop.
- **Clock Stopped:** The clock is stopped with CLKRUN# being monitored for a restart.

## 4.8.5 SDRAM Power Down Mode

The 82443BX supports a SDRAM power down mode to minimize SDRAM power usage. The 82443BX controls the SDRAM power mode per row, when all banks in a given row are idle, the associated CKE signal is deasserted. When a powered down row address is requested, the associated CKE is asserted.

## 4.8.6 SMRAM

### SMRAM ranges

The 82443BX supports the use of main memory as System Management RAM (SMRAM) enabling the use of System Management Mode. There are two SMRAM options: Compatible SMRAM (C\_SMRAM) and Extended SMRAM (E\_SMRAM). System Management RAM (SMRAM) space provides a memory area that is available for the SMI handler's and code and data storage. This memory resource is normally hidden from the operating system so that the processor has immediate access to this memory space upon entry to SMM. 82443BX provides three SMRAM options:

- Below 1 MB option that supports compatible SMI handlers.
- Above 1 MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional larger write-back cacheable T\_SEG area from 128KB to 1MB in size above 1 MB that is reserved from the highest area in system DRAM memory. The above 1 MB solutions require changes to compatible SMRAM handlers code to properly execute above 1 MB.

### Compatible SMRAM (C\_SMRAM)

This is the traditional SMRAM feature supported in Intel AGPsets. When this function is enabled via C\_BASE\_SEG[2:0]=010 and G\_SMRAME=1 of the SMRAMC register, the 82443BX reserves 000A0000h through 000BFFFFh (A and B segments) of the main memory for use as non-cacheable SMRAM.

The SMI handler can set the CLS bit to enable data accesses to aliased memory space, while code fetches access the SMRAM space.

### Extended SMRAM (E\_SMRAM)

This feature in the 82443BX extend the SMRAM space up to 1 MB and provide write-back cacheability.

The TSEG size is 128 KBs, 256 KBs, 512 KBs or 1 MB, as defined by TSEG\_SZ[1:0] of the SMRAMC register.

The CPU can access these memory ranges by one of the following mechanisms:

- The processor can access SMRAM while in the SMM mode. A processor access to while not in SMM and with while the D\_OPN bit is reset will be forwarded to PCI bus and a status bit is set in the SMRAMC register.
- The processor can access SMRAM while the D\_OPN bit is set.

## 5.1 82443BX Pinout

Figure 5-1 and Figure 5-2 show the ball footprint of the 82443BX package. These figures represent the pinout by ball number. For an alphabetical list of the pinout by signal name refer to Table 5-1.

## 5.1 82443BX Pinout



Figure 5-1. 82443BX Pinout (Top View-left side)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VSS	AD20	PCIRST#	AD25	AD29	PREQ0#	HD56#	HD62#	HD55#	HD54#	HD49#	HD47#	HD40#
B	VCC	PCLKIN	AD22	AD27	AD28	PHOLD#	HD50#	HD61#	HD63#	HD53#	HD48#	HD42#	HD36#
C	AD19	REFVCC	AD21	C/BE3#	VSS	AD31	PREQ1#	HD52#	VSS	HD60#	HD59#	HD51#	HD44#
D	AD16	AD18	AD17	AD23	AD26	PHLDA#	PGNT1#	PREQ3#	HD58#	PREQ4#	HD46#	HD41#	HD39#
E	IRDY#	FRAME#	VSS	C/BE2#	AD24	AD30	PGNT0#	PGNT3#	PGNT4#	PGNT2#	HD57#	VSS	HD45#
F	SERR#	PLOCK#	DEVSEL#	STOP#	TRDY#	VSS	VCC	VSS	VCC	PREQ2#			
G	AD13	AD14	C/BE1#	AD15	PAR	VCC							
H	AD8	AD7	AD10	AD12	AD11	VSS							
J	AD5	AD6	VSS	C/BE0#	AD9	VCC							
K	SBA0	AD1	AD3	AD2	AD4	AD0							
L	ST2	ST1	GGNT#	ST0	GREQ#								
M	SBA2	SBA1	PIPE#	RBF#	VSS								
N	VSS	SBA3	SBSTB	AGPREF	GCLKIN								
P	VCC	SBA4	SBA6	SBA5	GCLKO								
R	SBA7	GAD31	GAD29	GAD30	VSS								
T	GAD27	GAD26	GAD24	GAD25	ADSTB_B								
U	GAD23	GC/BE3#	GAD22	GAD21	GAD19	GAD28							
V	GAD20	GAD17	VSS	GC/BE2#	GIRDY#	VCC							
W	GAD16	GAD18	GFRAME#	GTRDY#	GDEVSEL#	VSS							
Y	GSTOP#	GPAR	GAD15	GC/BE1#	GAD14	VCC							
AA	GAD13	GAD12	GAD10	GAD11	GAD9	VSS	VCC	VSS	VCC	MECC1			
AB	GAD8	GC/BE0#	VSS	GAD7	GAD0	MD34	MD5	MD8	MD9	MD12	MD46	VSS	SCASB#
AC	GAD6	ADSTB_A	GAD5	CLKRUN#	MD32	MD35	MD6	MD39	MD10	MD13	MD47	WEB#	DQMA1
AD	GAD4	GAD3	GAD2	SUSTAT#	VSS	MD3	MD37	MD40	VSS	MD44	MD15	MECC5	DQMA0
AE	VCC	GAD1	WSC#	MD1	MD33	MD4	MD38	MD42	MD11	MD45	MECC0	WEA#	DQMB1
AF	VSS	VCC	BXPWROK	MD0	MD2	MD36	MD7	MD41	MD43	MD14	MECC4	SCASA#	VSS

VCC	VSS	VCC
VSS	VCC	VSS
VCC	VSS	VSS
VCC	VSS	VSS
VSS	VCC	VSS
VCC	VSS	VCC

**NOTES:**

- The following signals are multiplexed. See the following Alphabetical pin list for details.
  - CSA[5:0]# is multiplexed with RASA[5:0]#; CSB[5:0]# is multiplexed with RASB[5:0]#
  - CKE[3:2] is multiplexed with CSA[7:6]#; CKE[5:4] is multiplexed with CSB[7:6]#; CKE1 is multiplexed with GCKE; CKE0 is multiplexed with FENA
  - DQMA[7:0] is multiplexed with CASA[7:0]#; DQMB[5,1] is multiplexed with CASB[5,1]#

Figure 5-2. 82443BX Pinout (Top View-right side)

14	15	16	17	18	19	20	21	22	23	24	25	26	
VSS	HD33#	HD31#	HD27#	HD19#	HD20#	HD10#	HD6#	HD3#	HA29#	HA24#	HA22#	VSS	A
HD43#	HD32#	HD29#	HD25#	HD21#	HD18#	HD12#	HD8#	HD0#	CPURST#	HA27#	HA20#	BREQ0#	B
HD37#	HD28#	HD26#	HD22#	VSS	HD17#	HD7#	HD5#	VSS	HA26#	HA28#	HA23#	HA21#	C
HD34#	HD35#	HD30#	HD24#	HD16#	HD15#	HD14#	HD4#	HD1#	HA31#	HA25#	HA18#	HA19#	D
HD38#	VSS	GTLREFB	HD23#	HD13#	HD11#	HD9#	HD2#	HA30#	HA15#	VSS	HA17#	HA16#	E
			VTTB	VCC	VSS	VCC	VSS	HA11#	HA12#	HA13#	HA14#	HA8#	F
							VCC	HA10#	HA5#	HA7#	HA3#	HA9#	G
							VSS	HA4#	HA6#	BNR#	HTRDY#	BPRI#	H
							VCC	HREQ0#	HREQ1#	VSS	HREQ4#	DEFER#	J
							ADS#	HLOCK#	DRDY#	HREQ2#	HREQ3#	RS0#	K
								HITM#	DBSY#	HIT#	RS2#	RS1#	L
								VSS	GTLREFA	VTTA	TESTIN#	CRESET#	M
								VCC	HCLKIN	VSS	MD31	VCC	N
								NC	MD30	MD62	MD63	VSS	P
								VSS	MD60	MD28	MD29	MD61	R
								MD25	MD26	MD57	MD58	MD27	T
							MD59	MD54	MD24	MD23	MD55	MD56	U
							VCC	MD51	MD52	VSS	MD53	MD22	V
							VSS	MD50	MD18	MD19	MD21	MD20	W
							VCC	MECC7	MD48	MD16	MD17	MD49	Y
			SRASB#	VCC	VSS	VCC	VSS	DQMA6	MECC2	DQMA7	MECC6	MECC3	AA
CSA0#	VSS	MAA1	MAB3#	MAB6#	MAB7#	MAB10	DCLKO	NC	CSB5#	VSS	VSS	DQMA3	AB
DQMA5	CSA3#	MAB1#	MAA3	MAA7	MAA8	MAB9#	MAA12	CKE0	CKE4	CSB3#	DQMA2#	CSB4#	AC
DQMB5	CSA4#	MAB0#	MAB2#	VSS	MAB5#	MAA10	MAB12#	VSS	CKE3	CSB1#	DCLKWR	CSB2#	AD
DQMA4	CSA2#	CSA5#	MAA2	MAB4#	MAA5	MAA9	MAB11#	NC	NC	CKE2	CSB0#	VCC	AE
VCC	CSA1#	SRASA#	MAA0	MAA4	MAA6	MAB8#	MAA11	MAB13	CKE1	CKE5	MAA13	VSS	AF

**NOTES:**

1. The following signals are multiplexed. See the following Alphabetical pin list for details.
  - d. CSA[5:0]# is multiplexed with RASA[5:0]#; CSB[5:0]# is multiplexed with RASB[5:0]#
  - e. CKE[3:2] is multiplexed with CSA[7:6]#; CKE[5:4] is multiplexed with CSB[7:6]#; CKE1 is multiplexed with GCKE; CKE0 is multiplexed with FENA
  - f. DQMA[7:0] is multiplexed with CASA[7:0]#; DQMB[5,1] is multiplexed with CASB[5,1]#

Table 5-1. 82443BX Alphabetical BGA Pin List (Sheet 1 of 4)

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
AD0	K6	C/BE2#	E4	GAD0	AB5
AD1	K2	C/BE3#	C4	GAD1	AE2
AD2	K4	CKE0/FENA	AC22	GAD2	AD3
AD3	K3	CKE1/GCKE	AF23	GAD3	AD2
AD4	K5	CKE2/CSA6	AE24	GAD4	AD1
AD5	J1	CKE3/CSA7	AD23	GAD5	AC3
AD6	J2	CKE4/CSB6	AC23	GAD6	AC1
AD7	H2	CKE5/CSB7	AF24	GAD7	AB4
AD8	H1	CLKRUN#	AC4	GAD8	AB1
AD9	J5	CPURST#	B23	GAD9	AA5
AD10	H3	CRESET#	M26	GAD10	AA3
AD11	H5	CSA0#/RASA0#	AB14	GAD11	AA4
AD12	H4	CSA1#/RASA1#	AF15	GAD12	AA2
AD13	G1	CSA2#/RASA2#	AE15	GAD13	AA1
AD14	G2	CSA3#/RASA3#	AC15	GAD14	Y5
AD15	G4	CSA4#/RASA4#	AD15	GAD15	Y3
AD16	D1	CSA5#/RASA5#	AE16	GAD16	W1
AD17	D3	CSB0#/RASB0#	AE25	GAD17	V2
AD18	D2	CSB1#/RASB1#	AD24	GAD18	W2
AD19	C1	CSB2#/RASB2#	AD26	GAD19	U5
AD20	A2	CSB3#/RASB3#	AC24	GAD20	V1
AD21	C3	CSB4#/RASB4#	AC26	GAD21	U4
AD22	B3	CSB5#/RASB5#	AB23	GAD22	U3
AD23	D4	DBSY#	L23	GAD23	U1
AD24	E5	DCLKO	AB21	GAD24	T3
AD25	A4	NC	AB22	GAD25	T4
AD26	D5	DCLKWR	AD25	GAD26	T2
AD27	B4	DEFER#	J26	GAD27	T1
AD28	B5	DEVSEL#	F3	GAD28	U6
AD29	A5	DQMA0/CASA0#	AD13	GAD29	R3
AD30	E6	DQMA1/CASA1#	AC13	GAD30	R4
AD31	C6	DQMA2/CASA2#	AC25	GAD31	R2
ADS#	K21	DQMA3/CASA3#	AB26	GC/BE0#	AB2
ADSTB_A	AC2	DQMA4/CASA4#	AE14	GC/BE1#	Y4
ADSTB_B	T5	DQMA5/CASA5#	AC14	GC/BE2#	V4
AGPREF	N4	DQMA6/CASA6#	AA22	GC/BE3#	U2
BNR#	H24	DQMA7/CASA7#	AA24	GCLKIN	N5
BPRI#	H26	DQMB1/CASB1#	AE13	GCLKO	P5
BREQ0#	B26	DQMB5/CASB5#	AD14	GDEVSEL#	W5
C/BE0#	J4	DRDY#	K23	GFRAME#	W3
C/BE1#	G3	FRAME#	E2	GGNT#	L3



Table 5-1. 82443BX Alphabetical BGA Pin List (Sheet 2 of 4)

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
GIRDY#	V5	HD4#	D21	HD45#	E13
GPARG	Y2	HD5#	C21	HD46#	D11
GREQ#	L5	HD6#	A21	HD47#	A12
GSTOP#	Y1	HD7#	C20	HD48#	B11
GTLREFA	M23	HD8#	B21	HD49#	A11
GTLREFB	E16	HD9#	E20	HD50#	B7
GTRDY#	W4	HD10#	A20	HD51#	C12
HA3#	G25	HD11#	E19	HD52#	C8
HA4#	H22	HD12#	B20	HD53#	B10
HA5#	G23	HD13#	E18	HD54#	A10
HA6#	H23	HD14#	D20	HD55#	A9
HA7#	G24	HD15#	D19	HD56#	A7
HA8#	F26	HD16#	D18	HD57#	E11
HA9#	G26	HD17#	C19	HD58#	D9
HA10#	G22	HD18#	B19	HD59#	C11
HA11#	F22	HD19#	A18	HD60#	C10
HA12#	F23	HD20#	A19	HD61#	B8
HA13#	F24	HD21#	B18	HD62#	A8
HA14#	F25	HD22#	C17	HD63#	B9
HA15#	E23	HD23#	E17	HIT#	L24
HA16#	E26	HD24#	D17	HITM#	L22
HA17#	E25	HD25#	B17	HLOCK#	K22
HA18#	D25	HD26#	C16	HREQ0#	J22
HA19#	D26	HD27#	A17	HREQ1#	J23
HA20#	B25	HD28#	C15	HREQ2#	K24
HA21#	C26	HD29#	B16	HREQ3#	K25
HA22#	A25	HD30#	D16	HREQ4#	J25
HA23#	C25	HD31#	A16	HTRDY#	H25
HA24#	A24	HD32#	B15	IRDY#	E1
HA25#	D24	HD33#	A15	MAA0	AF17
HA26#	C23	HD34#	D14	MAA1	AB16
HA27#	B24	HD35#	D15	MAA2	AE17
HA28#	C24	HD36#	B13	MAA3	AC17
HA29#	A23	HD37#	C14	MAA4	AF18
HA30#	E22	HD38#	E14	MAA5	AE19
HA31#	D23	HD39#	D13	MAA6	AF19
HCLKIN	N23	HD40#	A13	MAA7	AC18
HD0#	B22	HD41#	D12	MAA8	AC19
HD1#	D22	HD42#	B12	MAA9	AE20
HD2#	E21	HD43#	B14	MAA10	AD20
HD3#	A22	HD44#	C13	MAA11	AF21

Table 5-1. 82443BX Alphabetical BGA Pin List (Sheet 3 of 4)

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
MAA12	AC21	MD25	T22	MECC2	AA23
MAA13	AF25	MD26	T23	MECC3	AA26
MAB0#	AD16	MD27	T26	MECC4	AF11
MAB1#	AC16	MD28	R24	MECC5	AD12
MAB2#	AD17	MD29	R25	MECC6	AA25
MAB3#	AB17	MD30	P23	MECC7	Y22
MAB4#	AE18	MD31	N25	NC	P22
MAB5#	AD19	MD32	AC5	NC	AE22
MAB6#	AB18	MD33	AE5	NC	AE23
MAB7#	AB19	MD34	AB6	PAR	G5
MAB8#	AF20	MD35	AC6	PCIRST#	A3
MAB9#	AC20	MD36	AF6	PCLKIN	B2
MAB10	AB20	MD37	AD7	PGNT0#	E7
MAB11#	AE21	MD38	AE7	PGNT1#	D7
MAB12#	AD21	MD39	AC8	PGNT2#	E10
MAB13	AF22	MD40	AD8	PGNT3#	E8
MD0	AF4	MD41	AF8	PGNT4#	E9
MD1	AE4	MD42	AE8	PHLDA#	D6
MD2	AF5	MD43	AF9	PHOLD#	B6
MD3	AD6	MD44	AD10	PIPE#	M3
MD4	AE6	MD45	AE10	PLOCK#	F2
MD5	AB7	MD46	AB11	PREQ0#	A6
MD6	AC7	MD47	AC11	PREQ1#	C7
MD7	AF7	MD48	Y23	PREQ2#	F10
MD8	AB8	MD49	Y26	REQ3#	D8
MD9	AB9	MD50	W22	PREQ4#	D10
MD10	AC9	MD51	V22	RBF#	M4
MD11	AE9	MD52	V23	REFVCC	C2
MD12	AB10	MD53	V25	RS0#	K26
MD13	AC10	MD54	U22	RS1#	L26
MD14	AF10	MD55	U25	RS2#	L25
MD15	AD11	MD56	U26	SBSTB	N3
MD16	Y24	MD57	T24	SBA0	K1
MD17	Y25	MD58	T25	SBA1	M2
MD18	W23	MD59	U21	SBA2	M1
MD19	W24	MD60	R23	SBA3	N2
MD20	W26	MD61	R26	SBA4	P2
MD21	W25	MD62	P24	SBA5	P4
MD22	V26	MD63	P25	SBA6	P3
MD23	U24	MECC0	AE11	SBA7	R1
MD24	U23	MECC1	AA10	SCASA#	AF12

Table 5-1. 82443BX Alphabetical BGA Pin List (Sheet 4 of 4)

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
SCASB#	AB13	VCC	V21	VSS	N14
SERR#	F1	VCC	Y6	VSS	N15
SRASA#	AF16	VCC	Y21	VSS	N24
SRASB#	AA17	VCC	AA7	VSS	P12
ST0	L4	VCC	AA9	VSS	P13
ST1	L2	VCC	AA18	VSS	P14
ST2	L1	VCC	AA20	VSS	P15
STOP#	F4	VCC	AE1	VSS	P26
BXPWROK	AF3	VCC	AE26	VSS	R5
SUSTAT#	AD4	VCC	AF2	VSS	R11
TESTIN#	M25	VCC	AF14	VSS	R13
TRDY#	F5	VSS	A1	VSS	R14
VCC	B1	VSS	A14	VSS	R16
VCC	F7	VSS	A26	VSS	R22
VCC	F9	VSS	C5	VSS	T12
VCC	F18	VSS	C9	VSS	T15
VCC	F20	VSS	C18	VSS	V3
VCC	G6	VSS	C22	VSS	V24
VCC	G21	VSS	E3	VSS	W6
VCC	J6	VSS	E12	VSS	W21
VCC	J21	VSS	E15	VSS	AA6
VCC	L11	VSS	E24	VSS	AA8
VCC	L13	VSS	F6	VSS	AA19
VCC	L14	VSS	F8	VSS	AA21
VCC	L16	VSS	F19	VSS	AB3
VCC	M12	VSS	F21	VSS	AB12
VCC	M15	VSS	H6	VSS	AB15
VCC	N11	VSS	H21	VSS	AB24
VCC	N16	VSS	J3	VSS	AB25
VCC	N22	VSS	J24	VSS	AD5
VCC	N26	VSS	L12	VSS	AD9
VCC	P1	VSS	L15	VSS	AD18
VCC	P11	VSS	M5	VSS	AD22
VCC	P16	VSS	M11	VSS	AF1
VCC	R12	VSS	M13	VSS	AF13
VCC	R15	VSS	M14	VSS	AF26
VCC	T11	VSS	M16	VTTA	M24
VCC	T13	VSS	M22	VTTB	F17
VCC	T14	VSS	N1	WEA#	AE12
VCC	T16	VSS	N12	WEB#	AC12
VCC	V6	VSS	N13	WSC#	AE3



## 5.2 Package Dimensions

This specification outlines the mechanical dimensions for the 82443BX Host Bridge. The package is a 492 ball grid array (BGA).

**Figure 5-3. 82443BX BGA Package Dimensions—Top and Side Views**

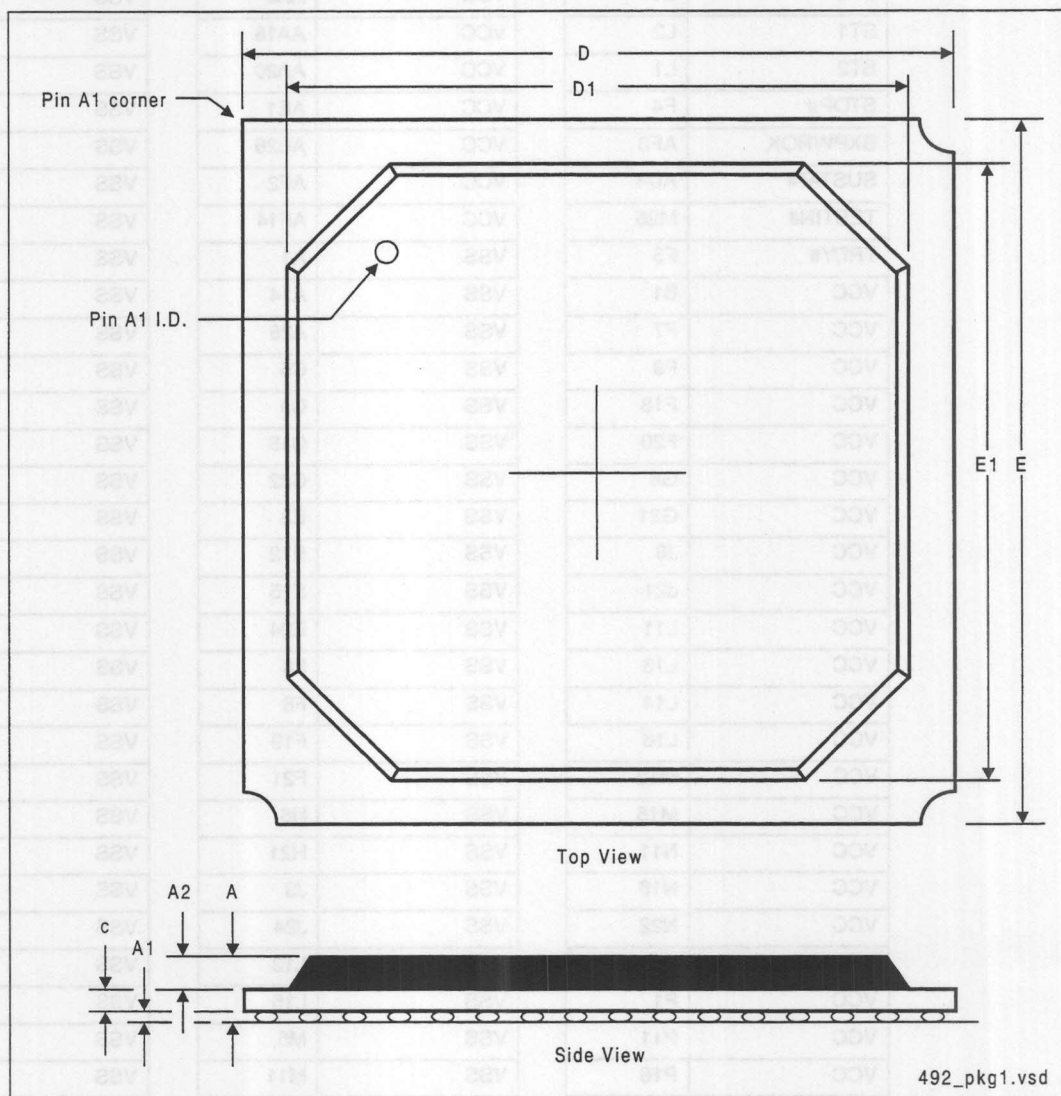


Figure 5-4. 82443BX BGA Package Dimensions—Bottom Views

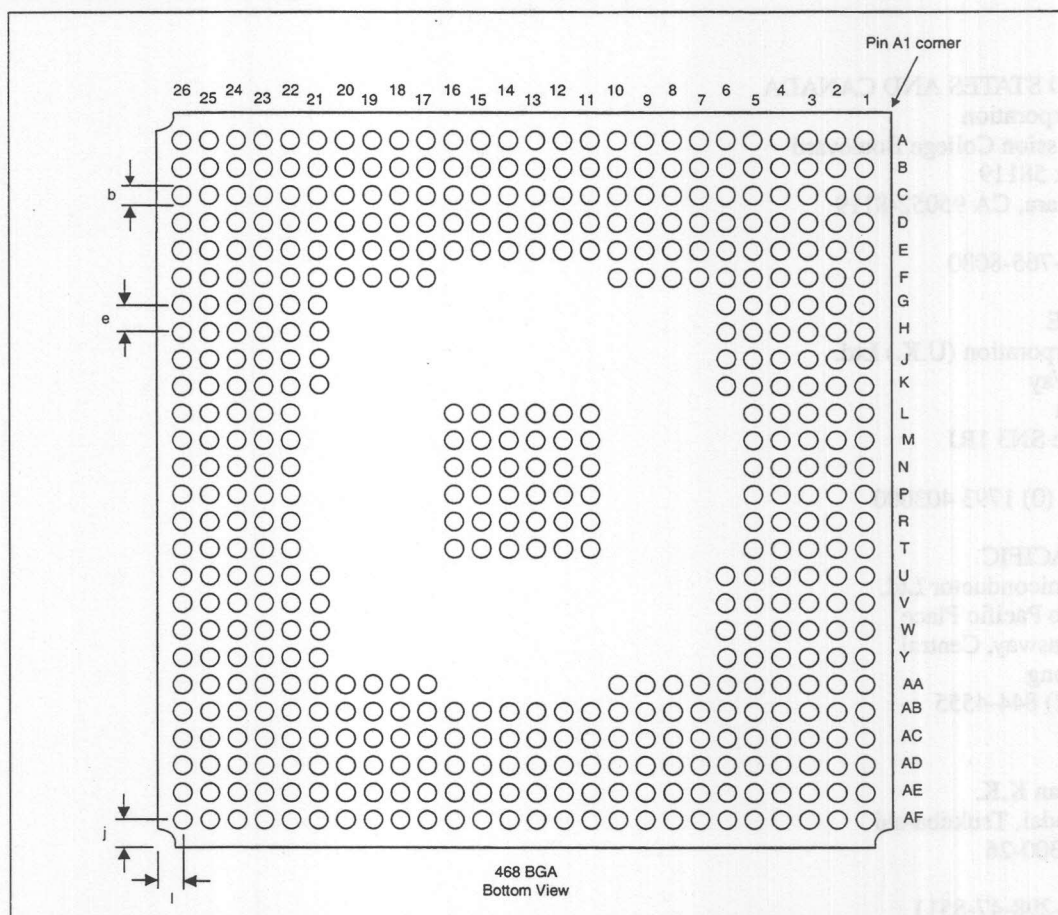


Table 5-2. 82443BX Package Dimensions (492 BGA)

Symbol	e=1.27 mm (solder ball pitch)			Note
	Min	Nominal	Max	
A	2.17	2.38	2.59	
A1	0.50	0.60	0.70	
A2	1.12	1.17	1.22	
D	34.80	35.00	35.20	
D1	29.75	30.00	30.25	
E	34.80	35.00	35.20	
E1	29.75	30.00	30.25	
I	1.63 REF.			
J	1.63 REF.			
M	26 x 26 Matrix			
N	4.92			
b	0.60	0.75	0.90	
c	0.55	0.61	0.67	

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**Flash Memory**  
**High Performance Boot Block, FlashFile™**



# Intel Flash Memory, High Performance Boot Block Family

## New Design Focus Products

Density	Product	Organization	Access	Access	Access	V <sub>pp</sub>	Package	Number
			Time (ns) 4.5 – 5.5V V <sub>cc</sub>	Time (ns) 3.0 – 3.6V V <sub>cc</sub>	Time (ns) 2.7 – 3.6V V <sub>cc</sub>			
Commercial Temperature								
8 Mb	28F800B5	1M x 8 or 512K x 16	70, 90			5V or 12V	TSOP	48
	28F800B5	1M x 8 or 512K x 16	70, 90			5V or 12V	PSOP	44
4 Mb	28F400B5	512K x 8 or 256K x 16	60, 80			5V or 12V	TSOP	48
	28F400B5	512K x 8 or 256K x 16	60, 80			5V or 12V	PSOP	44
	28F004B5	512K x 8	80			5V or 12V	TSOP	40
2 Mb	28F200B5	256K x 8 or 128K x 16	60, 80			5V or 12V	TSOP	48
	28F200B5	256K x 8 or 128K x 16	60, 80			5V or 12V	PSOP	44
	28F002BC	256K x 8	80, 120			12V	TSOP, PDIP	40
	28F002BC	256K x 8	80, 120			12V	PSOP	44
Extended Temperature								
16 Mb	28F160B3	1M x 16			120,150 1.8V I/O	2.7-3.6V or 12V	TSOP, µBGA*	48
	28F016B3	2M x 8			120,150 1.8V I/O	2.7-3.6V or 12V	TSOP, µBGA	40
8 Mb	28F800B3	512K x 16			120,150 1.8V I/O	2.7-3.6V or 12V	TSOP, µBGA	48
	28F008B3	1M x 8			120,150 1.8V I/O	2.7-3.6V or 12V	TSOP, µBGA	40
	28F800B5	1M x 8 or 512K x 16	90			5V or 12V	TSOP	48
	28F800B5	1M X 8 or 512K x 16	90			5V or 12V	PSOP	44
4 Mb	28F400B3	256K x 16			120,150 1.8V I/O	2.7-3.6V or 12V	TSOP, µBGA	48
	28F004B3	512K x 8			120,150 1.8V I/O	2.7-3.6V or 12V	TSOP, µBGA	40
	28F400B5	512K x 8 or 256K x 16	80			5V or 12V	TSOP	48
	28F400B5	512K x 8 or 256K x 16	80			5V or 12V	PSOP	44
2 Mb	28F200B5	256K x 8 or 128K x 16	80			5V or 12V	TSOP	48
	28F200B5	256K x 8 or 128K x 16	80			5V or 12V	PSOP	44

### Availability Schedule

Products not listed here are in full production.

Product	Package	Samples	Production
<b>Extended Temperatures</b>			
28F400B3/004B3	TSOP, µBGA	Q4'97	Q1'98







## SMART 5 BOOT BLOCK FLASH MEMORY FAMILY 2, 4, 8 MBIT

28F200B5, 28F400B5, 28F800B5

- **SmartVoltage Technology**
  - Smart 5 Flash: 5V Reads, 5V or 12V Writes
  - Increased Programming Throughput at 12V V<sub>pp</sub>
- **Very High-Performance Read**
  - 2-, 4-Mbit: 60 ns Access Time
  - 8-Mbit: 70 ns Access Time
- **x8/x16-Configurable Input/Output Bus**
- **Low Power Consumption**
  - Max 60 mA Read Current at 5V
  - Auto Power Savings: <1 mA Typical Standby Current
- **Optimized Array Blocking Architecture**
  - 16-KB Protected Boot Block
  - Two 8-KB Parameter Blocks
  - 96-KB and 128-KB Main Blocks
  - Top or Bottom Boot Locations
- **Extended Temperature Operation**
  - -40°C to +85°C
- **Industry-Standard Packaging**
  - 44-Lead PSOP, 48-Lead TSOP
- **Extended Block Erase Cycling**
  - 100,000 Cycles at Commercial Temp
  - 10,000 Cycles at Extended Temp
- **Hardware Data Protection Feature**
  - Absolute Hardware-Protection for Boot Block
  - Write Lockout during Power Transitions
- **Automated Word/Byte Program and Block Erase**
  - Command User Interface
  - Status Registers
  - Erase Suspend Capability
- **SRAM-Compatible Write Interface**
- **Reset/Deep Power-Down Input**
  - Provides Low-Power Mode and Reset for Boot Operations
- **Pinout Compatible 2, 4, and 8 Mbit**
- **ETOX™ Flash Technology**
  - 0.6  $\mu$  ETOX IV Initial Production
  - 0.4  $\mu$  ETOX V Later Production

Intel's word-wide Smart 5 boot block flash memory family provides 2-, 4-, and 8-Mbit memories featuring high-density, low-cost, nonvolatile, read/write storage solutions for a wide range of applications. Their asymmetrically-blocked architecture, flexible voltage, and extended cycling provide highly flexible components suitable for embedded code execution applications, such as networking infrastructure and office automation.

Based on Intel's boot block architecture, the word-wide Smart 5 boot block memory family enables quick and easy upgrades for designs that demand state-of-the-art technology. This family of products comes in industry-standard packages: the 48-lead TSOP, ideal for board-constrained applications, and the rugged, easy to handle 44-lead PSOP.

# SMART 2-BOOT BLOCK FLASH MEMORY FAMILY 2, 4, 8 MBIT

INTEGRATED CIRCUITS

<ul style="list-style-type: none"> <li>Extended Block Erase Cycling</li> <li>100,000 Cycles at Commercial Temp</li> <li>10,000 Cycles at Extended Temp</li> <li>Hardware Data Protection Feature</li> <li>Absolute Hardware Protection for Boot Block</li> <li>Write Lockout during Power Transition</li> <li>Automated Memory Program and Block Erase</li> <li>Command User Interface</li> <li>Status Register</li> <li>Erase Suspend Capability</li> <li>SMART-Compatible Write Interface</li> <li>PowerDown Power-On Reset</li> <li>Provides Low-Power Mode and Reset for Boot Operations</li> <li>Power Consumption 2, 4 and 8 Mbit</li> <li>ETOX<sup>®</sup> Flash Technology</li> <li>ETOX IV Initial Production</li> <li>ETOX V Initial Production</li> </ul>	<ul style="list-style-type: none"> <li>SmartVantage Technology</li> <li>Smart 2-Boot 2V Read/Write</li> <li>2V or 1.5V Write</li> <li>Reduced Programming Throughput at 1.5V Vpp</li> <li>Very High Performance Read</li> <li>2-4 Mbit/s at Access Time</li> <li>0.5 Mbit/s at Access Time</li> <li>Smart-Configurable Input/Output Bus</li> <li>Low Power Consumption</li> <li>Max 50 mA Read Current at 2V</li> <li>Auto Power Savings: 100 nA Typical Standby Current</li> <li>Optimized Array Blocking Architecture</li> <li>16-KB Protected Boot Block</li> <li>Two 8-KB Parameter Blocks</li> <li>24-KB and 128-KB Main Blocks</li> <li>Top or Bottom Bank Locations</li> <li>Extended Temperature Operation</li> <li>-40°C to +85°C</li> <li>Industry Standard Packaging</li> <li>55-Lead PQFP, 48-Lead TQFP</li> </ul>
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## REVISION HISTORY

Number	Description
-001	Original Version
-002	Minor changes throughout document. Section 3.1.5 and Figure 13 redone to clarify program/erase operation abort. Information added to Table 2, Figure 1, and Section 3.3 to clarify WP# on 8-Mbit, 44-PSOP. Read and Write Waveforms changed to numbered format. Typical numbers removed from DC Characteristics and Erase/Program Timings.
-003	Minor text changes throughout document. Figure 1, 44-PSOP pinout: mistake on pin 3 on 2-Mbit pinout corrected from A <sub>17</sub> to NC. Specs t <sub>EHQZ</sub> and t <sub>GHQZ</sub> improved. Explanations of program/erase abort commands reworked in Table 6, Command Codes.

## 1.0 INTRODUCTION

This datasheet contains specifications for 2-, 4-, and 8-Mbit Smart 5 boot block flash memories. Section 1 provides a feature overview. Sections 2, 3, and 4 describe the product and functionality. Section 5 details the electrical and timing specifications for both commercial and extended temperature operation.

### 1.1 New Features in the Smart 5 Memory Products

The Smart 5 boot block flash memory family offers identical features with the BV/CV/BE/CE SmartVoltage products, except the Smart 5 boot block -B5 parts only support 5V  $V_{CC}$  read voltage.

The following differences distinguish the Smart 5 boot block products from their predecessors:

- A delay is required if the part is reset during an in-progress program or erase operation.
- On the fly word-byte mode switching is no longer supported. Word-byte mode must be configured at power-up and remain stable during operation.
- Write operations are no longer specified as WE#- or CE#-controlled in favor of a simpler "unified" write method, which is compatible with either of the old methods.

### 1.2 Product Overview

The word-wide Smart 5 boot block memory family provides pinout-compatible flash memories at the 2-, 4- and 8-Mbit densities. The 28F200B5, 28F400B5, and 28F800B5 can be configured to operate either in 16-bit or 8-bit bus mode, with the data divided into individually erasable blocks.

**Table 1. Smart 5 Boot Block Family: Feature Summary**

Feature		28F200B5	28F400B5	28F800B5	Reference
$V_{CC}$ Read Voltage		5V $\pm$ 5%, 5V $\pm$ 10%			Table 10
$V_{PP}$ Prog/Erase Voltage		5V $\pm$ 10% or 12V $\pm$ 5%, auto-detected			Table 10
Bus-width		8- or 16-bit configurable			Table 2
Speed (ns)	Commercial	60, 80	60, 80	70, 90	Table 14
	Extended	80	80	90	Table 14
Memory Arrangement		x8: 256K x 8 x16: 128K x 16	x8: 512K x 8 x16: 256K x 16	x8: 1M x 8 x16: 512K x 16	
Blocking (Top or Bottom boot locations available)		1 x 16k Boot Block 2 x 8k Parameter 1 x 96k Main Block 1 x 128k Main Block	1 x 16k Boot Block 2 x 8k Parameter 1 x 96k Main Block 3 x 128k Main Block	1 x 16k Boot Block 2 x 8k Parameter 1 x 96k Main Block 7 x 128k Main Block	Sect. 2.3, Fig. 3-6
Locking		Boot Block lockable using WP# and/or RP# All others protectable using $V_{PP}$ switch			Sect. 3.3
Operating Temperature		Commercial: 0°C – +70 °C Extended: -40°C – +85 °C			Table 10
Erase Cycling		100,000 cycles at Commercial Temperature 10,000 cycles at Extended Temperature			
Packages		44-PSOP, 48-TSOP			Figs. 1-2

## PRODUCT PREVIEW



SmartVoltage technology enables fast factory programming and low-power designs. Specifically designed for 5V systems, Smart 5 components support read operations at 5V  $V_{CC}$  and internally configure to program/erase at 5V or 12V. The 12V  $V_{PP}$  option renders the fastest program and erase performance which will increase your factory throughput. With the 5V  $V_{PP}$  option,  $V_{CC}$  and  $V_{PP}$  can be tied together for a simple 5V design. In addition, the dedicated  $V_{PP}$  pin gives complete data protection when  $V_{PP} \leq V_{PPLK}$ .

The memory array is asymmetrically divided into blocks in an asymmetrical architecture to accommodate microprocessors that boot from the top (denoted by -T suffix) or the bottom (-B suffix) of the memory map. The blocks include a hardware-lockable boot block (16,384 bytes), two parameter blocks (8,192 bytes each) and main blocks (one block of 98,304 bytes and additional block(s) of 131,072 bytes). See Figures 3–6 for memory maps. Each block can be independently erased and programmed 100,000 times at commercial temperature or 10,000 times at extended temperature. Unlike erase operations, which erase all locations within a block simultaneously, each byte or word in the flash memory can be programmed independently of other memory locations.

The hardware-lockable boot block provides complete code security for the kernel code required for system initialization. Locking and unlocking of the boot block is controlled by  $WP\#$  and/or  $RP\#$  (see Section 3.3 for details).

The system processor interfaces to the flash device through a Command User Interface (CUI), using valid command sequences to initiate device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for program and erase operations. The Status Register (SR) indicates the status of the WSM and whether it successfully completed the desired program or erase operation.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical  $I_{CCR}$  current is 1 mA.

When  $CE\#$  and  $RP\#$  pins are at  $V_{CC}$ , the component enters a CMOS standby mode. Driving  $RP\#$  to GND enables a deep power-down mode which significantly reduces power consumption, provides write protection, resets the device, and clears the status register. A reset time ( $t_{PHQV}$ ) is required from  $RP\#$  switching high until outputs are valid. Likewise, the device has a wake time ( $t_{PHEL}$ ) from  $RP\#$ -high until writes to the CUI are recognized. See Section 4.2.

The deep power-down mode can also be used as a device reset, allowing the flash to be reset along with the rest of the system. For example, when the flash memory powers-up, it automatically defaults to the read array mode, but during a warm system reset, where power continues uninterrupted to the system components, the flash memory could remain in a non-read mode, such as erase. Consequently, the system Reset signal should be tied to  $RP\#$  to reset the memory to normal read mode upon activation of the Reset signal. This also provides protection against unwanted command writes due to invalid system bus conditions during system reset or power-up/down sequences.

These devices are configurable at power-up for either byte-wide or word-wide input/output using the  $BYTE\#$  pin. Please see Table 2 for a detailed description of  $BYTE\#$  operations, especially the usage of the  $DQ_{15}/A_{-1}$  pin.

These Smart 5 memory products are available in the 44-lead PSOP (Plastic Small Outline Package), which is ROM/EPROM-compatible, and the 48-lead TSOP (Thin Small Outline Package, 1.2 mm thick) as shown in Figure 1, and 2, respectively.

## 2.0 PRODUCT DESCRIPTION

This section describes the pinout and block architecture of the device family.

### 2.1 Pin Descriptions

The pin descriptions table details the usage of each of the device pins.

Table 2. Pin Descriptions

Symbol	Type	Name and Function
A <sub>0</sub> –A <sub>18</sub>	INPUT	<b>ADDRESS INPUTS</b> for memory addresses. Addresses are internally latched during a write cycle. <b>28F200: A[0-16], 28F400: A[0-17], 28F800: A[0-18]</b>
A <sub>9</sub>	INPUT	<b>ADDRESS INPUT:</b> When A <sub>9</sub> is at V <sub>HH</sub> the signature mode is accessed. During this mode, A <sub>0</sub> decodes between the manufacturer and device IDs. When BYTE# is at a logic low, only the lower byte of the signatures are read. DQ <sub>15</sub> /A <sub>–1</sub> is a don't care in the signature mode when BYTE# is low.
DQ <sub>0</sub> –DQ <sub>7</sub>	INPUT/ OUTPUT	<b>DATA INPUTS/OUTPUTS:</b> Inputs array data on the second CE# and WE# cycle during a Program command. Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched during the write cycle. Outputs array, Intelligent Identifier and Status Register data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled.
DQ <sub>8</sub> –DQ <sub>15</sub>	INPUT/ OUTPUT	<b>DATA INPUTS/OUTPUTS:</b> Inputs array data on the second CE# and WE# cycle during a Program command. Data is internally latched during the write cycle. Outputs array data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled as in the byte-wide mode (BYTE# = "0"). In the byte-wide mode DQ <sub>15</sub> /A <sub>–1</sub> becomes the lowest order address for data output on DQ <sub>0</sub> –DQ <sub>7</sub> .
CE#	INPUT	<b>CHIP ENABLE:</b> Activates the device's control logic, input buffers, decoders and sense amplifiers. CE# is active low. CE# high de-selects the memory device and reduces power consumption to standby levels. If CE# and RP# are high, but not at a CMOS high level, the standby current will increase due to current flow through the CE# and RP# input stages.
OE#	INPUT	<b>OUTPUT ENABLE:</b> Enables the device's outputs through the data buffers during a read cycle. OE# is active low.
WE#	INPUT	<b>WRITE ENABLE:</b> Controls writes to the Command Register and array blocks. WE# is active low. Addresses and data are latched on the rising edge of the WE# pulse.
RP#	INPUT	<b>RESET/DEEP POWER-DOWN:</b> Uses three voltage levels (V <sub>IL</sub> , V <sub>IH</sub> , and V <sub>HH</sub> ) to control two different functions: reset/deep power-down mode and boot block unlocking. It is backwards-compatible with the BX/BL/BV products.  <b>When RP# is at logic low, the device is in reset/deep power-down mode,</b> which puts the outputs at High-Z, resets the Write State Machine, and draws minimum current.  <b>When RP# is at logic high, the device is in standard operation.</b> When RP# transitions from logic-low to logic-high, the device defaults to the read array mode.  <b>When RP# is at V<sub>HH</sub>, the boot block is unlocked</b> and can be programmed or erased. This overrides any control from the WP# input.

Table 2. Pin Descriptions (Continued)

Symbol	Type	Name and Function
WP#	INPUT	<p><b>WRITE PROTECT:</b> Provides a method for unlocking the boot block with a logic level signal in a system without a 12V supply.</p> <p><b>When WP# is at logic low, the boot block is locked</b>, preventing program and erase operations to the boot block. If a program or erase operation is attempted on the boot block when WP# is low, the corresponding status bit (bit 4 for program, bit 5 for erase) will be set in the Status Register to indicate the operation failed.</p> <p><b>When WP# is at logic high, the boot block is unlocked</b> and can be programmed or erased.</p> <p><b>NOTE:</b> This feature is overridden and the boot block unlocked when RP# is at <math>V_{HH}</math>. This pin can not be left floating. Because the 8-Mbit 44-PSOP package does not have enough pins, it does not include this pin and thus 12V on RP# is required to unlock the boot block. See Section 3.3 for details on write protection.</p>
BYTE#	INPUT	<p><b>BYTE# ENABLE:</b> Configures whether the device operates in byte-wide mode (x8) or word-wide mode (x16). This pin must be set at power-up or return from deep power-down and not changed during device operation. BYTE# pin must be controlled at CMOS levels to meet the CMOS current specification in standby mode.</p> <p><b>When BYTE# is at logic low, the byte-wide mode is enabled</b>, where data is read and programmed on DQ<sub>0</sub>–DQ<sub>7</sub> and DQ<sub>15</sub>/A<sub>–1</sub> becomes the lowest order address that decodes between the upper and lower byte. DQ<sub>8</sub>–DQ<sub>14</sub> are tri-stated during the byte-wide mode.</p> <p><b>When BYTE# is at logic high, the word-wide mode is enabled</b>, where data is read and programmed on DQ<sub>0</sub>–DQ<sub>15</sub>.</p>
V <sub>CC</sub>		<b>DEVICE POWER SUPPLY:</b> 5.0V ± 10%
V <sub>PP</sub>		<b>PROGRAM/ERASE POWER SUPPLY:</b> For erasing memory array blocks or programming data in each block, a voltage either of 5V ± 10% or 12V ± 5% must be applied to this pin. When $V_{PP} < V_{PPLK}$ all blocks are locked and protected against Program and Erase commands.
GND		<b>GROUND:</b> For all internal circuitry.
NC		<b>NO CONNECT:</b> Pin may be driven or left floating.

## 2.2 Pinouts

Intel's Smart 5 boot block architecture provides upgrade paths in each package pinout up to the 8-Mbit density. The 44-lead PSOP pinout follows the industry-standard ROM/EPROM pinout, as shown in Figure 1. Designs with space concerns should consider the 48-lead pinout shown in Figure 2.

Pinouts for the corresponding 2-, 4- and 8-Mbit components are provided on the same diagram for convenient reference. 2-Mbit pinouts are given on the chip illustration in the center, with 4-Mbit and 8-Mbit pinouts going outward from the center.



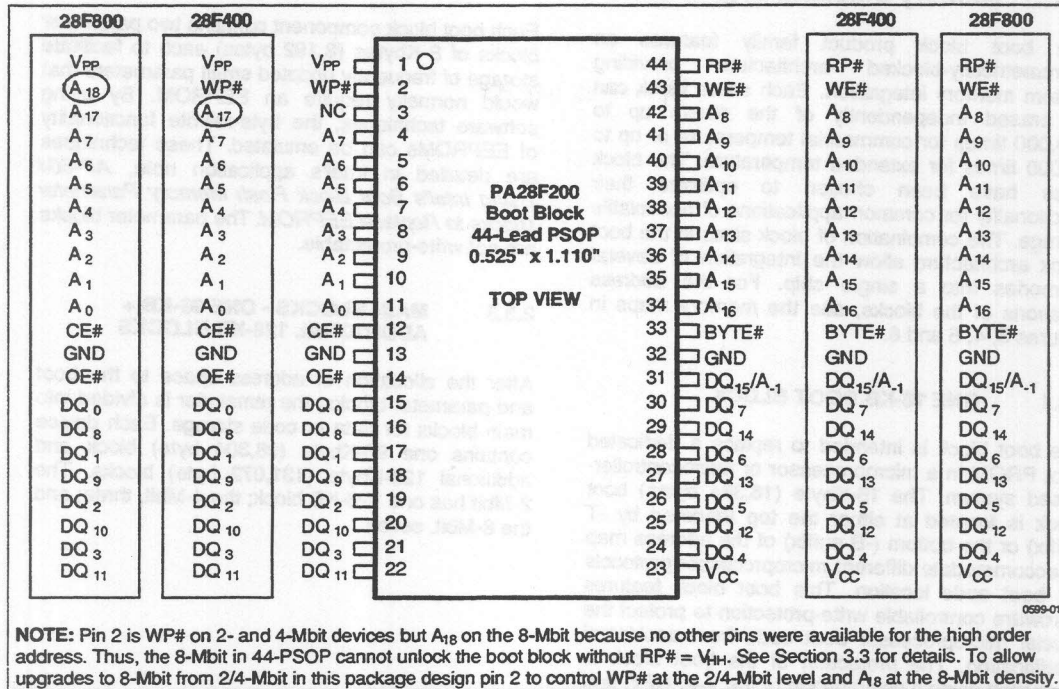


Figure 1. 44-Lead PSOP Pinout Diagram

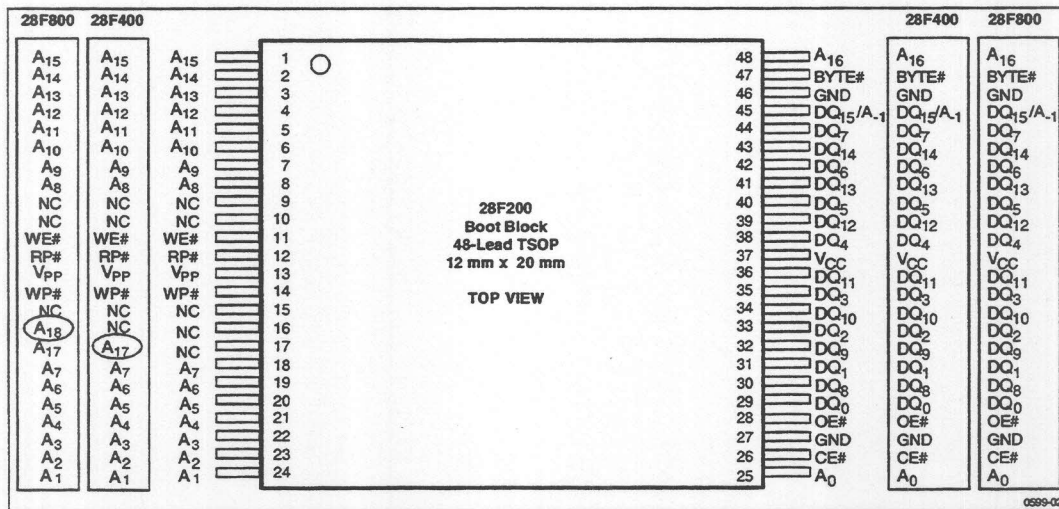


Figure 2. 48-Lead TSOP Pinout Diagram

### 2.3 Memory Blocking Organization

The boot block product family features an asymmetrically-blocked architecture providing system memory integration. Each erase block can be erased independently of the others up to 100,000 times for commercial temperature or up to 10,000 times for extended temperature. The block sizes have been chosen to optimize their functionality for common applications of nonvolatile storage. The combination of block sizes in the boot block architecture allow the integration of several memories into a single chip. For the address locations of the blocks, see the memory maps in Figures 3, 4, 5 and 6.

#### 2.3.1 ONE 16-KB BOOT BLOCK

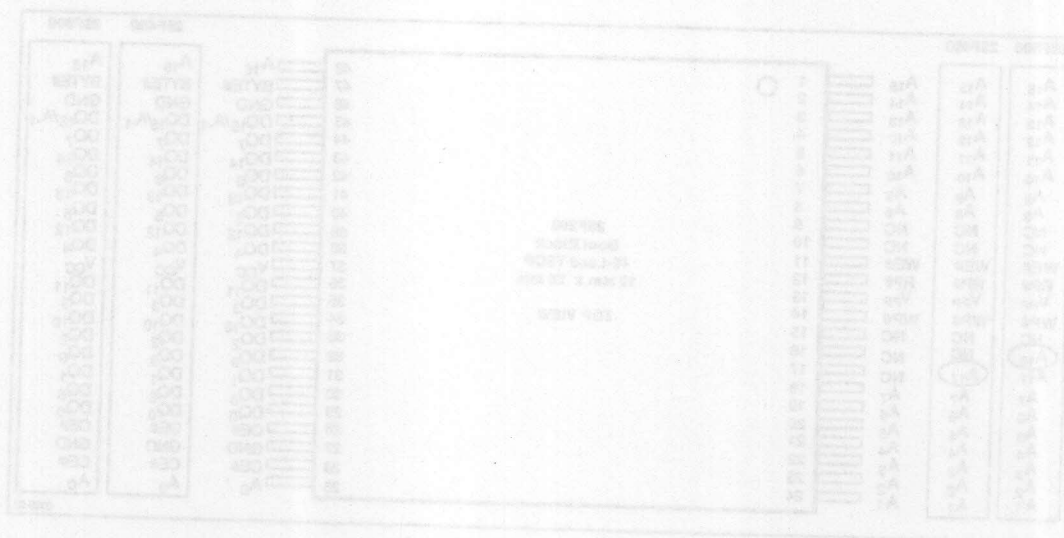
The boot block is intended to replace a dedicated boot PROM in a microprocessor or microcontroller-based system. The 16-Kbyte (16,384 bytes) boot block is located at either the top (denoted by -T suffix) or the bottom (-B suffix) of the address map to accommodate different microprocessor protocols for boot code location. This boot block features hardware controllable write-protection to protect the crucial microprocessor boot code from accidental modification. The protection of the boot block is controlled using a combination of the  $V_{pp}$ , RP#, and WP# pins, as is detailed in Section 3.3.

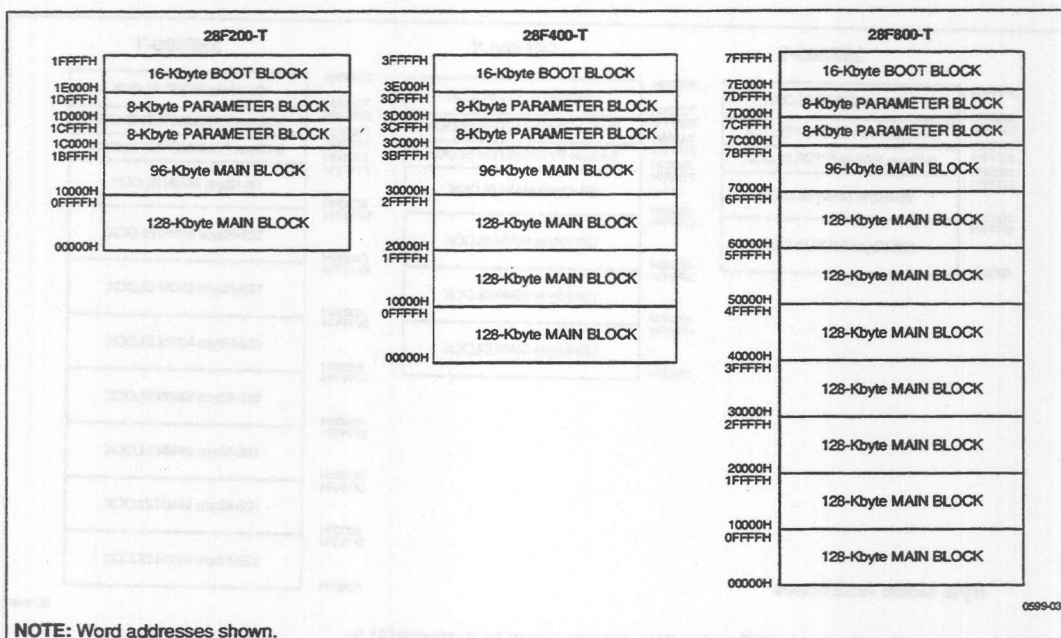
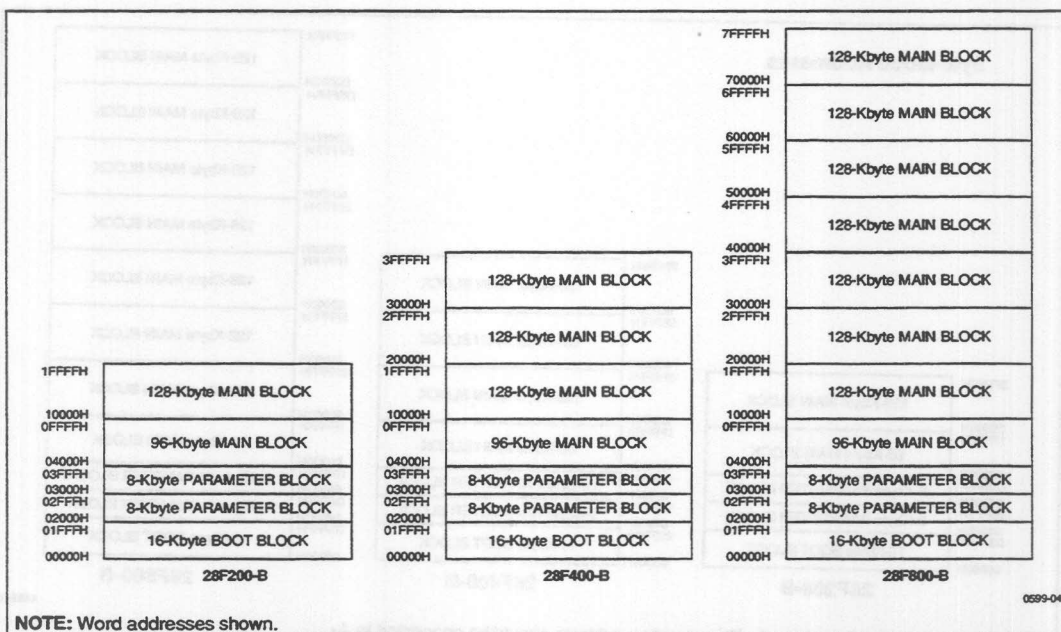
#### 2.3.2 TWO 8-KB PARAMETER BLOCKS

Each boot block component contains two parameter blocks of 8 Kbytes (8,192 bytes) each to facilitate storage of frequently updated small parameters that would normally require an EEPROM. By using software techniques, the byte-rewrite functionality of EEPROMs can be emulated. These techniques are detailed in Intel's application note, *AP-604 Using Intel's Boot Block Flash Memory Parameter Blocks to Replace EEPROM*. The parameter blocks are not write-protectable.

#### 2.3.3 MAIN BLOCKS - ONE 96-KB + ADDITIONAL 128-KB BLOCKS

After the allocation of address space to the boot and parameter blocks, the remainder is divided into main blocks for data or code storage. Each device contains one 96-Kbyte (98,304 byte) block and additional 128-Kbyte (131,072 byte) blocks. The 2-Mbit has one 128-KB block; the 4-Mbit, three; and the 8-Mbit, seven.




**Figure 3. Word-Wide x16-Mode Memory Maps (Top Boot)**

**Figure 4. Word-Wide x16-Mode Memory Maps (Bottom Boot)**



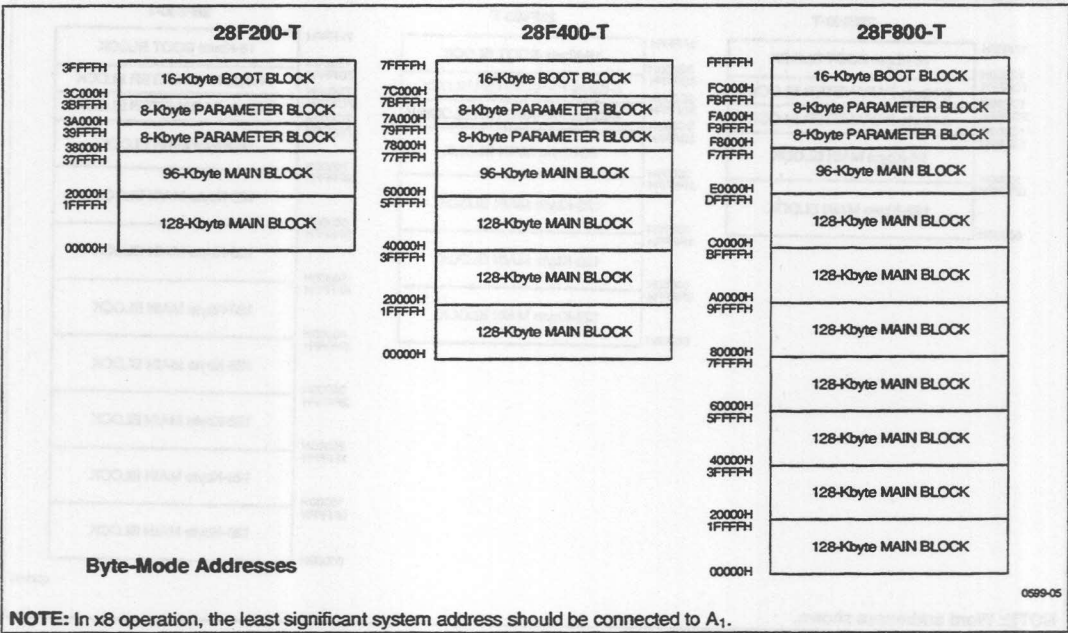


Figure 5. Byte-Wide x8-Mode Memory Maps (Top Boot)

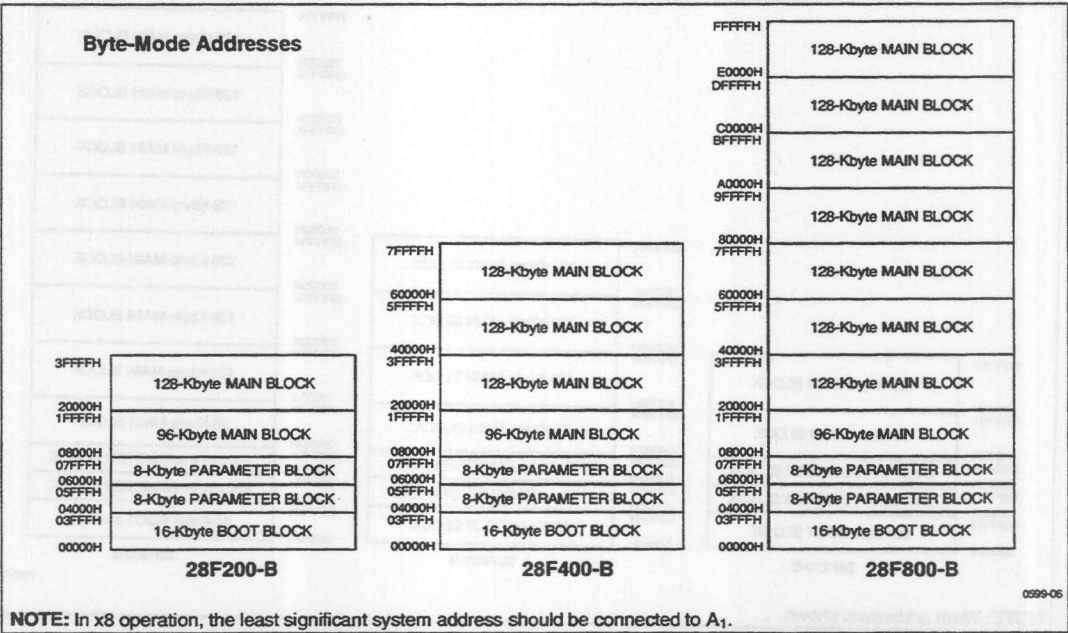


Figure 6. Byte-Wide x8-Mode Memory Maps (Bottom Boot)

### 3.0 PRINCIPLES OF OPERATION

The system processor accesses the Smart 5 boot block memories through the Command User Interface (CUI), which accepts commands written with standard microprocessor write timings and TTL-level control inputs. The flash can be switched into each of its read and write modes through commands issued to the CUI.

The flash memory has three read modes and two write modes. The read modes are read array, read identifier, and read status. The write modes are program and block erase. An additional mode, erase suspend to read, is available only during suspended block erasures. A comprehensive chart showing the state transitions is in Appendix B.

After initial device power-up or return from deep power-down mode, the device defaults to read array mode. In this mode, manipulation of the memory control pins allows array read, standby, and output disable operations. The other read modes, read identifier and read status register, can be reached by issuing the appropriate command to the CUI. Array data, Identifier codes and status register results can be accessed using these commands independently from the  $V_{PP}$  voltage. Read identifier mode can also be accessed by PROM programming equipment by raising  $A_9$  to high voltage ( $V_{ID}$ ).

CUI commands sequences also control the write functions of the flash memory, Program and Erase. Issuing program or erase command sequences internally latches addresses and data and initiates Write State Machine (WSM) operations to execute the requested write function. The WSM internally regulates the program and erase algorithms, including pulse repetition, internal verification, and margining of data, freeing the host processor from these tasks and allowing precise control for high reliability. To execute Program or Erase commands,  $V_{PP}$  must be at valid write voltage (5V or 12V).

While the WSM is executing a program operation, the device defaults to the read status register mode and all commands are ignored. Thus during the programming process, only status register data can be accessed from the device. While the WSM is executing a erase operation, the device also defaults to the read status register mode but one additional command is available, erase suspend to read, which will suspend the erase operation and allow reading of array data. The suspended erase

operation can be completed by issuing the Erase Resume command. After the program or erase operation has completed, the device remains in read status register mode. From this mode any of the other read or write modes can be reached with the appropriate command. For example, to read data, issue the Read Array command. Additional Program or Erase commands can also be issued from this state.

During program or erase operations, the array data is not available for reading or code execution, except during an erase suspend. Consequently, the software that initiates and polls progress of program and erase operations must be copied to and executed from system RAM during flash memory update. After successful completion, reads are again possible via the Read Array command.

Each of the device modes will be discussed in detail in the following sections.

### 3.1 Bus Operations

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles. Four control pins dictate the data flow in and out of the component:  $CE\#$ ,  $OE\#$ ,  $WE\#$ , and  $RP\#$ . These bus operations are summarized in Table 3 and 4.

#### 3.1.1 READ

The flash memory has three read modes available, read array, read identifier, and read status. These read modes are accessible independent of the  $V_{PP}$  voltage.  $RP\#$  can be at either  $V_{IH}$  or  $V_{HH}$ . The appropriate read-mode command must be issued to the CUI to enter the corresponding mode. Upon initial device power-up or after exit from deep power-down mode, the device automatically defaults to read array mode.

$CE\#$  and  $OE\#$  must be driven active to obtain data at the outputs.  $CE\#$  is the device selection control, and, when active, enables the selected memory device.  $OE\#$  is the data output ( $DQ_0$ – $DQ_{15}$ ) control and when active drives the selected memory data onto the I/O bus. In read modes,  $WE\#$  must be at  $V_{IH}$  and  $RP\#$  must be at  $V_{IH}$  or  $V_{HH}$ . Figure 14 illustrates a read cycle.

## PRODUCT PREVIEW

**3.1.2 OUTPUT DISABLE**

With OE# at a logic-high level ( $V_{IH}$ ), the device outputs are disabled. Output pins DQ<sub>0</sub>–DQ<sub>15</sub> are placed in a high-impedance state.

**3.1.3 STANDBY**

Deselecting the device by bringing CE# to a logic-high level ( $V_{IH}$ ) places the device in standby mode which substantially reduces device power consumption. In standby, outputs DQ<sub>0</sub>–DQ<sub>15</sub> are placed in a high-impedance state independent of OE#. If deselected during program or erase operation, the device continues functioning and consuming active power until the operation completes.

**3.1.4 WORD/BYTE CONFIGURATION**

The device can be configured for either an 8-bit or 16-bit bus width by setting the BYTE# pin before power-up.

When BYTE# is set to logic low, the byte-wide mode is enabled, where data is read and programmed on DQ<sub>0</sub>–DQ<sub>7</sub> and DQ<sub>15</sub>/A<sub>–1</sub> becomes the lowest order address that decodes between the upper and lower byte. DQ<sub>8</sub>–DQ<sub>14</sub> are tri-stated during the byte-wide mode.

When BYTE# is at logic high, the word-wide mode is enabled, and data is read and programmed on DQ<sub>0</sub>–DQ<sub>15</sub>.

**3.1.5 DEEP POWER-DOWN/RESET**

RP# at  $V_{IL}$  initiates the deep power-down mode, also referred to as Reset mode.

From read mode, RP# going low for time  $t_{PLPH}$  deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. After return from power-down, a time  $t_{PHQV}$  is required until the initial memory access outputs are valid. A delay ( $t_{PHWL}$  or  $t_{PHEL}$ ) is required after return from power-down before a write can be initiated. After this wake-up interval, normal operation is restored. The CUI resets to read array

mode, and the status register is set to 80H. This case is shown in Figure 13A.

If RP# is taken low for time  $t_{PLPH}$  during a program or erase operation, the operation will be aborted and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid, since the data may be partially erased or written. The abort process goes through the following sequence: When RP# goes low, the device shuts down the operation in progress, a process which takes time  $t_{PLRH}$  to complete. After this time  $t_{PLRH}$ , the part will either reset to read array mode (if RP# has gone high during  $t_{PLRH}$ , Figure 13B) or enter deep power-down mode (if RP# is still logic low after  $t_{PLRH}$ , Figure 13C). In both cases, after returning from an aborted operation, the relevant time  $t_{PHQV}$  or  $t_{PHWL}/t_{PHEL}$  must be waited before a read or write operation is initiated, as discussed in the previous paragraph. However, in this case, these delays are referenced to the end of  $t_{PLRH}$  rather than when RP# goes high.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, processor expects to read from the flash memory. Automated flash memories provide status information when read during program or block erase operations. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. Intel's Flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

**3.1.6 WRITE**

The CUI does not occupy an addressable memory location. Instead, commands are written into the CUI using standard microprocessor write timings when WE# and CE# are low, OE# =  $V_{IH}$ , and the proper address and data (command) are presented. The address and data for a command are latched on the rising edge of WE# or CE#, whichever goes high first. Figure 15 illustrates a write operation.



**Table 3. Bus Operations for Word-Wide Mode (BYTE# = V<sub>IH</sub>)**

Mode	Notes	RP#	CE#	OE#	WE#	A <sub>9</sub>	A <sub>0</sub>	V <sub>PP</sub>	DQ <sub>0-15</sub>
Read	1,2,3	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	X	X	D <sub>OUT</sub>
Output Disable		V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X	X	X	High Z
Standby		V <sub>IH</sub>	V <sub>IH</sub>	X	X	X	X	X	High Z
Deep Power-Down	9	V <sub>IL</sub>	X	X	X	X	X	X	High Z
Intelligent Identifier (Mfr.)	4	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>ID</sub>	V <sub>IL</sub>	X	0089 H
Intelligent Identifier (Device)	4,5	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>ID</sub>	V <sub>IH</sub>	X	See Table 5
Write	6,7,8	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	X	X	X	D <sub>IN</sub>

**Table 4. Bus Operations for Byte-Wide Mode (BYTE# = V<sub>IL</sub>)**

Mode	Notes	RP#	CE#	OE#	WE#	A <sub>9</sub>	A <sub>0</sub>	A <sub>-1</sub>	V <sub>PP</sub>	DQ <sub>0-7</sub>	DQ <sub>8-14</sub>
Read	1,2,3	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	X	X	X	D <sub>OUT</sub>	High Z
Output Disable		V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X	X	X	X	High Z	High Z
Standby		V <sub>IH</sub>	V <sub>IH</sub>	X	X	X	X	X	X	High Z	High Z
Deep Power-Down	9	V <sub>IL</sub>	X	X	X	X	X	X	X	High Z	High Z
Intelligent Identifier (Mfr.)	4	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>ID</sub>	V <sub>IL</sub>	X	X	89H	High Z
Intelligent Identifier (Device)	4,5	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>ID</sub>	V <sub>IH</sub>	X	X	See Table 5	High Z
Write	6,7,8	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	X	X	X	X	D <sub>IN</sub>	High Z

**NOTES:**

1. Refer to DC Characteristics.
2. X can be V<sub>IL</sub>, V<sub>IH</sub> for control pins and addresses, V<sub>PPLK</sub> or V<sub>PPH</sub> for V<sub>PP</sub>.
3. See DC Characteristics for V<sub>PPLK</sub>, V<sub>PPH1</sub>, V<sub>PPH2</sub>, V<sub>IH</sub>, V<sub>ID</sub> voltages.
4. Manufacturer and device codes may also be accessed via a CUI write sequence, A<sub>0</sub> selects, all other addresses = X.
5. See Table 5 for device IDs.
6. Refer to Table 7 for valid D<sub>IN</sub> during a write operation.
7. Command writes for block erase or program are only executed when V<sub>PP</sub> = V<sub>PPH1</sub> or V<sub>PPH2</sub>.
8. To program or erase the boot block, hold RP# at V<sub>IH</sub> or WP# at V<sub>IH</sub>. See Section 3.3.
9. RP# must be at GND ± 0.2V to meet the maximum deep power-down current specified.

### 3.2 Modes of Operation

The flash memory has three read modes and two write modes. The read modes are read array, read identifier, and read status. The write modes are program and block erase. An additional mode, erase suspend to read, is available only during suspended block erasures. These modes are reached using the commands summarized in Table 6. A comprehensive chart showing the state transitions is in Appendix B.

#### 3.2.1 READ ARRAY

After initial device power-up or return from deep power-down mode, the device defaults to read array mode. This mode can also be entered by writing the Read Array command (FFH). The device remains in this mode until another command is written.

Data is read by presenting the address of the read location in conjunction with a read bus operation.

Once the WSM has started a program or block erase operation, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend command. The Read Array command functions independently of the  $V_{PP}$  voltage and  $RP\#$  can be  $V_{IH}$  or  $V_{HH}$ .

During system design, consideration should be taken to ensure address and control inputs meet required input slew rates of <10 ns as defined in Figures 10 and 11.

#### 3.2.2 READ IDENTIFIER

To read the manufacturer and device codes, the device must be in intelligent identifier read mode, which can be reached using two methods: by writing the intelligent identifier command (90H) or by taking the  $A_9$  pin to  $V_{ID}$ . Once in intelligent identifier read mode,  $A_0 = 0$  outputs the manufacturer's identification code and  $A_0 = 1$  outputs the device code. In byte-wide mode, only the lower byte of the above signatures is read ( $DQ_{15}/A_{-1}$  is a "don't care" in this mode). See Table 5 for product signatures. To return to read array mode, write a Read Array command (FFH).

Table 5. Word-Mode Intelligent Identifier Codes

Product	Mfr. ID	Device ID	
		-T Top Boot	-B Bottom Boot
28F200	0089 H	2274 H	2275 H
28F400	0089 H	4470 H	4471 H
28F800	0089 H	889C H	889D H

NOTE: In byte-mode, the upper byte will be tri-stated.

#### 3.2.3 READ STATUS REGISTER

The device Status Register indicates when a program or erase operation is complete, and the success or failure of that operation. The status register is output when the device is read in read status register mode, which can be entered by issuing the Read Status (70H) command to the CUI. This mode is automatically entered when a program or erase operation is initiated, and the device remains in this mode after the operation has completed. The status register bit codes are defined in Table 8

The Status Register bits are output on  $DQ_0$ – $DQ_7$ , in both byte-wide (x8) or word-wide (x16) mode. In the word-wide mode, the upper byte,  $DQ_8$ – $DQ_{15}$ , outputs 00H during a Read Status command. In the byte-wide mode,  $DQ_8$ – $DQ_{14}$  are tri-stated and  $DQ_{15}/A_{-1}$  retains the low order address function.

Note that the contents of the Status Register are latched on the falling edge of  $OE\#$  or  $CE\#$ , whichever occurs last in the read cycle. This prevents possible bus errors which might occur if Status Register contents change while being read.  $CE\#$  or  $OE\#$  must be toggled with each subsequent status read, or the Status Register will not indicate completion of a program or erase operation.

To return to reading from the array, issue a Read Array (FFH) command.

##### 3.2.3.1 Clearing the Status Register

Status register bits SR.5, SR.4, and SR.3 are set to "1"s when appropriate by the WSM but can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 8). By requiring system software to reset these bits, several operations (such as cumulatively

erasing multiple blocks or programming several bytes in sequence) may be performed before polling the Status Register to determine if an error occurred during the series.

Issue the Clear Status Register command (50H) to clear the status register. It functions independently of the applied  $V_{PP}$  voltage and RP# can be  $V_{IH}$  or  $V_{HH}$ . This command is not functional during block erase suspend modes. Resetting the part with RP# also clears the Status Register.

### 3.2.4 WORD/BYTE PROGRAM

Word or byte program operations are executed by a two-cycle command sequence. Program Setup (40H) is issued, followed by a second write that specifies the address and data (latched on the rising edge of WE# or CE#, whichever comes first). The WSM then takes over, controlling the program and program verify algorithms internally. While the WSM is working, the device automatically enters read status register mode and remains there after the word/byte program is complete. (see Figure 7). The completion of the program event is indicated on status register bit SR.7.

When a word/byte program is complete, check status register bit SR.4 for an error flag ("1"). The cause of a failure may be found on SR.3, which indicates "1" if  $V_{PP}$  was out of program/erase voltage range ( $V_{PPH1}$  or  $V_{PPH2}$ ). The Status Register should be cleared before the next operation. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s.

Since the device remains in Status Register Read mode after programming is completed, a command must be issued to switch to another mode before beginning a different operation.

### 3.2.5 BLOCK ERASE

A block erase changes all block data to 1's (FFFFH) and is initiated by a two-cycle command. An Erase Setup command (20H) is issued first, followed by an Erase Confirm command (D0H) along with an address within the target block. The address will be latched at the rising edge of WE# or CE#, whichever comes first.

Internally, the WSM will program all bits in the block to "0," verify all bits are adequately programmed to "0," erase all bits to "1," and verify that all bits in the

block are sufficiently erased. After block erase command sequence is issued, the device automatically enters read status register mode and outputs status register data when read (see Figure 8). The completion of the erase event is indicated on status register bit SR.7.

When an erase is complete, check status register bit SR.5 for an error flag ("1"). The cause of a failure may be found on SR.3, which indicates "1" if  $V_{PP}$  was out of program/erase voltage range ( $V_{PPH1}$  or  $V_{PPH2}$ ). If an Erase Setup (20H) command is issued but not followed by an Erase Confirm (D0H) command, then both the Program Status (SR.4) and the Erase Status (SR.5) will be set to "1."

The Status Register should be cleared before the next operation. Since the device remains in Status Register Read mode after erasing is completed, a command must be issued to switch to another mode before beginning a different operation.

#### 3.2.5.1 Erase Suspend/Resume

The Erase Suspend command (B0H) interrupts an erase operation in order to read data in another block of memory. While the erase is in progress, issuing the Erase Suspend command requests that the WSM suspend the erase algorithm after a certain latency period. The device outputs Status Register data when read after the Erase Suspend command is issued. Status Register bits SR.7 and SR.6 indicate when the block erase operation has been suspended (both will be set to "1").

At this point, a Read Array command (FFH) can be written to read from blocks other than that which is suspended. The only other valid commands at this time are Erase Resume (D0H) or Read Status Register.

During erase suspend mode, the chip can go into a pseudo-standby mode by taking CE# to  $V_{IH}$ , which reduces active current draw.  $V_{PP}$  must remain at  $V_{PPH1}$  or  $V_{PPH2}$  (the same  $V_{PP}$  level used for block erase) while erase is suspended. RP# must also remain at  $V_{IH}$  or  $V_{HH}$  (the same RP# level used for block erase).

To resume the erase operation, enable the chip by taking CE# to  $V_{IL}$ , then issue the Erase Resume command, which continues the erase sequence to completion. As with the end of a standard erase operation, the status register must be read, cleared, and the next instruction issued in order to continue.



Table 6. Command Codes and Descriptions

Code	Device Mode	Description
00	Invalid/ Reserved	Unassigned commands that should not be used. Intel reserves the right to redefine these codes for future functions.
FF	Read Array	Places the device in read array mode, so that array data will be output on the data pins.
40	Program Set-Up	<p>Sets the CUI into a state such that the next write will load the Address and Data registers. The next write after the Program Set-Up command will latch addresses and data on the rising edge and begin the program algorithm. The device then defaults to the read status mode, where the device outputs Status Register data when OE# is enabled. To read the array, issue a Read Array command.</p> <p>To cancel a program operation after issuing a Program Set-Up command, write all 1's (FFH for x8, FFFFH for x16) to the CUI. This will return to read status register mode after a standard program time without modifying array contents. If a program operation has already been initiated to the WSM this command can not cancel that operation in progress.</p>
10	Alternate Prog Set-Up	(See 40H/Program Set-Up)
20	Erase Set-Up	Prepares the CUI for the Erase Confirm command. If the next command is not an Erase Confirm command, then the CUI will set both the Program Status (SR.4) and Erase Status (SR.5) bits of the Status Register to a "1," place the device into the read Status Register state, and wait for another command without modifying array contents. This can be used to cancel an erase operation after the Erase Setup command has been issued. If an operation has already been initiated to the WSM this can not cancel that operation in progress.
D0	Erase Resume/ Erase Confirm	If the previous command was an Erase Set-Up command, then the CUI will latch address and data, and begin erasing the block indicated on the address pins. During erase, the device will respond only to the Read Status Register and Erase Suspend commands and will output Status Register data when OE# is toggled low. Status Register data is updated by toggling either OE# or CE# low.
B0	Erase Suspend	Valid only while an erase operation is in progress and will be ignored in any other circumstance. Issuing this command will begin to suspend erase operation. The Status Register will indicate when the device reaches erase suspend mode. In this mode, the CUI will respond only to the Read Array, Read Status Register, and Erase Resume commands and the WSM will also set the WSM Status bit to a "1" (ready). The WSM will continue to idle in the SUSPEND state, regardless of the state of all input control pins except RP#, which will immediately shut down the WSM and the remainder of the chip, if it is made active. During a suspend operation, the data and address latches will remain closed, but the address pads are able to drive the address into the read path. See Section 3.2.5.1.
70	Read Status Register	Puts the device into the read status register mode, so that reading the device outputs status register data, regardless of the address presented to the device. The device automatically enters this mode after program or erase has completed. This is one of the two commands that is executable while the WSM is operating. See Section 3.2.3.

**Table 6. Command Codes and Descriptions (Continued)**

Code	Device Mode	Description
50	Clear Status Register	<p>The WSM can only set the Program Status and Erase Status bits in the status register to "1"; it cannot clear them to "0."</p> <p>The status register operates in this fashion for two reasons. The first is to give the host CPU the flexibility to read the status bits at any time. Second, when programming a string of bytes, a single status register query after programming the string may be more efficient, since it will return the accumulated error status of the entire string. See Section 3.2.3.1.</p>
90	Intelligent Identifier	<p>Puts the device into the intelligent identifier read mode, so that reading the device will output the manufacturer and device codes. (<math>A_0 = 0</math> for manufacturer, <math>A_0 = 1</math> for device, all other address inputs are ignored). See Section 3.2.2.</p>

**Table 7. Command Bus Definitions**

Command	Note	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array		Write	X	FFH			
Intelligent Identifier	2,4	Write	X	90H	Read	IA	IID
Read Status Register	3	Write	X	70H	Read	X	SRD
Clear Status Register	3	Write	X	50H			
Word/Byte Program	6,7	Write	PA	40H/10H	Write	PA	PD
Block Erase/Confirm	5	Write	BA	20H	Write	BA	D0H
Erase Suspend		Write	X	B0H			
Erase Resume		Write	X	D0H			

**ADDRESS**

BA = Block Address  
 IA = Identifier Address  
 PA = Program Address  
 X = Don't Care

**DATA**

SRD = Status Register Data  
 IID = Identifier Data  
 PD = Program Data

**NOTES:**

1. Bus operations are defined in Tables 3 and 4.
2. IA = Identifier Address:  $A_0 = 0$  for manufacturer code,  $A_0 = 1$  for device code.
3. SRD - Data read from Status Register.
4. IID = Intelligent Identifier Data. Following the Intelligent Identifier command, two read operations access manufacturer and device codes.
5. BA = Address within the block being erased.
6. PA = Address to be programmed. PD = Data to be programmed at location PA.
7. Either 40H or 10H commands is valid.
8. When writing commands to the device, the upper data bus [ $DQ_8-DQ_{15}$ ] = X which is either  $V_{IL}$  or  $V_{IH}$ , to minimize current draw.

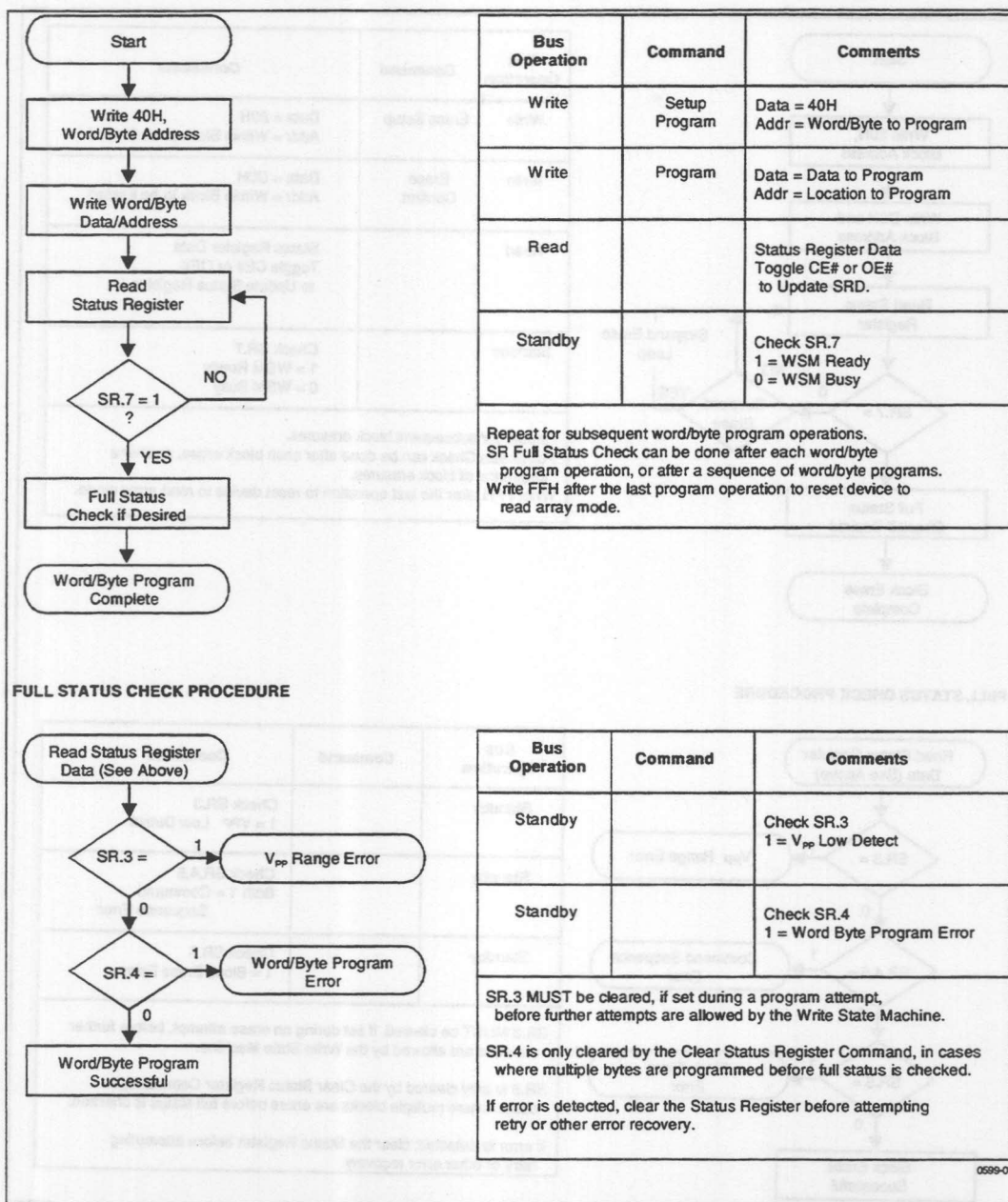
Table 8. Status Register Bit Definition

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

<b>NOTES:</b>							
<b>SR.7 WRITE STATE MACHINE STATUS</b>				Check WSM bit first to determine word/byte program or block erase completion, before checking Program or Erase Status bits.			
1 = Ready (WSMS)							
0 = Busy							
<b>SR.6 = ERASE-SUSPEND STATUS (ESS)</b>				When Erase Suspend is issued, WSM halts execution and sets both WSMS and ESS bits to "1." ESS bit remains set to "1" until an Erase Resume command is issued.			
1 = Erase Suspended							
0 = Erase In Progress/Completed							
<b>SR.5 = ERASE STATUS (ES)</b>				When this bit is set to "1," one of the following has occurred:			
1 = Error In Block Erasure				1. V <sub>PP</sub> out of range.			
0 = Successful Block Erase				2. WSM has applied the max number of erase pulses to the block and is still unable to verify successful block erasure.			
				3. Erase Setup command was followed by a command other than Erase Confirm.			
<b>SR.4 = PROGRAM STATUS (DWS)</b>				When this bit is set to "1," one of the following has occurred:			
1 = Error in Byte/Word Program				1. V <sub>PP</sub> out of range.			
0 = Successful Byte/Word Program				2. WSM has applied the max number of program pulses and is still unable to verify a successful program.			
				3. Erase Setup command was followed by a command other than Erase Confirm.			
<b>SR.3 = V<sub>PP</sub> STATUS (VPPS)</b>				The V <sub>PP</sub> Status bit does not provide continuous indication of V <sub>PP</sub> level. The WSM interrogates V <sub>PP</sub> level only after the Program or Erase command sequences have been entered, and informs the system if V <sub>PP</sub> is out of range. The V <sub>PP</sub> Status bit is not guaranteed to report accurate feedback between V <sub>PPLK</sub> and V <sub>PPH</sub> .			
1 = V <sub>PP</sub> Low Detect, Operation Abort							
0 = V <sub>PP</sub> OK							
<b>SR.2-SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</b>				These bits are reserved for future use and should be masked out when polling the Status Register.			




**Figure 7. Automated Word/Byte Program Flowchart**

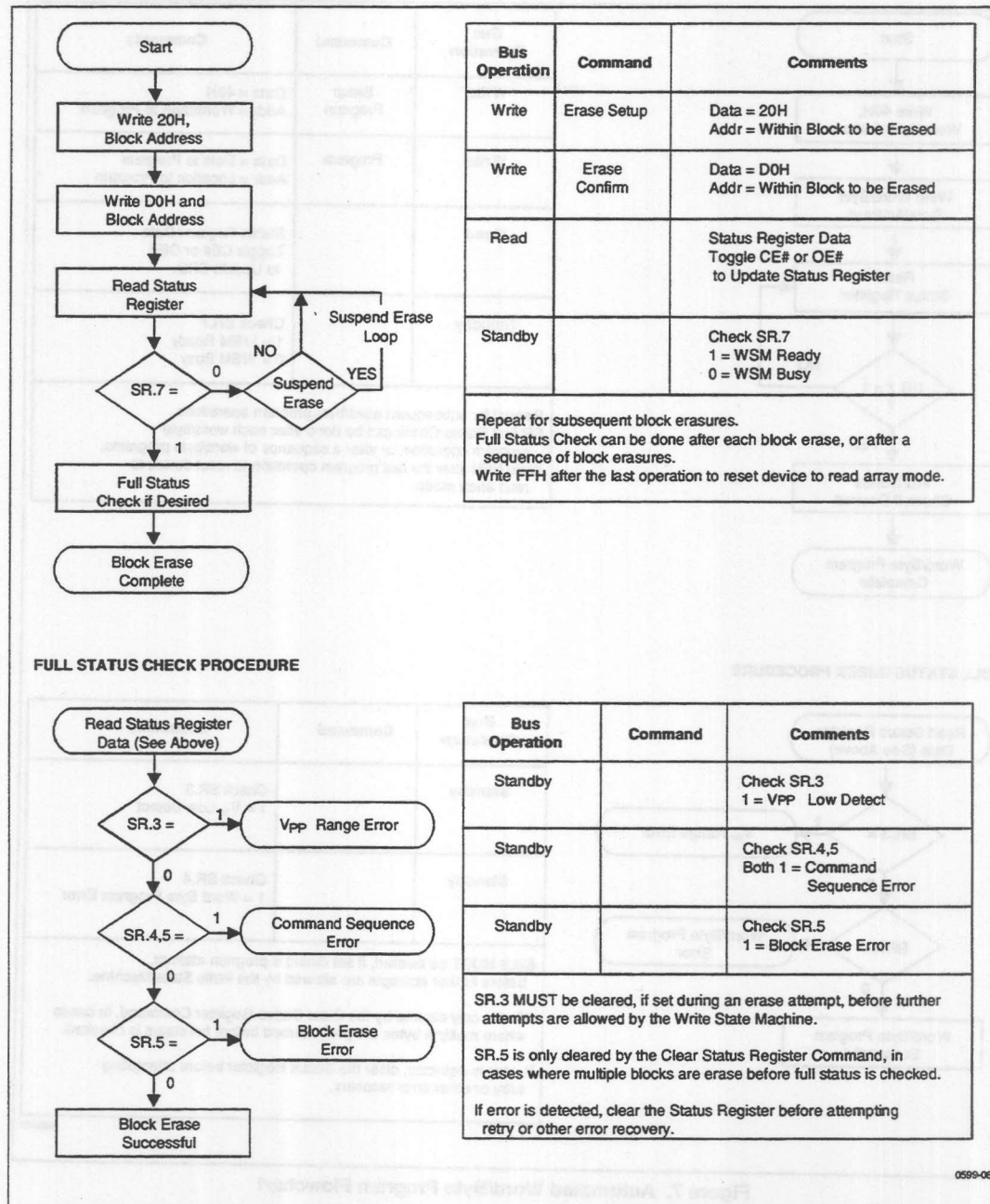


Figure 8. Automated Block Erase Flowchart

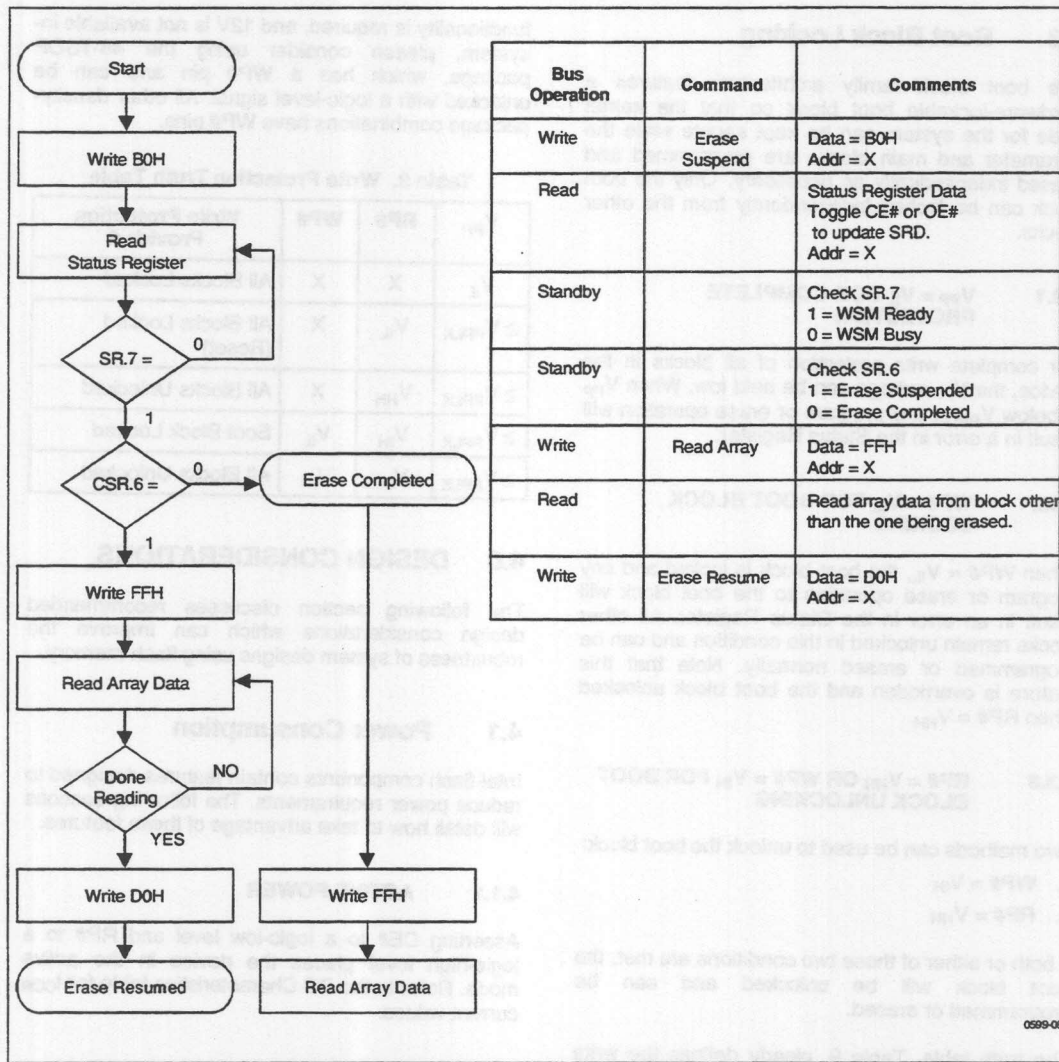


Figure 9. Erase Suspend/Resume Flowchart



### 3.3 Boot Block Locking

The boot block family architecture features a hardware-lockable boot block so that the kernel code for the system can be kept secure while the parameter and main blocks are programmed and erased independently as necessary. Only the boot block can be locked independently from the other blocks.

#### 3.3.1 $V_{PP} = V_{IL}$ FOR COMPLETE PROTECTION

For complete write protection of all blocks in the device, the  $V_{PP}$  voltage can be held low. When  $V_{PP}$  is below  $V_{PPLK}$ , any program or erase operation will result in an error in the Status Register.

#### 3.3.2 $WP\# = V_{IL}$ FOR BOOT BLOCK LOCKING

When  $WP\# = V_{IL}$ , the boot block is locked and any program or erase operation to the boot block will result in an error in the Status Register. All other blocks remain unlocked in this condition and can be programmed or erased normally. Note that this feature is overridden and the boot block unlocked when  $RP\# = V_{HH}$ .

#### 3.3.3 $RP\# = V_{HH}$ OR $WP\# = V_{IH}$ FOR BOOT BLOCK UNLOCKING

Two methods can be used to unlock the boot block:

1.  $WP\# = V_{IH}$
2.  $RP\# = V_{HH}$

If both or either of these two conditions are met, the boot block will be unlocked and can be programmed or erased.

The truth table, Table 9, clearly defines the write protection methods.

#### 3.3.4 NOTE FOR 8-MBIT 44-PSOP PACKAGE

The 8-Mbit in the 44-PSOP package does not have a  $WP\#$  because no other pins were available for the 8-Mbit upgrade address. Thus, in this density-package combination only,  $V_{HH}$  (12V) on  $RP\#$  is required to unlock the boot block and unlocking with a logic-level signal is not possible. If this unlocking

functionality is required, and 12V is not available in-system, please consider using the 48-TSOP package, which has a  $WP\#$  pin and can be unlocked with a logic-level signal. All other density-package combinations have  $WP\#$  pins.

Table 9. Write Protection Truth Table

$V_{PP}$	$RP\#$	$WP\#$	Write Protection Provided
$V_{IL}$	X	X	All Blocks Locked
$\geq V_{PPLK}$	$V_{IL}$	X	All Blocks Locked (Reset)
$\geq V_{PPLK}$	$V_{HH}$	X	All Blocks Unlocked
$\geq V_{PPLK}$	$V_{IH}$	$V_{IL}$	Boot Block Locked
$\geq V_{PPLK}$	$V_{IH}$	$V_{IH}$	All Blocks Unlocked

## 4.0 DESIGN CONSIDERATIONS

The following section discusses recommended design considerations which can improve the robustness of system designs using flash memory.

### 4.1 Power Consumption

Intel flash components contain features designed to reduce power requirements. The following sections will detail how to take advantage of these features.

#### 4.1.1 ACTIVE POWER

Asserting  $CE\#$  to a logic-low level and  $RP\#$  to a logic-high level places the device in the active mode. Refer to the DC Characteristics table for  $I_{CC}$  current values.

#### 4.1.2 AUTOMATIC POWER SAVINGS (APS)

Automatic Power Savings (APS) provides low-power operation in active mode. Power Reduction Control (PRC) circuitry allows the device to put itself into a low current state when not being accessed. After data is read from the memory array, PRC logic controls the device's power consumption by entering the APS mode where typical  $I_{CC}$  current is less than 1 mA. The device stays in this static state with outputs valid until a new location is read.

#### 4.1.3 STANDBY POWER

When CE# is at a logic-high level ( $V_{IH}$ ), and the device is not programming or erasing, the memory enters in standby mode, which disables much of the device's circuitry and substantially reduces power consumption. Outputs (DQ<sub>0</sub>–DQ<sub>15</sub> or DQ<sub>0</sub>–DQ<sub>7</sub>) are placed in a high-impedance state independent of the status of the OE# signal. When CE# is at logic-high level during program or erase operations, the device will continue to perform the operation and consume corresponding active power until the operation is completed.

#### 4.1.4 DEEP POWER-DOWN MODE

The Smart 5 boot block family supports a low typical  $I_{CCD}$  in deep power-down mode, which turns off all circuits to save power. This mode is activated by the RP# pin when it is at a logic-low ( $GND \pm 0.2V$ ). Note: BYTE# pin must be at CMOS levels to meet the  $I_{CCD}$  specification.

During read modes, the RP# pin going low de-selects the memory and places the output drivers in a high impedance state. Recovery from the deep power-down state, requires a minimum access time of  $t_{PHQV}$ . RP# transitions to  $V_{IL}$ , or turning power off to the device will clear the Status Register.

During an program or erase operation, RP# going low for time  $t_{PLPH}$  will abort the operation, but the location's memory contents will no longer valid and additional timing must be met. See Section 3.1.5 and 6.1 for additional information.

### 4.2 Power-Up/Down Operation

The device protects against accidental block erasure or programming during power transitions. Power supply sequencing is not required, so either  $V_{PP}$  or  $V_{CC}$  can power-up first. The CUI defaults to the read mode after power-up, but the system must drop CE# low or present an address to receive valid data at the outputs.

A system designer must guard against spurious writes when  $V_{CC}$  voltages are above  $V_{LKO}$  and  $V_{PP}$  is active. Since both WE# and CE# must be low for a command write, driving either signal to  $V_{IH}$  will inhibit writes to the device. Additionally, alteration of memory can only occur after successful completion of a two-step command sequences. The device is also disabled until RP# is brought to  $V_{IH}$ , regardless of the state of its control inputs. By holding the

device in reset (RP# connected to system PowerGood) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

#### 4.2.1 RP# CONNECTED TO SYSTEM RESET

Using RP# properly during system reset is important with automated program/erase devices because the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization would not occur because the flash memory may in a mode other than Read Array. Intel's Flash memories allow proper CPU initialization following a system reset by connecting the RP# pin to the same RESET# signal that resets the system CPU.

### 4.3 Board Design

#### 4.3.1 POWER SUPPLY DECOUPLING

Flash memory's switching characteristics require careful decoupling methods. System designers should consider three supply current issues: standby current levels ( $I_{CCS}$ ), active current levels ( $I_{CCR}$ ), and transient peaks produced by falling and rising edges of CE#.

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1  $\mu F$  ceramic capacitor connected between  $V_{CC}$  and GND, and between  $V_{PP}$  and GND. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads.

#### 4.3.2 $V_{PP}$ TRACE ON PRINTED CIRCUIT BOARDS

In-system updates to the flash memory requires special consideration of the  $V_{PP}$  power supply trace by the printed circuit board designer. Since the  $V_{PP}$  pin supplies the current for programming and erasing, it should have similar trace widths and layout considerations as given to the  $V_{CC}$  power supply trace. Adequate  $V_{PP}$  supply traces, and decoupling capacitors placed adjacent to the component, will decrease spikes and overshoots.

## PRODUCT PREVIEW

## 5.0 SPECIFICATIONS

### 5.1 Absolute Maximum Ratings\*

#### Commercial Operating Temperature

During Read/Erase/Program .....0°C to +70°C

Temperature Under Bias .....-10°C to +80°C

#### Extended Operating Temperature

During Read/Erase/Program ....-40°C to +85°C

Temperature Under Bias .....-40°C to +85°C

Storage Temperature.....-65°C to +125°C

#### Voltage on Any Pin

(except  $V_{CC}$ ,  $V_{PP}$ ,  $A_9$  and  $RP\#$ )

with Respect to GND .....-2.0V to +7.0V(2)

#### Voltage on Pin $RP\#$ or Pin $A_9$

with Respect to GND ..... -2.0V to +13.5V(2,3)

#### $V_{PP}$ Program Voltage with Respect

to GND during Block Erase

and Word/Byte Program .... -2.0V to +14.0V(2,3)

#### $V_{CC}$ Supply Voltage

with Respect to GND .....-2.0V to +7.0V(2)

Output Short Circuit Current ..... 100 mA (4)

### 5.2 Test Conditions

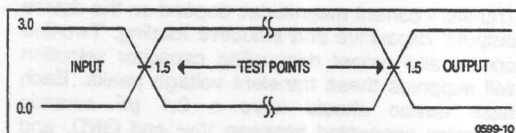


Figure 10. High Speed Test Waveform

NOTE: AC test inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 ns.

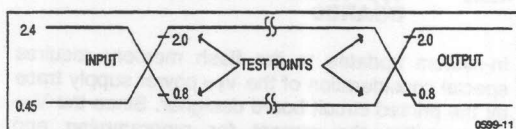


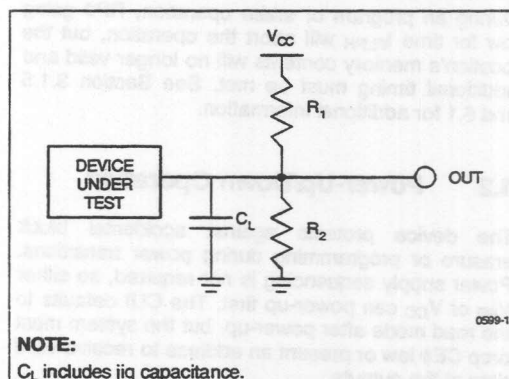
Figure 11. Standard Test Waveform

NOTE: AC test inputs driven at  $V_{OH}$  (2.4  $V_{TTL}$ ) for logic "1" and  $V_{OL}$  (0.45  $V_{TTL}$ ) for logic "0." Input timing begins at  $V_{IH}$  (2.0  $V_{TTL}$ ) and  $V_{IL}$  (0.8  $V_{TTL}$ ). Output timing ends at  $V_{IH}$  and  $V_{IL}$ . Input rise and fall times (10% to 90%) <10 ns.

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

\* **WARNING:** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20 ns. Maximum DC voltage on input/output pins is  $V_{CC} + 0.5V$  which, during transitions, may overshoot to  $V_{CC} + 2.0V$  for periods <20 ns.
3. Maximum DC voltage on  $V_{PP}$  may overshoot to +14.0V for periods <20 ns. Maximum DC voltage on  $RP\#$  or  $A_9$  may overshoot to 13.5V for periods <20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.



NOTE:

$C_L$  includes jig capacitance.

Figure 12. Test Configuration

#### Test Configuration Component Values

Test Configuration	$C_L$ (pF)	$R_1$ ( $\Omega$ )	$R_2$ ( $\Omega$ )
5V Standard Test	100	580	390
5V High-Speed Test	30	580	390



### 5.3 Operating Conditions

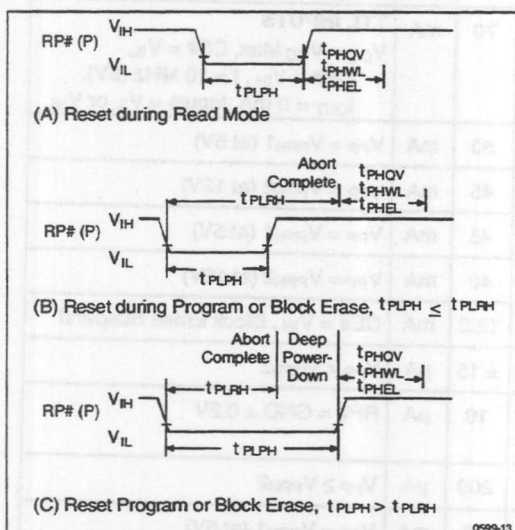
**Table 10. Temperature and V<sub>CC</sub> Operating Conditions**

Symbol	Parameter	Notes	Min	Max	Units
T <sub>A</sub>	Commercial Operating Temperature		0	+70	°C
	Extended Operating Temperature		-40	+85	°C
V <sub>CC</sub>	5V V <sub>CC</sub> Supply Voltage (10%)	1	4.50	5.50	Volts
	5V V <sub>CC</sub> Supply Voltage (5%)	2	4.75	5.25	Volts
V <sub>PP</sub>	5V V <sub>PP</sub> Supply Voltage (10%)	1	4.50	5.50	Volts
	12V V <sub>CC</sub> Supply Voltage (5%)	1	11.4	12.6	Volts

**NOTES:**

1. 10% V<sub>CC</sub> specifications apply to the standard test configuration (Figures 11 and 12).
2. 5% V<sub>CC</sub> specifications apply to the high-speed test configuration (Figures 10 and 12).

### 5.4 Reset Operations


**Figure 13. AC Waveform for Reset Operation**
**Table 11. Reset Specifications<sup>(1)</sup>**

Sym	Parameter	Min	Max	Unit
t <sub>PLPH</sub>	RP# Pulse Low Time	60		ns
t <sub>PLRH</sub>	RP# Low to Reset during Prog/Erase		12	μs

1. If RP# is tied to V<sub>CC</sub>, these specs are not applicable.
2. These specifications are valid for all product versions (packages and speeds).
3. If RP# is asserted while a program or block erase, is not executing, the reset will complete within t<sub>PLPH</sub>.
4. A reset time, t<sub>PHQV</sub>, is required after t<sub>PLRH</sub> until outputs are valid. See Section 3.1.5 for detailed information.

## 5.6 Electrical Specifications

Table 12. DC Characteristics (Commercial and Extended Temperature)

Sym	Parameter	Temp	Comm		Extended		Unit	Test Condition
		Note	Typ	Max	Typ	Max		
$I_{IL}$	Input Load Current	1		$\pm 1.0$		$\pm 1.0$	$\mu A$	$V_{CC} = V_{CC} \text{ Max}, V_{IN} = V_{CC} \text{ or GND}$
$I_{LO}$	Output Leakage Current	1		$\pm 10$		$\pm 10$	$\mu A$	$V_{CC} = V_{CC} \text{ Max}, V_{IN} = V_{CC} \text{ or GND}$
$I_{CCS}$	$V_{CC}$ Standby Current	1,3		2.0		2.5	mA	$V_{CC} = V_{CC} \text{ Max}, CE\# = RP\# =$ $BYTE\# = WP\# = V_{IH}$
				130		150	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ $CE\# = RP\# = V_{CC} \pm 0.2V$
$I_{CCD}$	$V_{CC}$ Deep Power-Down Current	1		8		8	$\mu A$	$V_{CC} = V_{CC} \text{ Max}, V_{IN} = V_{CC} \text{ or GND}$ $RP\# = GND \pm 0.2V$
$I_{CCR}$	$V_{CC}$ Read Current (Word or Byte Mode)	1,5,6		60		65	mA	<b>CMOS INPUTS</b> $V_{CC} = V_{CC} \text{ Max}, CE\# = GND,$ $OE\# = V_{CC}, f = 10 \text{ MHz (5V)},$ $I_{OUT} = 0 \text{ mA}, \text{Inputs} = GND \text{ or } V_{CC}$
				65		70	mA	<b>TTL INPUTS</b> $V_{CC} = V_{CC} \text{ Max}, CE\# = V_{IL},$ $OE\# = V_{IH}, f = 10 \text{ MHz (5V)},$ $I_{OUT} = 0 \text{ mA}, \text{Inputs} = V_{IL} \text{ or } V_{IH}$
$I_{CCW}$	$V_{CC}$ Program Current (Word or Byte Mode)	1,4		50		50	mA	$V_{PP} = V_{PPH1} \text{ (at 5V)}$
				45		45	mA	$V_{PP} = V_{PPH2} \text{ (at 12V)}$
$I_{CCE}$	$V_{CC}$ Erase Current	1,4		35		45	mA	$V_{PP} = V_{PPH1} \text{ (at 5V)}$
				30		40	mA	$V_{PP} = V_{PPH2} \text{ (at 12V)}$
$I_{CCES}$	$V_{CC}$ Erase Susp Current	1,2		10		12.0	mA	$CE\# = V_{IH}, \text{Block Erase Suspend}$
$I_{PPS}$	$V_{PP}$ Standby Current	1		$\pm 10$		$\pm 15$	$\mu A$	$V_{PP} < V_{PPH2}$
$I_{PPD}$	$V_{PP}$ Deep Power-Down Current	1		5.0		10	$\mu A$	$RP\# = GND \pm 0.2V$
$I_{PPR}$	$V_{PP}$ Read Current	1		200		200	$\mu A$	$V_{PP} \geq V_{PPH2}$
$I_{PPW}$	$V_{PP}$ Program Current (Word or Byte Mode)	1,4		25		30	mA	$V_{PP} = V_{PPH1} \text{ (at 5V)}$
				20		25		$V_{PP} = V_{PPH2} \text{ (at 12V)}$
$I_{PPE}$	$V_{PP}$ Erase Current	1,4		20		25	mA	$V_{PP} = V_{PPH1} \text{ (at 5V)}$
				15		20		$V_{PP} = V_{PPH2} \text{ (at 12V)}$
$I_{PPES}$	$V_{PP}$ Erase Susp Current	1		200		200	$\mu A$	$V_{PP} = V_{PPH}, \text{Block Erase Suspend}$
$I_{RP\#}$	$RP\#$ Unlock Current	1,4		500		500	$\mu A$	$RP\# = V_{HH} \text{ (to unlock Boot Block)}$
$I_{ID}$	$A_9$ Identifier Current	1,4		500		500	$\mu A$	$A_9 = V_{ID}$

**Table 12. DC Characteristics (Commercial and Extended Temperature) (Continued)**

Sym	Parameter	Temp	Comm/Ext		Unit	Test Condition
		Note	Min	Max		
V <sub>ID</sub>	A <sub>9</sub> Intelligent Identifier Voltage		11.4	12.6	V	
V <sub>IL</sub>	Input Low Voltage		-0.5	0.8	V	
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 0.5V	V	
V <sub>OL</sub>	Output Low Voltage			0.45	V	V <sub>CC</sub> = V <sub>CC</sub> Min, I <sub>OL</sub> = 5.8 mA
V <sub>OH1</sub>	Output High Voltage (TTL)		2.4		V	V <sub>CC</sub> = V <sub>CC</sub> Min, I <sub>OH</sub> = -2.5 mA
V <sub>OH2</sub>	Output High Voltage (CMOS)		0.85 x V <sub>CC</sub>		V	V <sub>CC</sub> = V <sub>CC</sub> Min, I <sub>OH</sub> = -2.5 mA
			V <sub>CC</sub> - 0.4V		V	V <sub>CC</sub> = V <sub>CC</sub> Min, I <sub>OH</sub> = -100 µA
V <sub>PPLK</sub>	V <sub>PP</sub> Lock-Out Voltage	3	0.0	1.5	V	Complete Data Protection
V <sub>PPH1</sub>	V <sub>PP</sub> (Prog/Erase Operations)		4.5	5.5	V	V <sub>PP</sub> at 5V
V <sub>PPH2</sub>	V <sub>PP</sub> (Prog/Erase Operations)		11.4	12.6	V	V <sub>PP</sub> at 12V
V <sub>LKO</sub>	V <sub>CC</sub> Erase/Prog Lock Voltage		2.0		V	
V <sub>HH</sub>	RP# Unlock Voltage		11.4	12.6	V	Boot Block Program/Erase

**NOTES:**

1. All currents are in RMS unless otherwise noted. Typical values at V<sub>CC</sub> = 5.0V, T = +25°C. These currents are valid for all product versions (packages and speeds).
2. I<sub>CCES</sub> is specified with the device deselected. If the device is read while in erase suspend mode, current draw is the sum of I<sub>CCES</sub> and I<sub>CCR</sub>.
3. Block erases and word/byte program operations are inhibited when V<sub>PP</sub> = V<sub>PPLK</sub>, and not guaranteed in the range between V<sub>PPH1</sub> and V<sub>PPLK</sub>.
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces I<sub>CCR</sub> to less than 1 mA typical, in static operation.
6. CMOS Inputs are either V<sub>CC</sub> ± 0.2V or GND ± 0.2V. TTL Inputs are either V<sub>IL</sub> or V<sub>IH</sub>.

**Table 13. Capacitance (T<sub>A</sub> = 25 °C, f = 1 MHz)**

Symbol	Parameter	Note	Typ	Max	Unit	Conditions
C <sub>IN</sub>	Input Capacitance	4	6	8	pF	V <sub>IN</sub> = 0V
C <sub>OUT</sub>	Output Capacitance	4, 7	10	12	pF	V <sub>OUT</sub> = 0V

1. Sampled, not 100% tested.



Table 14. AC Characteristics: Read Operations (Commercial and Extended Temperature)

#	Sym	Parameter			Temp	Commercial						Extended		Unit
					Speed	-60/-70				-80/-90		-80/-90		
					V <sub>CC</sub>	5V ± 5% (4)		5V±10% (5)		5V± 10%(5)		5V± 10%(5)		
					Load	30 pF		100 pF		100 pF		100 pF		
					Notes	Min	Max	Min	Max	Min	Max	Min	Max	
R1	t <sub>AVAV</sub>	Read Cycle	2-, 4-Mbit		60		70		80		80		ns	
		Time	8-Mbit		70		80		90		90		ns	
R2	t <sub>AVQV</sub>	Address to	2-, 4-Mbit			60		70		80		80	ns	
		Output Delay	8-Mbit			70		80		90		90	ns	
R3	t <sub>ELQV</sub>	CE# to	2-, 4-Mbit	2		60		70		80		80	ns	
		Output Delay	8-Mbit			70		80		90		90	ns	
R4	t <sub>GLQV</sub>	OE# to Output Delay			2		30		35		40		40	ns
R5	t <sub>PHQV</sub>	RP# to Output Delay					450		450		450		450	ns
R6	t <sub>ELQX</sub>	CE# to Output in Low Z			3	0		0		0		0		ns
R7	t <sub>GLQX</sub>	OE# to Output in Low Z			3	0		0		0		0		ns
R8	t <sub>EHQZ</sub>	CE# to Output in High Z			3		20		20		20		25	ns
R9	t <sub>GHQZ</sub>	OE# to Output in High Z			3		20		20		20		25	ns
R10	t <sub>OH</sub>	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First			3	0		0		0		0		ns

## NOTES:

1. See AC Input/Output Reference Waveform for timing measurements.
2. OE# may be delayed up to t<sub>CE</sub>-t<sub>OE</sub> after the falling edge of CE# without impact on t<sub>CE</sub>.
3. Sampled, but not 100% tested.
4. See Test Configurations (Figure 12), 5V High-Speed Test component values.
5. See Test Configurations (Figure 12), 5V Standard Test component values.
6. Dynamic BYTE# switching between word and byte modes is not supported. Mode changes must be made when the device is in deep power-down or powered down.

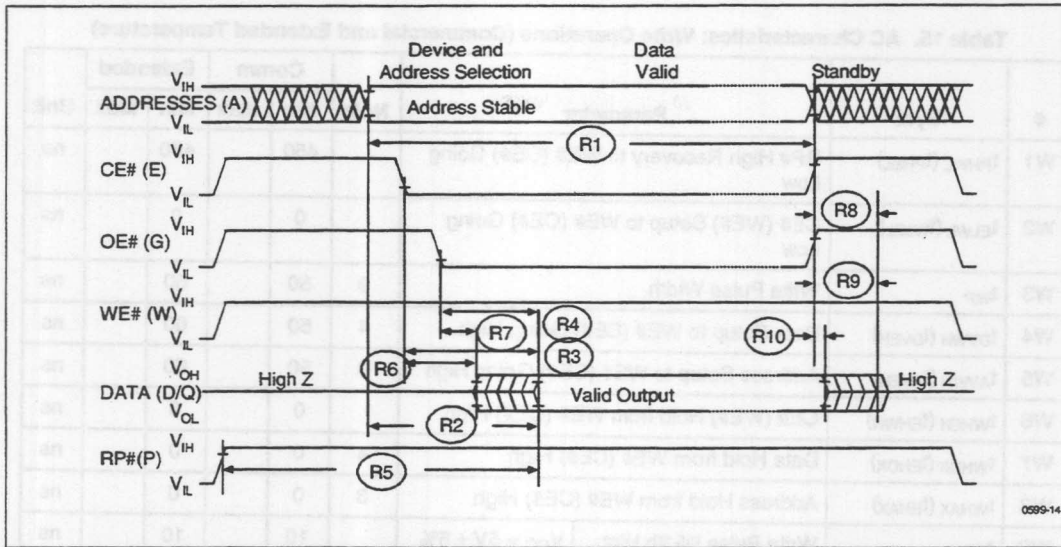


Figure 14. AC Waveforms for Read Operations

Table 15. AC Characteristics: Write Operations (Commercial and Extended Temperature)

#	Sym	Parameter	Note	Comm		Extended		Unit
				Min	Max	Min	Max	
W1	$t_{PHWL}$ ( $t_{PHEL}$ )	RP# High Recovery to WE# (CE#) Going Low		450		450		ns
W2	$t_{ELWL}$ ( $t_{WLEL}$ )	CE# (WE#) Setup to WE# (CE#) Going Low		0		0		ns
W3	$t_{WP}$	Write Pulse Width	9	50		60		ns
W4	$t_{DVWH}$ ( $t_{DVEH}$ )	Data Setup to WE# (CE#) Going High	4	50		60		ns
W5	$t_{AVWH}$ ( $t_{AVEH}$ )	Address Setup to WE# (CE#) Going High	3	50		60		ns
W6	$t_{WHEH}$ ( $t_{EHWH}$ )	CE# (WE#) Hold from WE# (CE#) High		0		0		ns
W7	$t_{WHDx}$ ( $t_{EHDX}$ )	Data Hold from WE# (CE#) High	4	0		0		ns
W8	$t_{WHAX}$ ( $t_{EHAX}$ )	Address Hold from WE# (CE#) High	3	0		0		ns
W9	$t_{WPH}$	Write Pulse Width High	$V_{CC} = 5V \pm 5\%$	10		10		ns
			$V_{CC} = 5V \pm 10\%$	20		20		ns
W10	$t_{PHHWH}$ ( $t_{PHHEH}$ )	RP# $V_{HH}$ Setup to WE# (CE#) Going High	6,8	100		100		ns
W11	$t_{VPWH}$ ( $t_{VPEH}$ )	$V_{PP}$ Setup to WE# (CE#) Going High	5,8	100		100		ns
W12	$t_{QVPH}$	RP# $V_{HH}$ Hold from Valid SRD	6,8	0		0		ns
W13	$t_{QVVL}$	$V_{PP}$ Hold from Valid SRD	5,8	0		0		ns
W14	$t_{PHBR}$	Boot Block Lock Delay	7,8		100		100	ns

## NOTES:

- Read timing characteristics during program and erase operations are the same as during read-only operations. Refer to AC characteristics for read operations.
- The on-chip WSM completely automates program/erase operations; program/erase algorithms are now controlled internally which includes verify operations.
- Refer to command definition table for valid  $A_{IN}$ . (Table 7)
- Refer to command definition table for valid  $D_{IN}$ . (Table 7)
- Program/erase durations are measured to valid SRD data (successful operation, SR.7 = 1).
- For boot block program/erase, RP# should be held at  $V_{HH}$  or WP# should be held at  $V_{HH}$  until operation completes successfully.
- Time  $t_{PHBR}$  is required for successful locking of the boot block.
- Sampled, but not 100% tested.
- Write pulse width ( $t_{WP}$ ) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). Hence,  $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$ .
- Write pulse width high ( $t_{WPH}$ ) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low first). Hence,  $t_{WPH} = t_{WHWL} = t_{EHLE} = t_{WHEL} = t_{EHWL}$ .



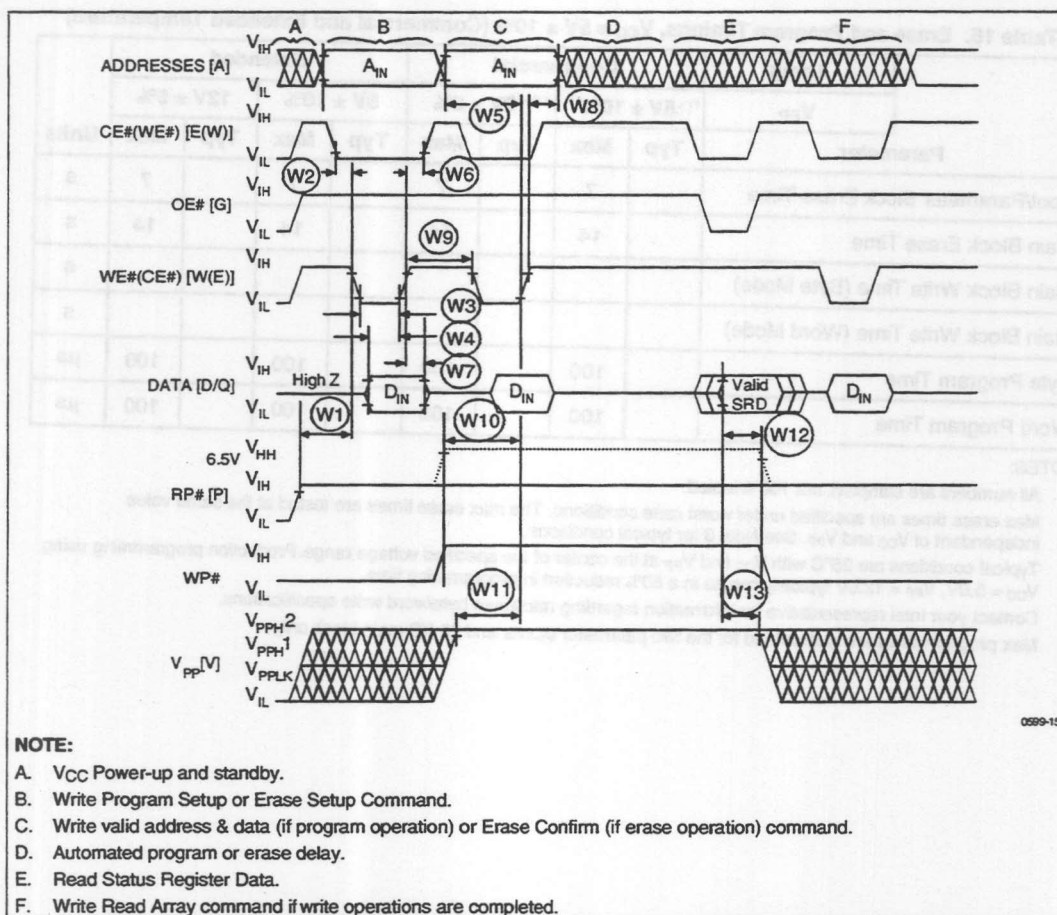


Figure 15. AC Waveforms for Write Operations

Table 16. Erase and Program Timings,  $V_{CC} = 5V \pm 10\%$  (Commercial and Extended Temperature)

	Temp	Commercial				Extended				Units
	V <sub>PP</sub>	5V ± 10%		12V ± 5%		5V ± 10%		12V ± 5%		
Parameter		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Boot/Parameter Block Erase Time			7		7		7		7	s
Main Block Erase Time			14		14		14		14	s
Main Block Write Time (Byte Mode)										s
Main Block Write Time (Word Mode)										s
Byte Program Time			100		100		100		100	μs
Word Program Time			100		100		100		100	μs

## NOTES:

1. All numbers are sampled, not 100% tested.
2. Max erase times are specified under worst case conditions. The max erase times are tested at the same value independent of  $V_{CC}$  and  $V_{PP}$ . See Note 3 for typical conditions.
3. Typical conditions are 25°C with  $V_{CC}$  and  $V_{PP}$  at the center of the specified voltage range. Production programming using  $V_{CC} = 5.0V$ ,  $V_{PP} = 12.0V$  typically results in a 60% reduction in programming time.
4. Contact your Intel representative for information regarding maximum byte/word write specifications.
5. Max program times are guaranteed for the two parameter blocks and 96-KB main block only.

## APPENDIX A ORDERING INFORMATION

E28F400B5 - T60

#### Operating Temperature

T = Extended Temp

Blank = Commercial Temp

#### Package

E = TSOP

PA = 44-Lead PSOP

TB = Ext. Temp 44-Lead PSOP

#### Product line designator

for all Intel Flash products

#### Density / Organization

X00 = x8/x16 Selectable (X = 2, 4, 8)

Access Speed ns

T = Top Boot

B = Bottom Boot

Voltage Options (V<sub>PP</sub> / V<sub>CC</sub>)

5 = (5 or 12 / 5)

Architecture

B = Boot Block

#### VALID COMBINATIONS

##### Commercial

2M

##### 44-Lead PSOP

PA28F200B5T60

PA28F200B5B60

PA28F200B5T80

PA28F200B5B80

4M

PA28F400B5T60

PA28F400B5B60

PA28F400B5T80

PA28F400B5B80

8M

PA28F800B5T70

PA28F800B5B70

PA28F800B5T90

PA28F800B5B90

##### 48-Lead TSOP

E28F200B5T60

E28F200B5B60

E28F200B5T80

E28F200B5B80

E28F400B5T60

E28F400B5B60

E28F400B5T80

E28F400B5B80

E28F800B5T70

E28F800B5B70

E28F800B5T90

E28F800B5B90

##### Extended

2M

TB28F200B5T80

TB28F200B5B80

4M

TB28F400B5T80

TB28F400B5B80

8M

TB28F800B5T90

TB28F800B5B90

TE28F200B5T80

TE28F200B5B80

TE28F400B5T80

TE28F400B5B80

TE28F800B5T90

TE28F800B5B90



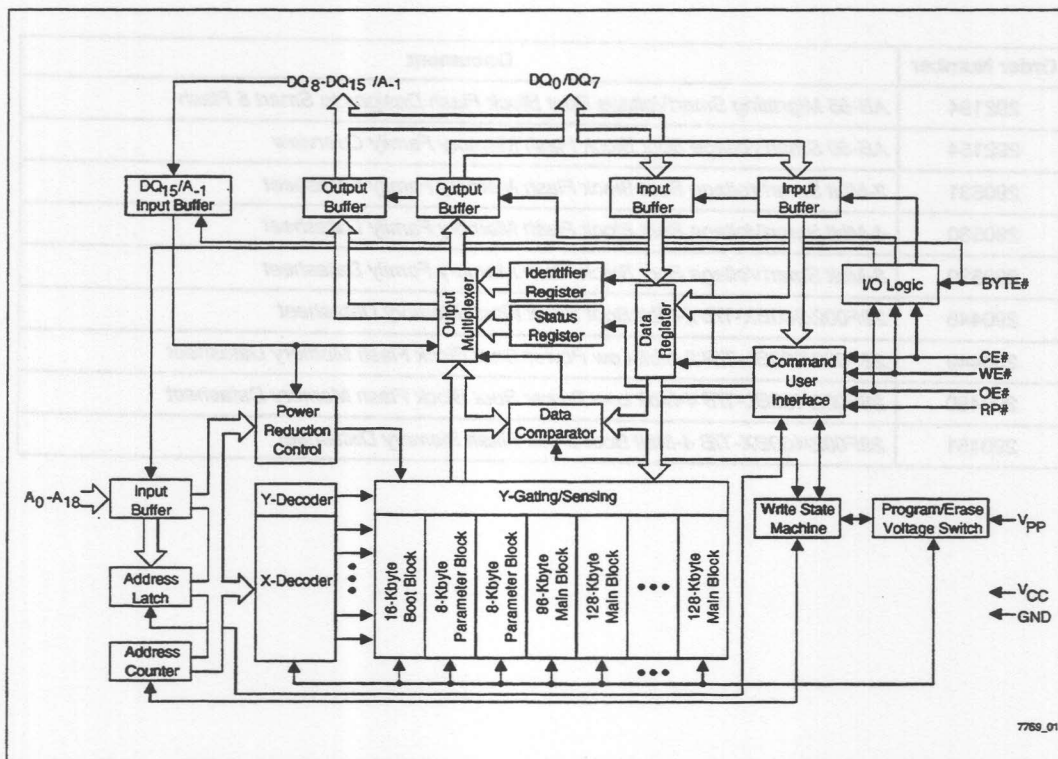
## APPENDIX B

### WRITE STATE MACHINE: CURRENT-NEXT STATE CHART

Write State Machine Current/Next States

Current State	SR.7	Data When Read	Read Array (FFH)	Command Input (and Next State)							
				Program Setup (10/40H)	Erase Setup (20H)	Erase Confirm (D0H)	Erase Susp. (B0H)	Erase Resume (D0H)	Read Status (70H)	Clear Status (50H)	Read ID (90H)
Read Array	"1"	Array	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read ID
Program Setup	"1"	Status	Program (Command Input = Data to be programmed)								
Program: Not Complete	"0"	Status	Program								
Program: Complete	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read ID
Erase Setup	"1"	Status	Erase Command Error			Erase	Erase Cmd. Error	Erase	Erase Command Error		
Erase Cmd. Error	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read ID
Erase: Not Complete	"0"	Status	Erase				Erase Susp. to Status	Erase			
Erase: Complete	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read ID
Erase Suspend to Status	"1"	Status	Erase Susp. to Array	Res'd.	Erase Susp. to Array	Erase	Erase Susp. to Array	Erase	Erase Susp. to Status	Erase Susp. to Array	Res'd.
Erase Suspend to Array	"1"	Array	Erase Susp. to Array	Res'd.	Erase Susp. to Array	Erase	Erase Susp. to Array	Erase	Erase Susp. to Status	Erase Susp. to Array	Res'd.
Read Status	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read ID
Read Identifier	"1"	ID	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read ID

## APPENDIX C PRODUCT BLOCK DIAGRAM



## APPENDIX D ADDITIONAL INFORMATION

Order Number	Document
292194	<i>AB-65 Migrating SmartVoltage Boot Block Flash Designs to Smart 5 Flash</i>
292154	<i>AB-60 SmartVoltage Boot Block Flash Memory Family Overview</i>
290531	<i>2-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet</i>
290530	<i>4-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet</i>
290539	<i>8-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet</i>
290448	<i>28F002/200BX-T/B 2-Mbit Boot Block Flash Memory Datasheet</i>
290449	<i>28F002/200BL-T/B 2-Mbit Low Power Boot Block Flash Memory Datasheet</i>
290450	<i>28F002/400BL-T/B 4-Mbit Low Power Boot Block Flash Memory Datasheet</i>
290451	<i>28F002/400BX-T/B 4-Mbit Boot Block Flash Memory Datasheet</i>



# Intel High Value FlashFile™ Memory Family

## New Design Focus Products

			Access Time (ns)	Access Time (ns)	Access Time (ns)			
Density	Product	Organization	4.5 – 5.5V V <sub>CC</sub>	3.0 – 3.6V V <sub>CC</sub>	2.7 – 3.6V V <sub>CC</sub>	V <sub>PP</sub>	Package	Number Pins
<b>Commercial Temperature</b>								
<b>*NEW Introducing Intel StrataFlash (TM) Memory - 2x the bits in 1x the space</b>								
64 Mb	28F640J5*	8M x 8 or 4M x 16	150			5V	SSOP, µBGA*	56
	28F640J5- L*	8M x 8 or 4M x 16	150 2.7V I/O			5V	µBGA	56
32 Mb	28F320J5*	4M x 8 or 2M x 16	120			5V	TSOP, SSOP, µBGA	56
	28F320J5- L*	4M x 8 or 2M x 16	120 207V I/O			5V	TSOP	56
16 Mb	28F016S3	2M x 8		120, 150	150, 170	3.3V or 12V	TSOP, µBGA	40
	28F016S3	2M x 8		120, 150	150, 170	3.3V or 12V	PSOP	44
	28F016S5	2M x 8	95, 120			5V or 12V	TSOP	40
	28F016S5	2M x 8	95, 120			5V or 12V	PSOP	44
8 Mb	28F008S3	1M x 8		120, 150	150, 170	3.3V or 12V	TSOP, µBGA	40
	28F008S3	1M x 8		120, 150	150, 170	3.3V or 12V	PSOP	44
	28F008S5	1M x 8	85, 120			5V or 12V	TSOP	40
	28F008S5	1M x 8	85, 120			5V or 12V	PSOP	44
4 Mb	28F004S3	512K x 8		120, 150	150, 170	3.3V or 12V	TSOP	40
	28F004S5	512K x 8	85, 120			5V or 12V	TSOP	40
<b>Extended Temperature</b>								
32 Mb	28F320S3 *	4M x 8 or 2M x 16		110, 140	130, 160	2.7V, 3.3V or 5V	SSOP, µBGA	56
	28F320S5 *	4M x 8 or 2M x 16	90, 120			5V	SSOP, µBGA	56
16 Mb	28F160S3 *	2M x 8 or 1M x 16		100, 130	120, 150	2.7V, 3.3V or 5V	TSOP, SSOP, µBGA	56
	28F160S5 *	2M x 8 or 1M x 16	70, 100			5V	TSOP, SSOP, µBGA	56
	28F016S5	2M x 8	110			5V or 12V	TSOP	40
	28F016S5	2M x 8	110			5V or 12V	PSOP	44



	28F016S3	2M x 8		150	170	3.3V or 12V	TSOP	40
	28F016S3	2M x 8		150	170	3.3V or 12V	PSOP	44
8 Mb	28F008S3	1M x 8		150	170	3.3V or 12V	TSOP	40
	28F008S3	1M x 8		150	170	3.3V or 12V	PSOP	44
	28F008S5	1M x 8	100			5V or 12V	TSOP	40
	28F008S5	1M x 8	100			5V or 12V	PSOP	44
4 Mb	28F004S5	512K x 8	100			5V or 12V	TSOP	40
	28F004S3	512K x 8		150	170	3.3V or 12V	TSOP	40

\*Common Flash Interface (CFI) compliant products, for easy software upgrade.

## Availability Schedule

Products not listed here are in full production.

Product	Package	Samples	Production
<b>Commercial Temperature</b>			
28F640J5/-L	SSOP μBGA	Now Q1'98	Q1'98 Q2'98
28F320J5/-L	TSOP SSOP, μBGA	Q1'98 2H'98	Q2'98 2H'98
28F016S3	μBGA	Q4'97	Q1'98
<b>Extended Temperature</b>			
28F320S3	SSOP μBGA	Q4'97 1998	Q1'98 1998
28F320S5	SSOP μBGA	Q4'97 1998	Q1'98 1998
28F160S3	TSOP SSOP μBGA	Now Now 1998	Q4'97 Q4'97 1998
28F160S5	TSOP SSOP μBGA	Now Now 1998	Q4'97 Q4'97 1998







## BYTE-WIDE SMART 5 FlashFile™ MEMORY FAMILY 4, 8, AND 16 MBIT

28F004S5, 28F008S5, 28F016S5

*Includes Commercial and Extended Temperature Specifications*

- **SmartVoltage Technology**
  - Smart 5 Flash: 5V V<sub>CC</sub> and 5V or 12V V<sub>PP</sub>
- **High-Performance**
  - 4, 8 Mbit: 85 ns Read Access Time
  - 16 Mbit: 95 ns Read Access Time
- **Enhanced Data Protection Features**
  - Absolute Protection with V<sub>PP</sub> = GND
  - Flexible Block Locking
  - Block Write Lockout during Power Transitions
- **Enhanced Automated Suspend Options**
  - Program Suspend to Read
  - Block Erase Suspend to Program
  - Block Erase Suspend to Read
- **Industry-Standard Packaging**
  - 40-Lead TSOP, 44-Lead PSOP
- **High-Density 64-Kbyte Symmetrical Erase Block Architecture**
  - 4 Mbit: Eight Blocks
  - 8 Mbit: Sixteen Blocks
  - 16 Mbit: Thirty-Two Blocks
- **Extended Cycling Capability**
  - 100,000 Block Erase Cycles
- **Low Power Management**
  - Deep Power-Down Mode
  - Automatic Power Savings Mode Decreases I<sub>CC</sub> in Static Mode
- **Automated Program and Block Erase**
  - Command User Interface
  - Status Register
- **SRAM-Compatible Write Interface**
- **ETOX™ V Nonvolatile Flash Technology**

Intel's byte-wide Smart 5 FlashFile™ memory family renders a variety of density offerings in the same package. The 4-, 8-, and 16-Mbit byte-wide FlashFile memories provide high-density, low-cost, nonvolatile, read/write storage solutions for a wide range of applications. Their symmetrically-blocked architecture, flexible voltage, and extended cycling provide highly flexible components suitable for resident flash arrays, SIMMs, and memory cards. Enhanced suspend capabilities provide an ideal solution for code or data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the 4-, 8-, and 16-Mbit FlashFile memories offer three levels of protection: absolute protection with V<sub>PP</sub> at GND, selective hardware block locking, or flexible software block locking. These alternatives give designers ultimate control of their code security needs.

This family of products is manufactured on Intel's 0.4 µm ETOX™ V process technology. They come in industry-standard packages: the 40-lead TSOP, ideal for board-constrained applications, and the rugged 44-lead PSOP. Based on the 28F008SA architecture, the byte-wide Smart 5 FlashFile memory family enables quick and easy upgrades for designs that demand state-of-the-art technology.

# SMART 2 Flash<sup>®</sup> MEMORY FAMILY 4, 8, AND 16 MBIT

## FEATURES AND BENEFITS

• High-Density 4-, 8-, and 16-Mbit Symmetrical	• Smart 2 Flash 2V and 3V or
• 4-Mbit, 8-Mbit, 16-Mbit	• 12V V <sub>CC</sub>
• 128Kb, 256Kb, 512Kb	• High-Performance
• 128Kb, 256Kb, 512Kb	• 4.0 Mbit: 55 ns Read Access Time
• 128Kb, 256Kb, 512Kb	• 70 Mbit: 55 ns Read Access Time
• Extended Operating Capability	• Enhanced Data Protection Features
• 100,000 Block Erase Cycles	• Absolute Protection with V <sub>CC</sub> = GND
• Low Power Management	• Flexible Block Locking
• Deep Power-Down Mode	• Block Write Lockout During Power
• Automatic Power Savings Mode	• Transitions
• Burn-In Test in Standby Mode	• Enhanced Automatic Erase/Program Options
• Automatic Program and Block Erase	• Program Suspend to Read
• Command Lock Interface	• Block Erase Suspend to Program
• Status Register	• Block Erase Suspend to Read
• Smart-Compare Write Interface	• Industry-Standard Packaging
• 28CM <sup>2</sup> V Nonvolatile Flash	• 28-Lead THOP, 44-Lead PQFP
• Technology	

Intel's Smart 2 Flash<sup>®</sup> memory family contains a variety of density offerings in the Smart 2 Flash<sup>®</sup> 4-, 8-, and 16-Mbit Symmetrical Flash<sup>®</sup> memory family. Low-cost, nonvolatile memory solutions for a wide range of applications. The symmetrical Flash<sup>®</sup> architecture, which provides high-speed programming and read access, is available in a variety of package types.

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# REVISION HISTORY

Number	Description
-001	Original version
-002	Table 3 revised to reflect change in abbreviations from "W" for write to "P" for program. Ordering information graphic (Appendix A) corrected: from PB = Ext. Temp. 44-Lead PSOP to TB = Ext. Temp. 44-Lead PSOP Updated Ordering Information and table Correction to table, Section 6.2.3. Under I <sub>LO</sub> Test Conditions, previously read V <sub>IN</sub> = V <sub>CC</sub> or GND, corrected to V <sub>OUT</sub> = V <sub>CC</sub> or GND Section 6.2.7, modified Program and Block Erase Suspend Latency Times
-003	Updated disclaimer

## 1.0 INTRODUCTION

This datasheet contains 4-, 8-, and 16-Mbit Smart 5 FlashFile memory specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4, and 5 describe the memory organization and functionality. Section 6 covers electrical specifications for commercial and extended temperature product offerings. The byte-wide Smart 5 FlashFile memory family documentation also includes application notes and design tools which are referenced in Appendix B.

## 1.1 New Features

The byte-wide Smart 5 FlashFile memory family maintains backwards-compatibility with Intel's 28F008SA. Key enhancements include:

- SmartVoltage Technology
- Enhanced Suspend Capabilities
- In-System Block Locking

They share a compatible status register, software commands, and pinouts. These similarities enable a clean upgrade from the 28F008SA to byte-wide Smart 5 FlashFile products. When upgrading, it is important to note the following differences:

- Because of new feature and density options, the devices have different device identifier codes. This allows for software optimization.
- $V_{PPLK}$  has been lowered from 6.5V to 1.5V to support low  $V_{PP}$  voltages during block erase, program, and lock-bit configuration operations. Designs that switch  $V_{PP}$  off during read operations should transition  $V_{PP}$  to GND.
- To take advantage of SmartVoltage technology, allow  $V_{PP}$  connection to 5V.

For more details see application note *AP-625, 28F008SC Compatibility with 28F008SA* (order number 292180).

## 1.2 Product Overview

The byte-wide Smart 5 FlashFile memory family provides density upgrades with pinout compatibility for the 4-, 8-, and 16-Mbit densities. The 28F004S5, 28F008S5, and 28F016S5 are high-performance memories arranged as 512 Kbyte, 1 Mbyte, and 2 Mbyte of 8 bits. This data is grouped in eight, sixteen, and thirty-two 64-Kbyte blocks which are individually erasable, lockable, and unlockable in-system. Figure 4 illustrates the memory organization.

SmartVoltage technology enables fast factory programming and low power designs. Specifically designed for 5V systems, Smart 5 FlashFile components support read operations at 5V  $V_{CC}$  and block erase and program operations at 5V and 12V  $V_{PP}$ . The 12V  $V_{PP}$  option renders the fastest program performance which will increase your factory throughput. With the 5V  $V_{PP}$  option,  $V_{CC}$  and  $V_{PP}$  can be tied together for a simple 5V design. In addition to the voltage flexibility, the dedicated  $V_{PP}$  pin gives complete data protection when  $V_{PP} \leq V_{PPLK}$ .

Internal  $V_{PP}$  detection circuitry automatically configures the device for optimized block erase and program operations.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, program, and lock-bit configuration operations.

A block erase operation erases one of the device's 64-Kbyte blocks typically within 1 second (12V  $V_{PP}$ ), independent of other blocks. Each block can be independently erased 100,000 times (1.6 million block erases per device). A block erase suspend operation allows system software to suspend block erase to read data from or program data to any other block.

Data is programmed in byte increments typically within 6  $\mu$ s (12V  $V_{PP}$ ). A program suspend operation permits system software to read data or execute code from any other flash memory array location.



To protect programmed data, each block can be locked. This block locking mechanism uses a combination of bits, block lock-bits and a master lock-bit, to lock and unlock individual blocks. The block lock-bits gate block erase and program operations, while the master lock-bit gates block lock-bit configuration operations. Lock-bit configuration operations (Set Block Lock-Bit, Set Master Lock-Bit, and Clear Block Lock-Bits commands) set and clear lock-bits.

The status register and RY/BY# output indicate whether or not the device is busy executing or ready for a new command. Polling the status register, system software retrieves WSM feedback. The RY/BY# output gives an additional indicator of WSM activity by providing a hardware status signal. Like the status register, RY/BY#-low indicates that the WSM is performing a block erase, program, or lock-bit configuration. RY/BY#-high indicates that the WSM is ready for a new command, block erase is suspended (and program is inactive), program is suspended, or the device is in deep power-down mode.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical  $I_{CCR}$  current is 1 mA.

When CE# and RP# pins are at  $V_{CC}$ , the component enters a CMOS standby mode. Driving RP# to GND enables a deep power-down mode which significantly reduces power consumption, provides write protection, resets the device, and clears the status register. A reset time ( $t_{PHQV}$ ) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time ( $t_{PHEL}$ ) from RP#-high until writes to the CUI are recognized.

### 1.3 Pinout and Pin Description

The family of devices is available in 40-lead TSOP (Thin Small Outline Package, 1.2 mm thick) and 44-lead PSOP (Plastic Small Outline Package). Pinouts are shown in Figures 2 and 3.

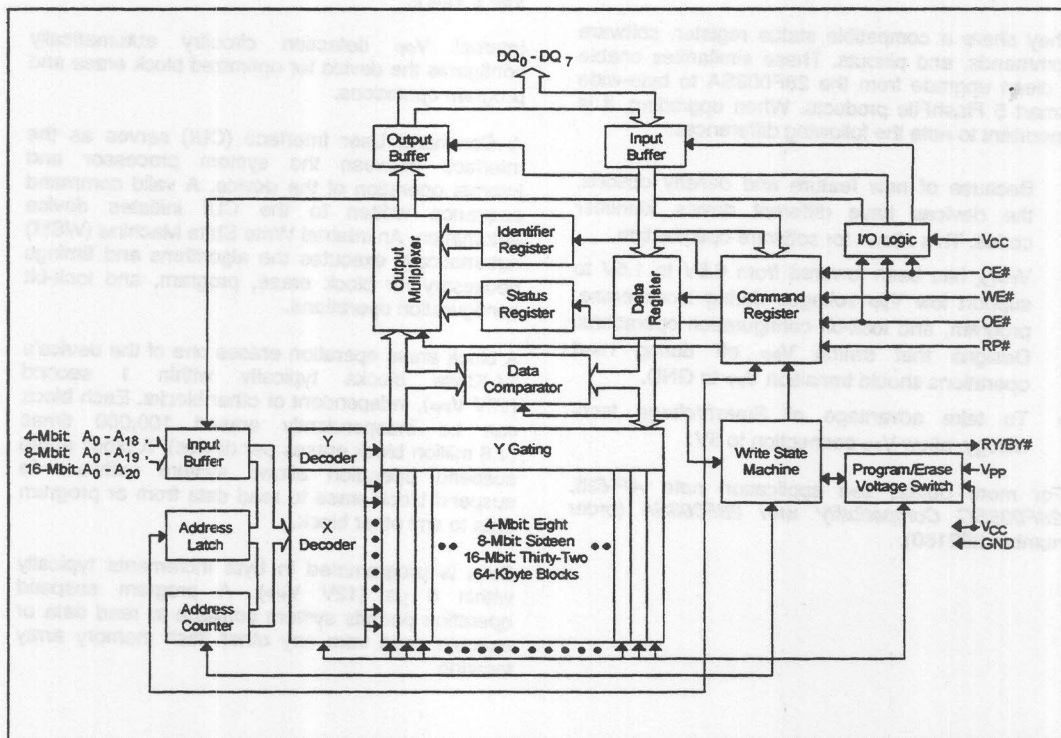


Figure 1. Block Diagram

**Table 1. Pin Descriptions**

Sym	Type	Name and Function
A <sub>0</sub> –A <sub>20</sub>	INPUT	<b>ADDRESS INPUTS:</b> Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle.  4 Mbit → A <sub>0</sub> –A <sub>18</sub> 8 Mbit → A <sub>0</sub> –A <sub>19</sub> 16 Mbit → A <sub>0</sub> –A <sub>20</sub>
DQ <sub>0</sub> –DQ <sub>7</sub>	INPUT/ OUTPUT	<b>DATA INPUT/OUTPUTS:</b> Inputs data and commands during CUI write cycles; outputs data during memory array, status register, and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle.
CE#	INPUT	<b>CHIP ENABLE:</b> Activates the device's control logic, input buffers, decoders, and sense amplifiers. CE#-high deselects the device and reduces power consumption to standby levels.
RP#	INPUT	<b>RESET/DEEP POWER-DOWN:</b> When driven low, RP# inhibits write operations which provides data protection during power transitions, puts the device in deep power-down mode, and resets internal automation. RP#-high enables normal operation. Exit from deep power-down sets the device to read array mode.  RP# at V <sub>HH</sub> enables setting of the master lock-bit and enables configuration of block lock-bits when the master lock-bit is set. RP# = V <sub>HH</sub> overrides block lock-bits, thereby enabling block erase and program operations to locked memory blocks. Block erase, program, or lock-bit configuration with V <sub>IH</sub> < RP# < V <sub>HH</sub> produce spurious results and should not be attempted.
OE#	INPUT	<b>OUTPUT ENABLE:</b> Gates the device's outputs during a read cycle.
WE#	INPUT	<b>WRITE ENABLE:</b> Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
RY/BY#	OUTPUT	<b>READY/BUSY#:</b> Indicates the status of the internal WSM. When low, the WSM is performing an internal operation (block erase, program, or lock-bit configuration). RY/BY#-high indicates that the WSM is ready for new commands, block erase or program is suspended, or the device is in deep power-down mode. RY/BY# is always active.
V <sub>PP</sub>	SUPPLY	<b>BLOCK ERASE, PROGRAM, LOCK-BIT CONFIGURATION POWER SUPPLY:</b> For erasing array blocks, programming data, or configuring lock-bits.  Smart 5 Flash → 5V and 12V V <sub>PP</sub>  With V <sub>PP</sub> ≤ V <sub>PPLK</sub> , memory contents cannot be altered. Block erase, program, and lock-bit configuration with an invalid V <sub>PP</sub> (see DC Characteristics) produce spurious results and should not be attempted.
V <sub>CC</sub>	SUPPLY	<b>DEVICE POWER SUPPLY:</b> Internal detection automatically configures the device for optimized read performance. Do not float any power pins.  Smart 5 Flash → 5V V <sub>CC</sub>  With V <sub>CC</sub> ≤ V <sub>LKO</sub> , all write attempts to the flash memory are inhibited. Device operations at invalid V <sub>CC</sub> voltages (see DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	<b>GROUND:</b> Do not float any ground pins.
NC		<b>NO CONNECT:</b> Lead is not internally connected; it may be driven or floated.

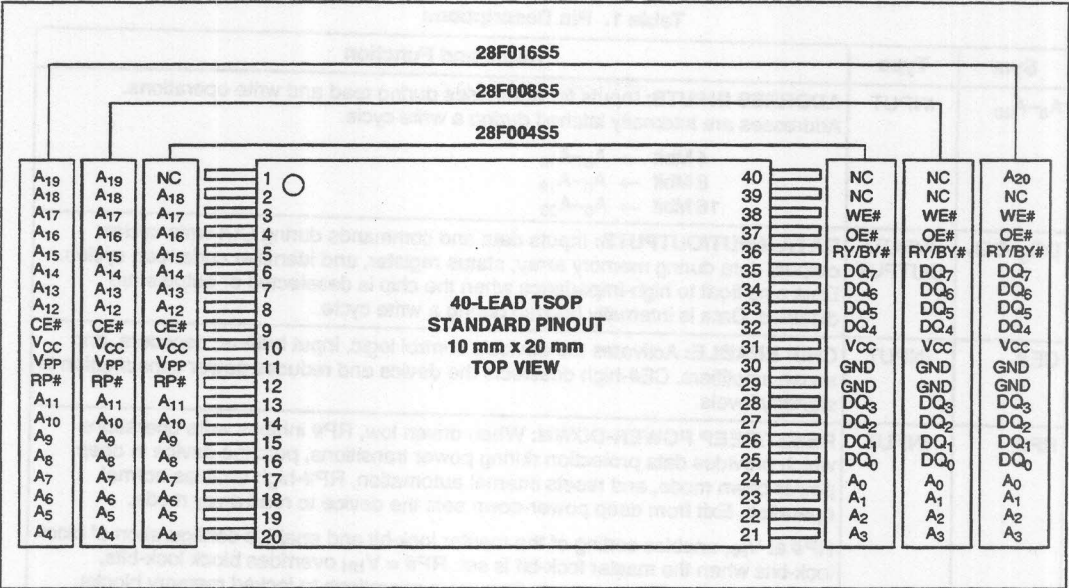


Figure 2. TSOP 40-Lead Pinout

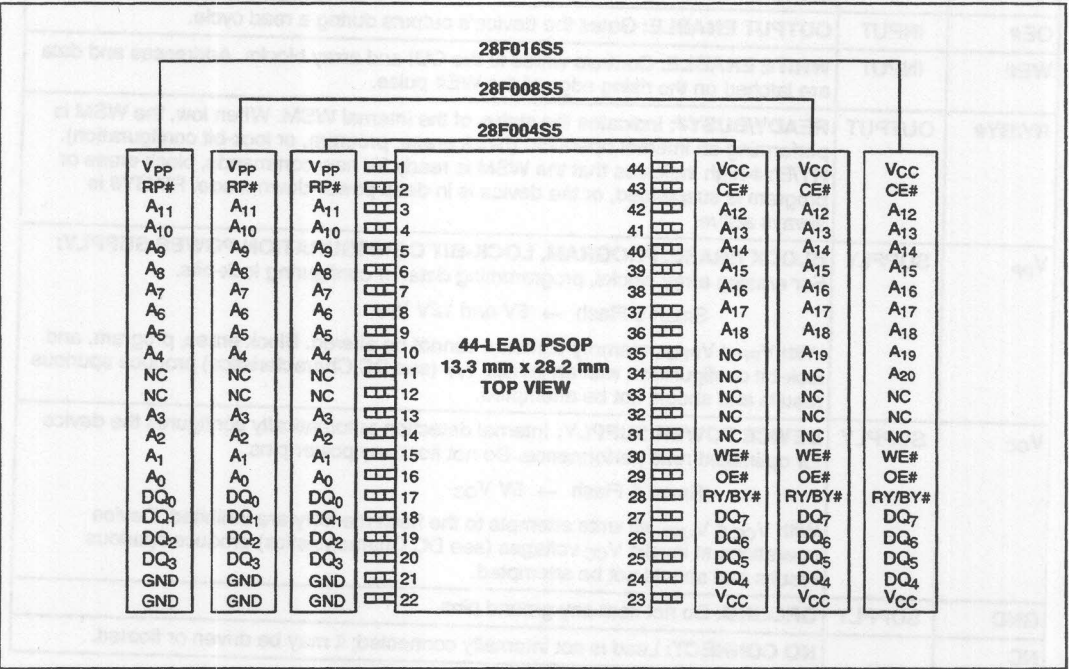


Figure 3. PSOP 44-Lead Pinout



## 2.0 PRINCIPLES OF OPERATION

The byte-wide Smart 5 FlashFile memories include an on-chip WSM to manage block erase, program, and lock-bit configuration functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erasure, program, and lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep power-down mode (see Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the  $V_{PP}$  voltage. High voltage on  $V_{PP}$  enables successful block erasure, program, and lock-bit configuration. All functions associated with altering memory contents—block erase, program, lock-bit configuration, status, and identifier codes—are accessed via the CUI and verified through the status register.

Commands are written using standard micro-processor write timings. The CUI contents serve as input to the WSM that controls block erase, program, and lock-bit configuration operations. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes, or outputs status register data.

Interface software that initiates and polls progress of block erase, program, and lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read data from or program data to any other block. Program suspend allows system software to suspend a program to read data from any other flash memory array location.

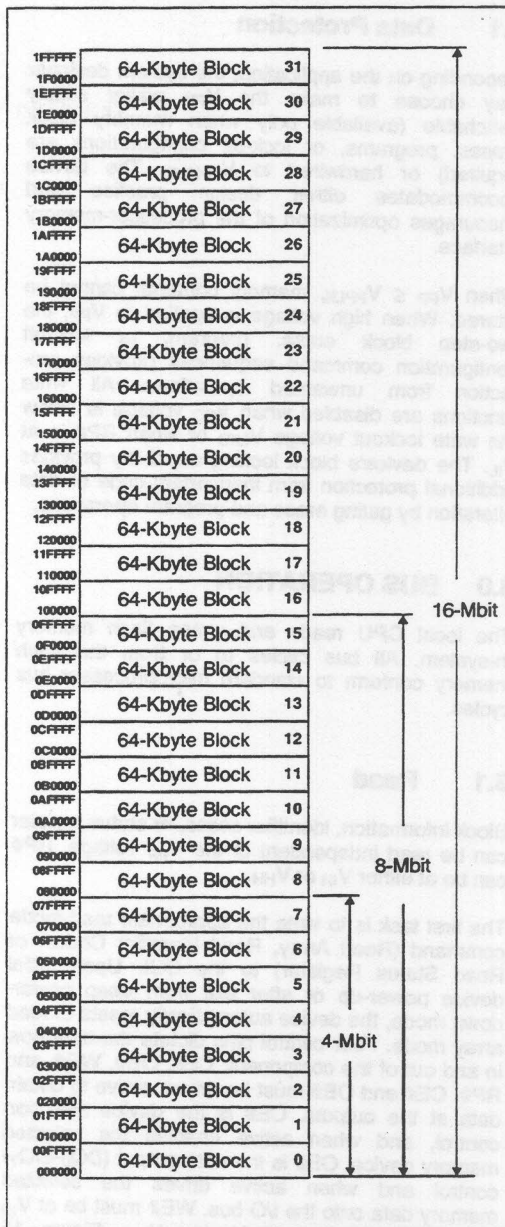


Figure 4. Memory Map

## 2.1 Data Protection

Depending on the application, the system designer may choose to make the  $V_{PP}$  power supply switchable (available only when memory block erases, programs, or lock-bit configurations are required) or hardwired to  $V_{PPH1/2}$ . The device accommodates either design practice and encourages optimization of the processor-memory interface.

When  $V_{PP} \leq V_{PPLK}$ , memory contents cannot be altered. When high voltage is applied to  $V_{PP}$ , the two-step block erase, program, or lock-bit configuration command sequences provides protection from unwanted operations. All write functions are disabled when  $V_{CC}$  voltage is below the write lockout voltage  $V_{LKO}$  or when  $RP\#$  is at  $V_{IL}$ . The device's block locking capability provides additional protection from inadvertent code or data alteration by gating erase and program operations.

## 3.0 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

### 3.1 Read

Block information, identifier codes, or status register can be read independent of the  $V_{PP}$  voltage.  $RP\#$  can be at either  $V_{IH}$  or  $V_{HH}$ .

The first task is to write the appropriate read-mode command (Read Array, Read Identifier Codes, or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Four control pins dictate the data flow in and out of the component:  $CE\#$ ,  $OE\#$ ,  $WE\#$ , and  $RP\#$ .  $CE\#$  and  $OE\#$  must be driven active to obtain data at the outputs.  $CE\#$  is the device selection control, and when active enables the selected memory device.  $OE\#$  is the data output ( $DQ_0$ – $DQ_7$ ) control and when active drives the selected memory data onto the I/O bus.  $WE\#$  must be at  $V_{IH}$  and  $RP\#$  must be at  $V_{IH}$  or  $V_{HH}$ . Figure 15 illustrates a read cycle.

### 3.2 Output Disable

With  $OE\#$  at a logic-high level ( $V_{IH}$ ), the device outputs are disabled. Output pins  $DQ_0$ – $DQ_7$  are placed in a high-impedance state.

### 3.3 Standby

$CE\#$  at a logic-high level ( $V_{IH}$ ) places the device in standby mode which substantially reduces device power consumption.  $DQ_0$ – $DQ_7$  outputs are placed in a high-impedance state independent of  $OE\#$ . If deselected during block erase, program, or lock-bit configuration, the device continues functioning and consuming active power until the operation completes.

### 3.4 Deep Power-Down

$RP\#$  at  $V_{IL}$  initiates the deep power-down mode.

In read mode,  $RP\#$ -low deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits.  $RP\#$  must be held low for time  $t_{PLPH}$ . Time  $t_{PHQV}$  is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI resets to read array mode, and the status register is set to 80H.

During block erase, program, or lock-bit configuration,  $RP\#$ -low will abort the operation.  $RY/BY\#$  remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time  $t_{PHWL}$  is required after  $RP\#$  goes to logic-high ( $V_{IH}$ ) before another command can be written.

As with any automated device, it is important to assert  $RP\#$  during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, program, or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. Intel's flash memories allow proper CPU initialization following a system reset through the use of the  $RP\#$  input. In this application,  $RP\#$  is controlled by the same  $RESET\#$  signal that resets the system CPU.

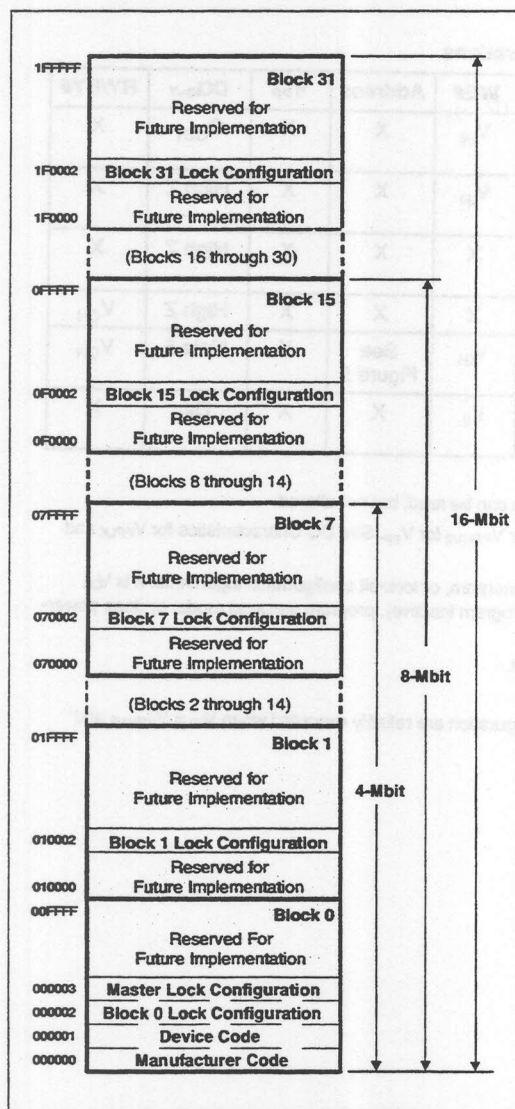


Figure 5. Device Identifier Code Memory Map

### 3.5 Read Identifier Codes Operation

The read identifier codes operation outputs the manufacturer code, device code, block lock configuration codes for each block, and master lock configuration code (see Figure 5). Using the manufacturer and device codes, the system software can automatically match the device with its proper algorithms. The block lock and master lock configuration codes identify locked and unlocked blocks and master lock-bit setting.

### 3.6 Write

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active and OE# = V<sub>IH</sub>. The address and data needed to execute a command are latched on the rising edge of WE# or CE# (whichever goes high first). Standard microprocessor write timings are used. Figure 17 illustrates a write operation.

### 4.0 COMMAND DEFINITIONS

When the V<sub>PP</sub> voltage ≤ V<sub>PPLK</sub>, read operations from the status register, identifier codes, or blocks are enabled. Placing V<sub>PPH1/2</sub> on V<sub>PP</sub> enables successful block erase, program, and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 3 defines these commands.



Table 2. Bus Operations

Mode	Notes	RP#	CE#	OE#	WE#	Address	V <sub>PP</sub>	DQ <sub>0-7</sub>	RY/BY#
Read	1,2,3	V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	X	D <sub>OUT</sub>	X
Output Disable	3	V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X	X	High Z	X
Standby	3	V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IH</sub>	X	X	X	X	High Z	X
Deep Power-Down	4	V <sub>IL</sub>	X	X	X	X	X	High Z	V <sub>OH</sub>
Read Identifier Codes		V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	See Figure 5	X	Note 5	V <sub>OH</sub>
Write	3,6,7	V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	X	X	D <sub>IN</sub>	X

**NOTES:**

1. Refer to DC Characteristics. When  $V_{PP} \leq V_{PPLK}$ , memory contents can be read, but not altered.
2. X can be V<sub>IL</sub> or V<sub>IH</sub> for control and address input pins and V<sub>PPLK</sub> or V<sub>PPH1/2</sub> for V<sub>PP</sub>. See DC Characteristics for V<sub>PPLK</sub> and V<sub>PPH1/2</sub> voltages.
3. RY/BY# is V<sub>OL</sub> when the WSM is executing internal block erase, program, or lock-bit configuration algorithms. It is V<sub>OH</sub> when the WSM is not busy, in block erase suspend mode (with program inactive), program suspend mode, or deep power-down mode.
4. RP# at GND ± 0.2V ensures the lowest deep power-down current.
5. See Section 4.2 for read identifier code data.
6. Command writes involving block erase, program, or lock-bit configuration are reliably executed when  $V_{PP} = V_{PPH1/2}$  and  $V_{CC} = V_{CC1/2}$  (see Section 6.2 for operating conditions).
7. Refer to Table 3 for valid D<sub>IN</sub> during a write operation.

**Table 3. Command Definitions<sup>(9)</sup>**

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper <sup>(1)</sup>	Addr <sup>(2)</sup>	Data <sup>(3)</sup>	Oper <sup>(1)</sup>	Addr <sup>(2)</sup>	Data <sup>(3)</sup>
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥ 2	4	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Program	2	5,6	Write	PA	40H or 10H	Write	PA	PD
Block Erase and Program Suspend	1	5	Write	X	B0H			
Block Erase and Program Resume	1	5	Write	X	D0H			
Set Block Lock-Bit	2	7	Write	BA	60H	Write	BA	01H
Set Master Lock-Bit	2	7	Write	X	60H	Write	X	F1H
Clear Block Lock-Bits	2	8	Write	X	60H	Write	X	D0H

**NOTES:**

1. Bus operations are defined in Table 2.
2. X = Any valid address within the device.  
IA = Identifier Code Address: see Figure 5.  
BA = Address within the block being erased or locked.  
PA = Address of memory location to be programmed.
3. SRD = Data read from status register. See Table 6 for a description of the status register bits.  
PD = Data to be programmed at location PA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).  
ID = Data read from identifier codes.
4. Following the Read Identifier Codes command, read operations access manufacturer, device, block lock, and master lock codes. See Section 4.2 for read identifier code data.
5. If the block is locked, RP# must be at V<sub>HH</sub> to enable block erase or program operations. Attempts to issue a block erase or program to a locked block while RP# is V<sub>HH</sub> will fail.
6. Either 40H or 10H are recognized by the WSM as the program setup.
7. If the master lock-bit is set, RP# must be at V<sub>HH</sub> to set a block lock-bit. RP# must be at V<sub>HH</sub> to set the master lock-bit. If the master lock-bit is not set, a block lock-bit can be set while RP# is V<sub>HH</sub>.
8. If the master lock-bit is set, RP# must be at V<sub>HH</sub> to clear block lock-bits. The clear block lock-bits operation simultaneously clears all block lock-bits. If the master lock-bit is not set, the Clear Block Lock-Bits command can be done while RP# is V<sub>HH</sub>.
9. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.

#### 4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, program or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Program Suspend command. The Read Array command functions independently of the  $V_{PP}$  voltage and RP# can be  $V_{IH}$  or  $V_{HH}$ .

#### 4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 5 retrieve the manufacturer, device, block lock configuration and master lock configuration codes (see Table 4 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the  $V_{PP}$  voltage and RP# can be  $V_{IH}$  or  $V_{HH}$ . Following the Read Identifier Codes command, the subsequent information can be read.

Table 4. Identifier Codes

Code	Address	Data
Manufacturer Code	000000	89
Device Code	4-Mbit	000001 A7
	8-Mbit	000001 A6
	16-Mbit	000001 AA
Block Lock Configuration	XX0002 <sup>(1)</sup>	
• Block Is Unlocked		DQ <sub>0</sub> = 0
• Block Is Locked		DQ <sub>0</sub> = 1
• Reserved for Future Use		DQ <sub>1-7</sub>
Master Lock Configuration	000003	
• Device Is Unlocked		DQ <sub>0</sub> = 0
• Device Is Locked		DQ <sub>0</sub> = 1
• Reserved for Future Use		DQ <sub>1-7</sub>

**NOTE:**

1. X selects the specific block lock configuration code to be read. See Figure 5 for the device identifier code memory map.

#### 4.3 Read Status Register Command

The status register may be read to determine when a block erase, program, or lock-bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE#, whichever occurs first. OE# or CE# must toggle to  $V_{IH}$  to update the status register latch. The Read Status Register command functions independently of the  $V_{PP}$  voltage. RP# can be  $V_{IH}$  or  $V_{HH}$ .

#### 4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3, and SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 6). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied  $V_{PP}$  voltage. RP# can be  $V_{IH}$  or  $V_{HH}$ . This command is not functional during block erase or program suspend modes.

#### 4.5 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is written first, followed by a block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect block erase completion by analyzing the RY/BY# pin or status register bit SR.7.



When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1." Also, reliable block erasure can only occur when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH1/2}$ . In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while  $V_{PP} \leq V_{PPLK}$ , SR.3 and SR.5 will be set to "1." Successful block erase requires that the corresponding block lock-bit be cleared or, if set, that  $RP\# = V_{HH}$ . If block erase is attempted when the corresponding block lock-bit is set and  $RP\# = V_{IH}$ , the block erase will fail, and SR.1 and SR.5 will be set to "1." Block erase operations with  $V_{IH} < RP\# < V_{HH}$  produce spurious results and should not be attempted.

#### 4.6 Program Command

Program is executed by a two-cycle command sequence. Program setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the program and write verify algorithms internally. After the program sequence is written, the device automatically outputs status register data when read (see Figure 7). The CPU can detect the completion of the program event by analyzing the RY/BY# pin or status register bit SR.7.

When program is complete, status register bit SR.4 should be checked. If program error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully program to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable programs only occurs when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH1/2}$ . In the absence of this high voltage, memory contents are protected against programs. If program is attempted while  $V_{PP} \leq V_{PPLK}$ , the operation will fail, and status register bits SR.3 and SR.5 will be set to "1."

Successful program also requires that the corresponding block lock-bit be cleared or, if set, that  $RP\# = V_{HH}$ . If program is attempted when the corresponding block lock-bit is set and  $RP\# = V_{IH}$ , program will fail, and SR.1 and SR.4 will be set to "1." Program operations with  $V_{IH} < RP\# < V_{HH}$  produce spurious results and should not be attempted.

#### 4.7 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read data from or program data to another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). RY/BY# will also transition to  $V_{OH}$ . Specification  $t_{WHRH2}$  defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Program command sequence can also be issued during erase suspend to program data in other blocks. Using the Program Suspend command (see Section 4.8), a program operation can also be suspended. During a program operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/BY# output will transition to  $V_{OL}$ . However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/BY# will return to  $V_{OL}$ . After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 8).  $V_{PP}$  must remain at  $V_{PPH1/2}$  (the same  $V_{PP}$  level used for block erase) while block erase is suspended.  $RP\#$  must also remain at  $V_{IH}$  or  $V_{HH}$  (the same  $RP\#$  level used for block erase). Block erase cannot resume until program operations initiated during block erase suspend have completed.

#### 4.8 Program Suspend Command

The Program Suspend command allows program interruption to read data in other flash memory locations. Once the program process starts, writing the Program Suspend command requests that the WSM suspend the program sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Program Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the program operation has been suspended (both will be set to "1"). RY/BY# will also transition to  $V_{OH}$ . Specification  $t_{WHRH1}$  defines the program suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while program is suspended are Read Status Register and Program Resume. After Program Resume command is written to the flash memory, the WSM will continue the program process. Status register bits SR.2 and SR.7 will automatically clear and RY/BY# will return to  $V_{OL}$ . After the Program Resume command is written, the device automatically outputs status register data when read (see Figure 9).  $V_{PP}$  must remain at  $V_{PPH1/2}$  (the same  $V_{PP}$  level used for program) while in program suspend mode. RP# must also remain at  $V_{IH}$  or  $V_{HH}$  (the same RP# level used for program).

#### 4.9 Set Block and Master Lock-Bit Commands

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits and a master lock-bit. The block lock-bits gate program and erase operations while the master lock-bit gates block-lock bit modification. With the master lock-bit not set, individual block lock-bits can be set using the Set Block Lock-Bit command. The Set Master Lock-Bit command, in conjunction with RP# =  $V_{HH}$ , sets the master lock-bit. After the

master lock-bit is set, subsequent setting of block lock-bits requires both the Set Block Lock-Bit command and  $V_{HH}$  on the RP# pin. See Table 5 for a summary of hardware and software write protection options.

Set block lock-bit and master lock-bit are initiated using two-cycle command sequence. The set block or master lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked) or the set master lock-bit confirm (and any device address). The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 10). The CPU can detect the completion of the set lock-bit event by analyzing the RY/BY# pin output or status register bit SR.7.

When the set lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of setup followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block or Master Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1." Also, reliable operations occur only when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH1/2}$ . In the absence of this high voltage, lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires that the master lock-bit be cleared or, if the master lock-bit is set, that RP# =  $V_{HH}$ . If it is attempted with the master lock-bit set and RP# =  $V_{IH}$ , the operation will fail, and SR.1 and SR.4 will be set to "1." A successful set master lock-bit operation requires that RP# =  $V_{HH}$ . If it is attempted with RP# =  $V_{IH}$ , the operation will fail, and SR.1 and SR.4 will be set to "1." Set block and master lock-bit operations with  $V_{IH} < RP\# < V_{HH}$  produce spurious results and should not be attempted.

#### 4.10 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With the master lock-bit not set, block lock-bits can be cleared using only the Clear Block Lock-Bits command. If the master lock-bit is set, clearing block lock-bits requires both the Clear Block Lock-Bits command and  $V_{HH}$  on the RP# pin. See Table 5 for a summary of hardware and software write protection options.

Clear block lock-bits operation is initiated using a two-cycle command sequence. A clear block lock-bits setup is written first. Then, the device automatically outputs status register data when read (see Figure 11). The CPU can detect completion of the clear block lock-bits event by analyzing the RY/BY# pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1." Also, a reliable clear block lock-bits operation can only occur when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH1/2}$ . If a clear block lock-bits operation is attempted while  $V_{PP} \leq V_{PPLK}$ , SR.3 and SR.5 will be set to "1." In the absence of this high voltage, the block lock-bits content are protected against alteration. A successful clear block lock-bits operation requires that the master lock-bit is not set or, if the master lock-bit is set, that  $RP\# = V_{HH}$ . If it is attempted with the master lock-bit set and  $RP\# = V_{IH}$ , SR.1 and SR.5 will be set to "1" and the operation will fail. A clear block lock-bits operation with  $V_{IH} < RP\# < V_{HH}$  produce spurious results and should not be attempted.

If a clear block lock-bits operation is aborted due to  $V_{PP}$  or  $V_{CC}$  transitioning out of valid range or  $RP\#$  active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values. Once the master lock-bit is set, it cannot be cleared.

**Table 5. Write Protection Alternatives**

Operation	Master Lock-Bit	Block Lock-Bit	RP#	Effect
Block Erase or Program	X	0	$V_{IH}$ or $V_{HH}$	Block Erase and Program Enabled
		1	$V_{IH}$	Block is Locked. Block Erase and Program Disabled
			$V_{HH}$	Block Lock-Bit Override. Block Erase and Program Enabled
Set Block Lock-Bit	0	X	$V_{IH}$ or $V_{HH}$	Set Block Lock-Bit Enabled
	1	X	$V_{IH}$	Master Lock-Bit is Set. Set Block Lock-Bit Disabled
			$V_{HH}$	Master Lock-Bit Override. Set Block Lock-Bit Enabled
Set Master Lock-Bit	X	X	$V_{IH}$	Set Master Lock-Bit Disabled
			$V_{HH}$	Set Master Lock-Bit Enabled
Clear Block Lock-Bits	0	X	$V_{IH}$ or $V_{HH}$	Clear Block Lock-Bits Enabled
	1	X	$V_{IH}$	Master Lock-Bit is Set. Clear Block Lock-Bits Disabled
			$V_{HH}$	Master Lock-Bit Override. Clear Block Lock-Bits Enabled



Table 6. Status Register Definition

WSMS	ESS	ECLBS	PSLBS	VPPS	PSS	DPS	R
7	6	5	4	3	2	1	0

<p>SR.7 = WRITE STATE MACHINE STATUS  1 = Ready  0 = Busy</p> <p>SR.6 = ERASE SUSPEND STATUS  1 = Block Erase Suspended  0 = Block Erase in Progress/Completed</p> <p>SR.5 = ERASE AND CLEAR LOCK-BITS STATUS  1 = Error in Block Erasure or Clear Lock-Bits  0 = Successful Block Erase or Clear Lock-Bits</p> <p>SR.4 = PROGRAM AND SET LOCK-BIT STATUS  1 = Error in Program or Set Master/Block Lock-Bit  0 = Successful Program or Set Master/Block Lock-Bit</p> <p>SR.3 = V<sub>PP</sub> STATUS  1 = V<sub>PP</sub> Low Detect, Operation Abort  0 = V<sub>PP</sub> OK</p> <p>SR.2 = PROGRAM SUSPEND STATUS  1 = Program Suspended  0 = Program in Progress/Completed</p> <p>SR.1 = DEVICE PROTECT STATUS  1 = Master Lock-Bit, Block Lock-Bit and/or RP# Lock Detected, Operation Abort  0 = Unlock</p> <p>SR.0 = RESERVED FOR FUTURE ENHANCEMENTS</p>	<p><b>NOTES:</b></p> <p>Check RY/BY# or SR.7 to determine block erase, program, or lock-bit configuration completion. SR.6–0 are invalid while SR.7 = “0.”</p> <p>If both SR.5 and SR.4 are “1”s after a block erase or lock-bit configuration attempt, an improper command sequence was entered.</p> <p>SR.3 does not provide a continuous indication of V<sub>PP</sub> level. The WSM interrogates and indicates the V<sub>PP</sub> level only after a block erase, program, or lock-bit configuration operation. SR.3 is not guaranteed to reports accurate feedback only when V<sub>PP</sub> ≠ V<sub>PPH1/2</sub>.</p> <p>SR.1 does not provide a continuous indication of master and block lock-bit values. The WSM interrogates the master lock-bit, block lock-bit, and RP# only after a block erase, program, or lock-bit configuration operation. It informs the system, depending on the attempted operation, if the block lock-bit is set, master lock-bit is set, and/or RP# ≠ V<sub>HH</sub>.</p> <p>SR.0 is reserved for future use and should be masked out when polling the status register.</p>
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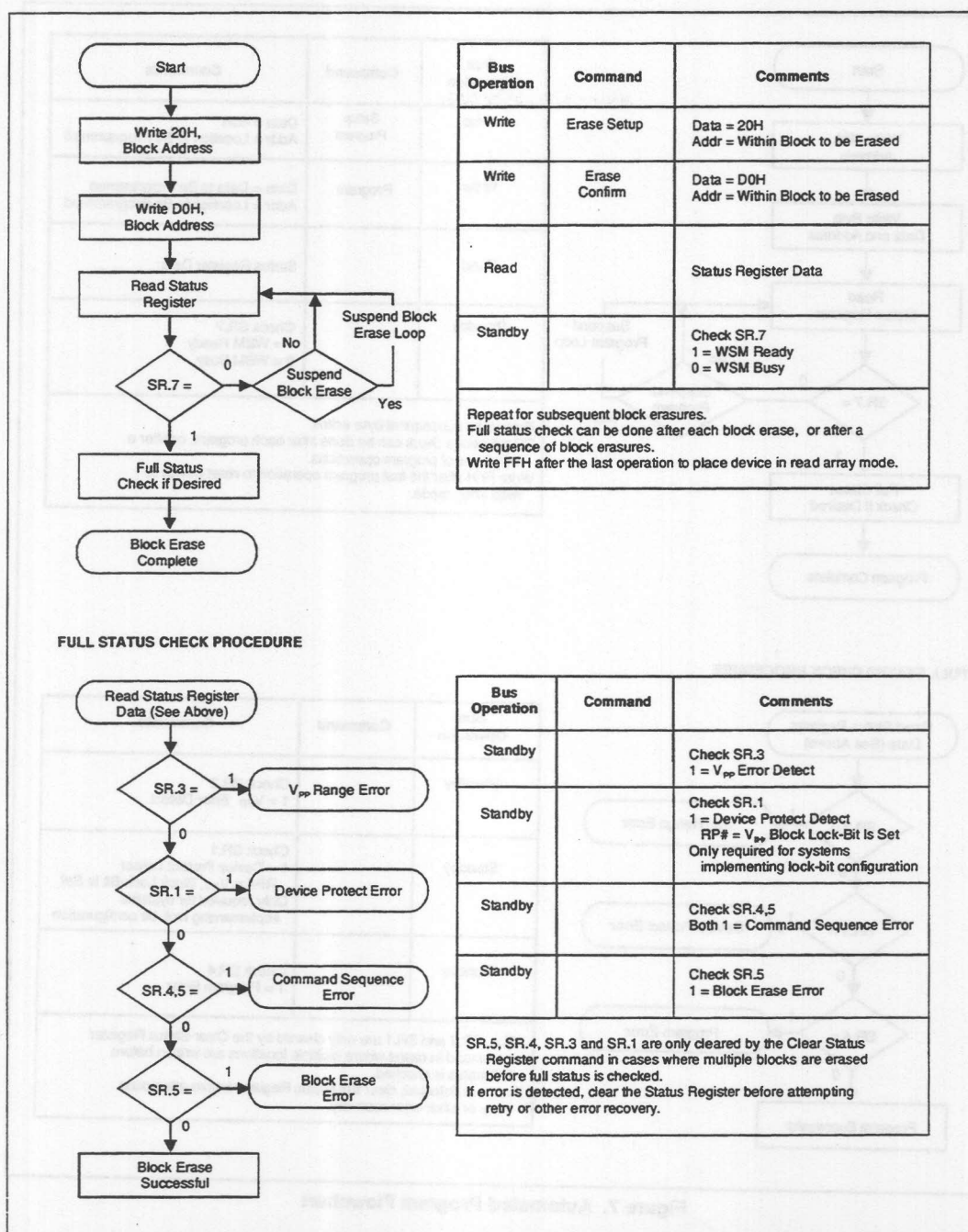
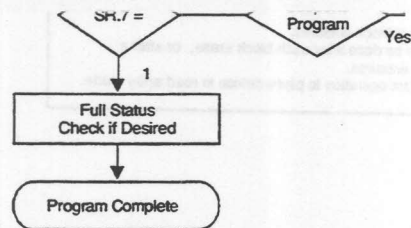
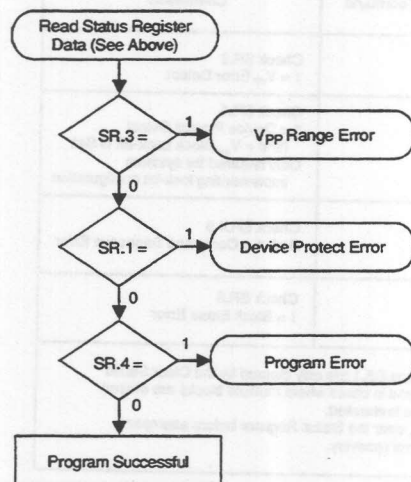


Figure 6. Automated Block Erase Flowchart



Repeat for subsequent byte writes.  
 SR full status check can be done after each program, or after a sequence of program operations.  
 Write FFH after the last program operation to reset device to read array mode.

#### FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V <sub>pp</sub> Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = V <sub>IH</sub> , Block Lock-Bit Is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4 1 = Program Error

SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.  
 If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 7. Automated Program Flowchart



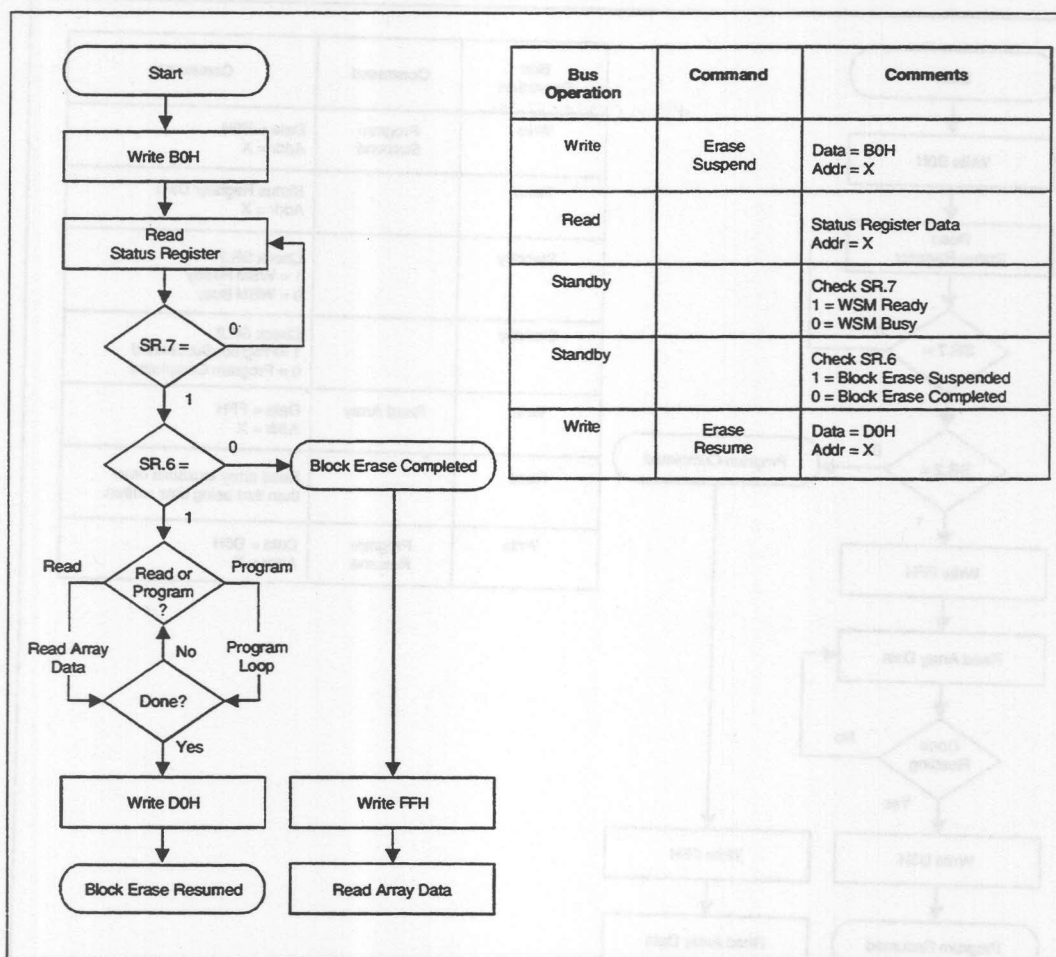


Figure 8. Block Erase Suspend/Resume Flowchart

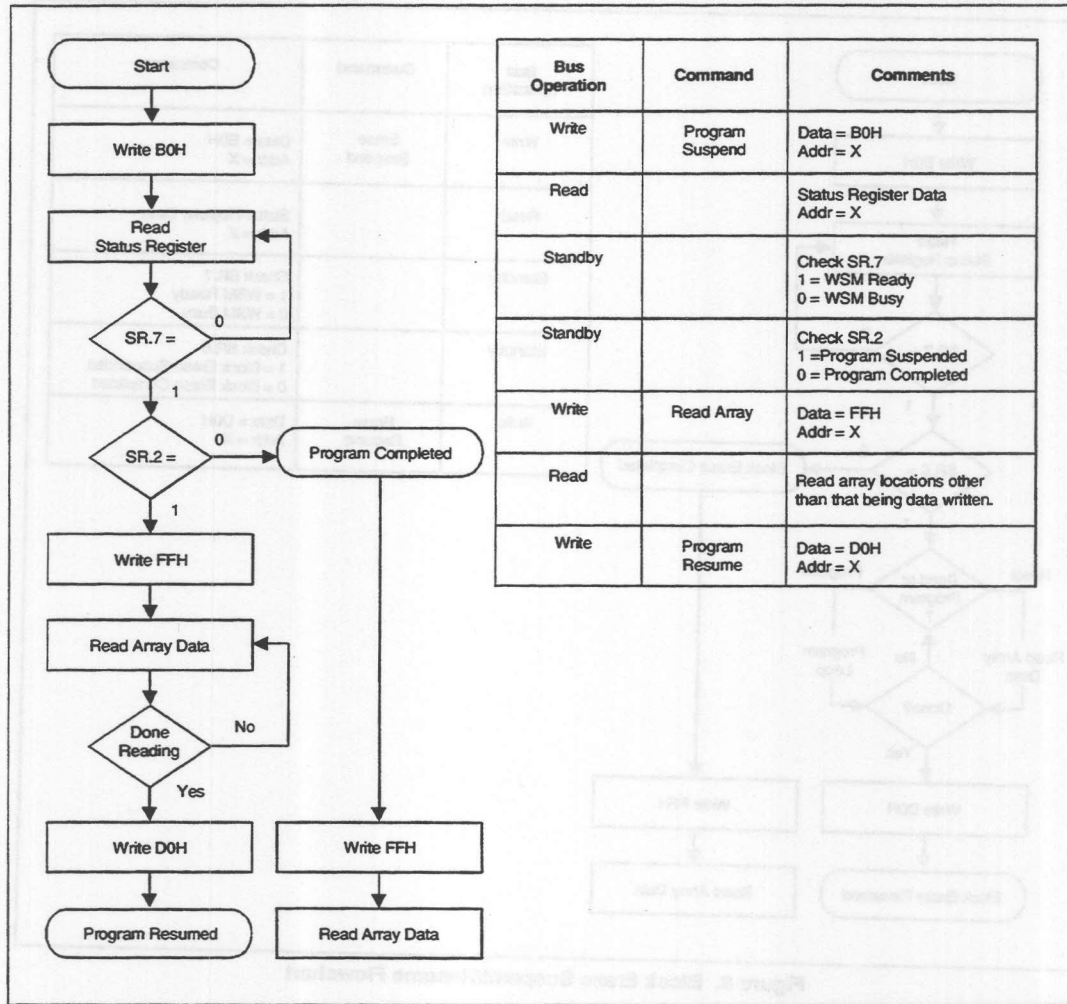


Figure 9. Program Suspend/Resume Flowchart

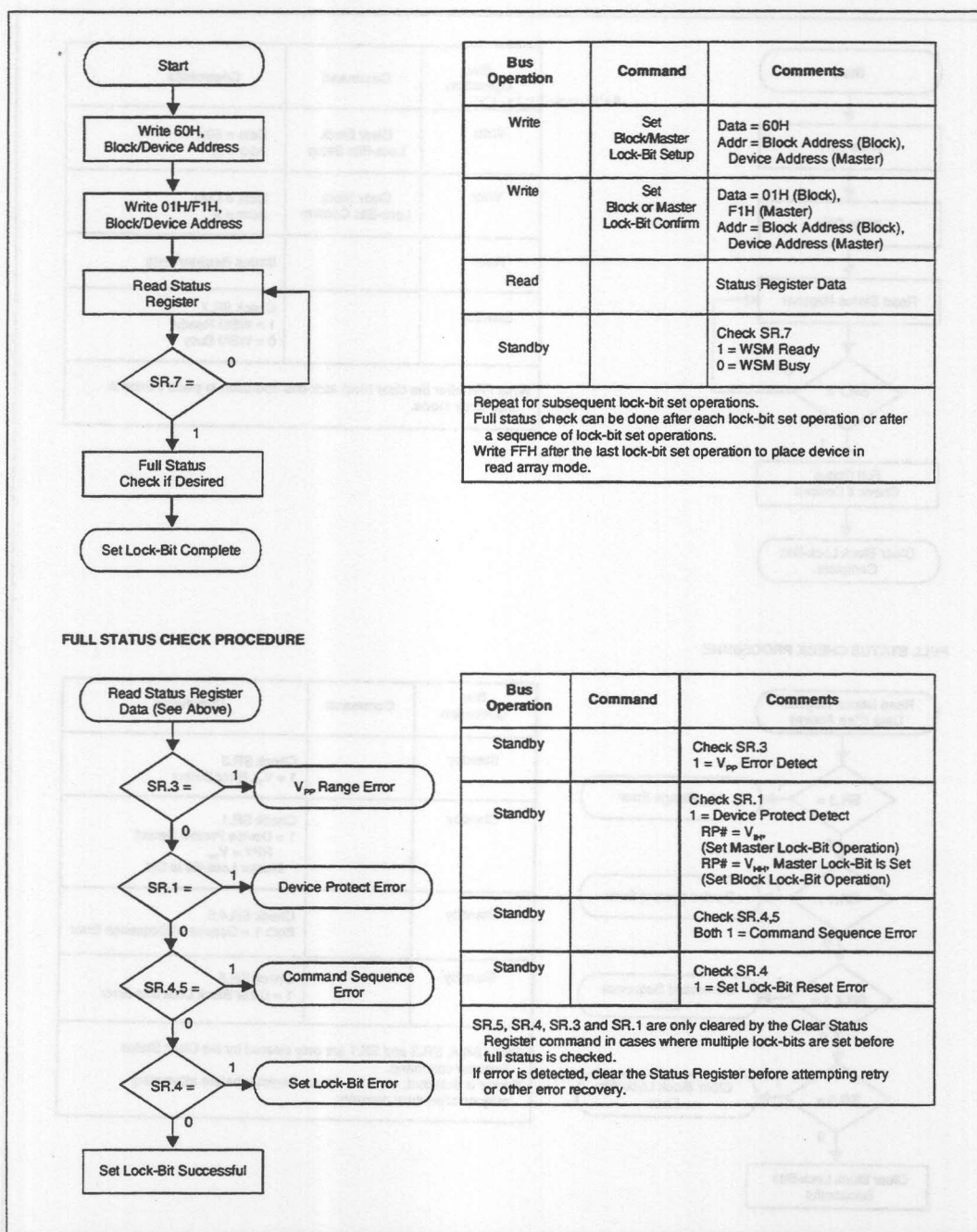


Figure 10. Set Block and Master Lock-Bit Flowchart



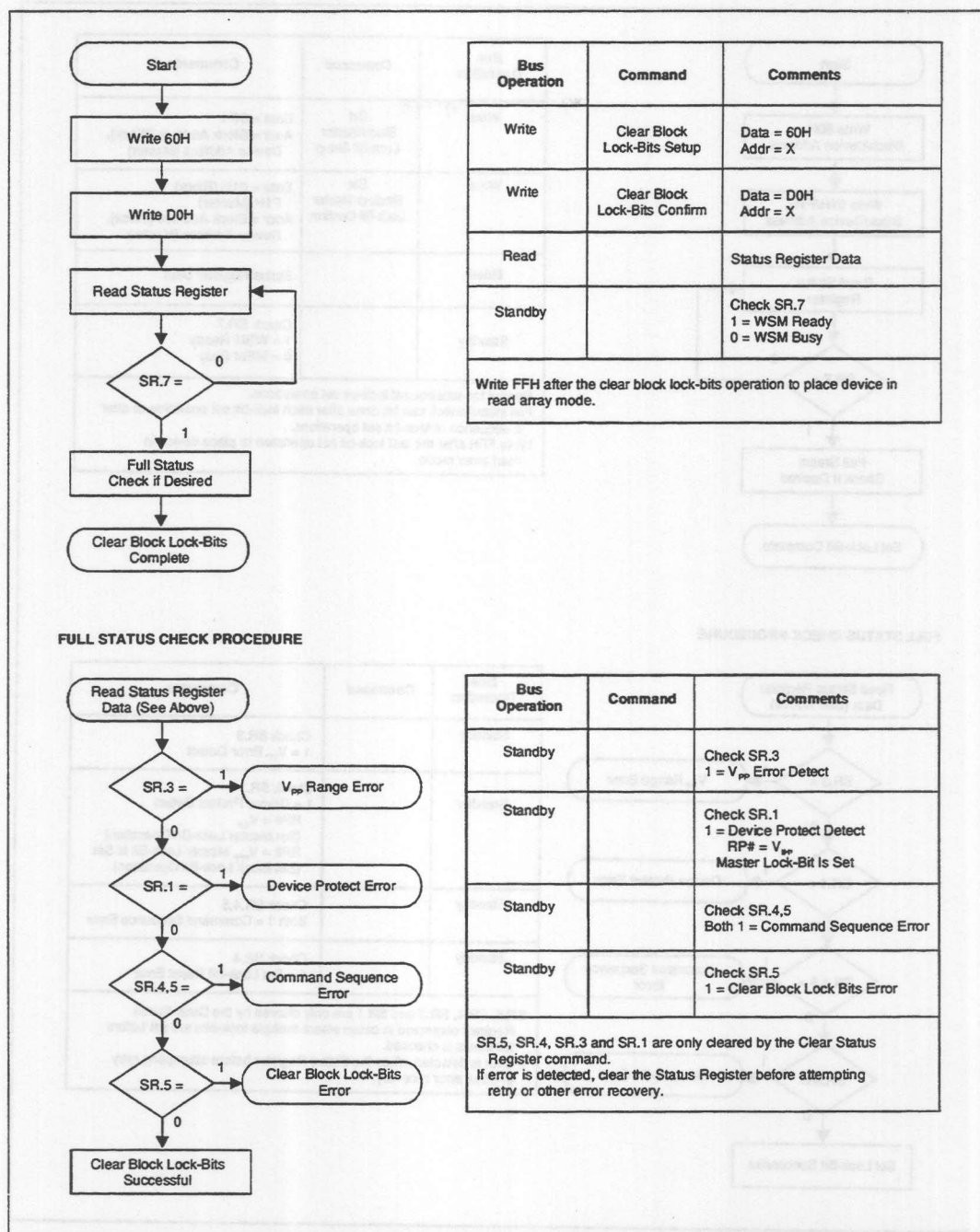


Figure 11. Clear Block Lock-Bits Flowchart

## 5.0 DESIGN CONSIDERATIONS

### 5.1 Three-Line Output Control

Intel provides three control inputs to accommodate multiple memory connections: CE#, OE#, and RP#. Three-line control provides for:

- Lowest possible memory power dissipation.
- Data bus contention avoidance.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

### 5.2 RY/BY# Hardware Detection

RY/BY# is a full CMOS output that provides a hardware method of detecting block erase, program and lock-bit configuration completion. This output can be directly connected to an interrupt input of the system CPU. RY/BY# transitions low when the WSM is busy and returns to  $V_{OH}$  when it is finished executing the internal algorithm. During suspend and deep power-down modes, RY/BY# remains at  $V_{OH}$ .

### 5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues: standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1  $\mu F$  ceramic capacitor connected between its  $V_{CC}$  and GND and between its  $V_{PP}$  and GND. These high-frequency, low-inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7  $\mu F$  electrolytic capacitor should be placed at the array's power supply connection between  $V_{CC}$  and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

### 5.4 $V_{PP}$ Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the  $V_{PP}$  power supply trace. The  $V_{PP}$  pin supplies the memory cell current for byte writing and block erasing. Use similar trace widths and layout considerations given to the  $V_{CC}$  power bus. Adequate  $V_{PP}$  supply traces and decoupling will decrease  $V_{PP}$  voltage spikes and overshoots.

### 5.5 $V_{CC}$ , $V_{PP}$ , RP# Transitions

Block erase, program and lock-bit configuration are not guaranteed if  $V_{PP}$  or  $V_{CC}$  fall outside of a valid voltage range ( $V_{CC1/2}$  and  $V_{PPH1/2}$ ) or  $RP\# \neq V_{IH}$  or  $V_{HH}$ . If  $V_{PP}$  error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If RP# transitions to  $V_{IL}$  during block erase, program, or lock-bit configuration, RY/BY# will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored.

### 5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block erasure, byte writing, or lock-bit configuration during power transitions. Upon power-up, the device is indifferent as to which power supply ( $V_{PP}$  or  $V_{CC}$ ) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for  $V_{CC}$  voltages above  $V_{LKO}$  when  $V_{PP}$  is active. Since both WE# and CE# must be low for a command write, driving either input signal to  $V_{IH}$  will inhibit writes. The CUI's two-step command sequence architecture provides an added level of protection against data alteration.

In-system block lock and unlock renders additional protection during power-up by prohibiting block erase and program operations. The device is disabled while  $RP\# = V_{IL}$  regardless of its control inputs state.

## PRODUCT PREVIEW

## 6.0 ELECTRICAL SPECIFICATIONS

### 6.1 Absolute Maximum Ratings\*

Temperature under Bias .....	-10°C to +80°C
Storage Temperature.....	-65°C to +125°C
Voltage On Any Pin (except V <sub>PP</sub> and RP#).....	-2.0V to +7.0V <sup>(2)</sup>
V <sub>PP</sub> Voltage .....	-2.0V to +14.0V <sup>(1,2)</sup>
RP# Voltage .....	-2.0V to +14.0V <sup>(1,2,4)</sup>
Output Short Circuit Current .....	100 mA <sup>(3)</sup>

#### NOTES:

1. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V<sub>CC</sub>, RP#, and V<sub>PP</sub> pins. During transitions, this level may undershoot to -2.0V for periods <20 ns. Maximum DC voltage on input/output pins and V<sub>CC</sub> is V<sub>CC</sub> +0.5V which, during transitions, may overshoot to V<sub>CC</sub> +2.0V for periods <20 ns.
2. Maximum DC voltage on V<sub>PP</sub> and RP# may overshoot to +14.0V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. RP# voltage is normally at V<sub>IL</sub> or V<sub>IH</sub>. Connection to supply of V<sub>IH</sub> is allowed for a maximum cumulative period of 80 hours.

NOTICE: This datasheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

*\*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

### 6.2 Commercial Temperature Operating Conditions

Commercial Temperature and V<sub>CC</sub> Operating Conditions

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
T <sub>A</sub>	Operating Temperature		0	+70	°C	Ambient Temperature
V <sub>CC1</sub>	V <sub>CC</sub> Supply Voltage (5V ± 5%)		4.75	5.25	V	
V <sub>CC2</sub>	V <sub>CC</sub> Supply Voltage (5V ± 10%)		4.50	5.50	V	

#### 6.2.1 CAPACITANCE <sup>(1)</sup>

T<sub>A</sub> = +25°C, f = 1 MHz

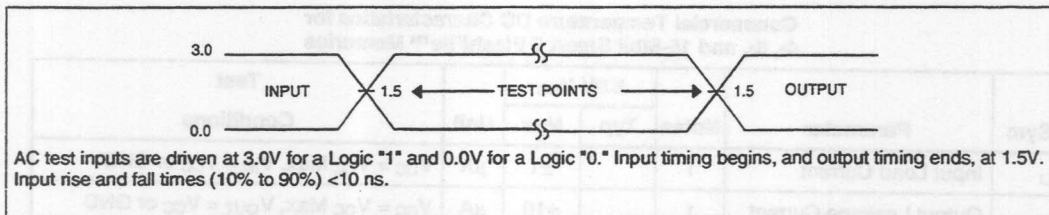
Symbol	Parameter	Typ	Max	Unit	Condition
C <sub>IN</sub>	Input Capacitance	6	8	pF	V <sub>IN</sub> = 0.0V
C <sub>OUT</sub>	Output Capacitance	8	12	pF	V <sub>OUT</sub> = 0.0V

#### NOTE:

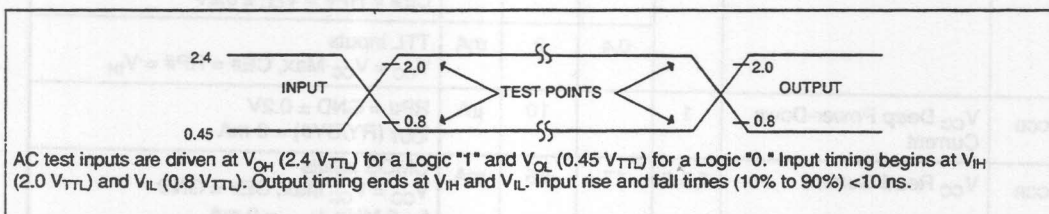
1. Sampled, not 100% tested.



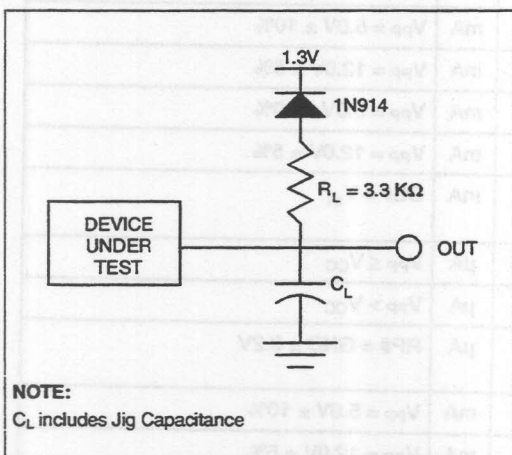
## 6.2.2 AC INPUT/OUTPUT TEST CONDITIONS



**Figure 12. Transient Input/Output Reference Waveform for  $V_{CC} = 5.0V \pm 5\%$  (High Speed Testing Configuration)**



**Figure 13. Transient Input/Output Reference Waveform for  $V_{CC} = 5.0V \pm 10\%$  (Standard Testing Configuration)**



**Figure 14. Transient Equivalent Testing Load Circuit**

## Test Configuration Capacitance Loading Value

Test Configuration	$C_L$ (pF)
$V_{CC} = 5.0V \pm 5\%$	30
$V_{CC} = 5.0V \pm 10\%$	100

6.2.3 COMMERCIAL TEMPERATURE DC CHARACTERISTICS

Commercial Temperature DC Characteristics for  
4-, 8-, and 16-Mbit Smart 5 FlashFile™ Memories

Sym	Parameter	Notes	5.0V V <sub>CC</sub>		Unit	Test Conditions
			Typ	Max		
I <sub>LI</sub>	Input Load Current	1		±1	μA	V <sub>CC</sub> = V <sub>CC</sub> Max, V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>LO</sub>	Output Leakage Current	1		±10	μA	V <sub>CC</sub> = V <sub>CC</sub> Max, V <sub>OUT</sub> = V <sub>CC</sub> or GND
I <sub>CCS</sub>	V <sub>CC</sub> Standby Current	1,3,6	25	100	μA	CMOS Inputs V <sub>CC</sub> = V <sub>CC</sub> Max CE# = RP# = V <sub>CC</sub> ± 0.2V
			0.4	2	mA	TTL Inputs V <sub>CC</sub> = V <sub>CC</sub> Max, CE# = RP# = V <sub>IH</sub>
I <sub>CCD</sub>	V <sub>CC</sub> Deep Power-Down Current	1		10	μA	RP# = GND ± 0.2V I <sub>OUT</sub> (RY/BY#) = 0 mA
I <sub>CCR</sub>	V <sub>CC</sub> Read Current	1,5,6	17	35	mA	CMOS Inputs V <sub>CC</sub> = V <sub>CC</sub> Max, CE# = GND f = 8 MHz, I <sub>OUT</sub> = 0 mA
			20	50	mA	TTL Inputs V <sub>CC</sub> = V <sub>CC</sub> Max, CE# = GND f = 8 MHz, I <sub>OUT</sub> = 0 mA
I <sub>CCW</sub>	V <sub>CC</sub> Program/Set Lock-Bit Current	1,7		35	mA	V <sub>PP</sub> = 5.0V ± 10%
				30	mA	V <sub>PP</sub> = 12.0V ± 5%
I <sub>CCE</sub>	V <sub>CC</sub> Block Erase/Clear Block Lock-Bits Current	1,7		30	mA	V <sub>PP</sub> = 5.0V ± 10%
				25	mA	V <sub>PP</sub> = 12.0V ± 5%
I <sub>CCWS</sub> I <sub>CCES</sub>	V <sub>CC</sub> Program/Block Erase Suspend Current	1,2	1	10	mA	CE# = V <sub>IH</sub>
I <sub>PPS</sub>	V <sub>PP</sub> Standby Current	1	± 2	± 15	μA	V <sub>PP</sub> ≤ V <sub>CC</sub>
I <sub>PPR</sub>	V <sub>PP</sub> Read Current	1	10	200	μA	V <sub>PP</sub> > V <sub>CC</sub>
I <sub>PPD</sub>	V <sub>PP</sub> Deep Power-Down Current	1	0.1	5	μA	RP# = GND ± 0.2V
I <sub>PPW</sub>	V <sub>PP</sub> Program or Set Lock-Bit Current	1,7		40	mA	V <sub>PP</sub> = 5.0V ± 10%
				15	mA	V <sub>PP</sub> = 12.0V ± 5%
I <sub>PPE</sub>	V <sub>PP</sub> Block Erase or Clear Block Lock-Bits Current	1,7		20	mA	V <sub>PP</sub> = 5.0V ± 10%
				15	mA	V <sub>PP</sub> = 12.0V ± 5%
I <sub>PPWS</sub> I <sub>PPES</sub>	V <sub>PP</sub> Program or Block Erase Suspend Current	1	10	200	μA	V <sub>PP</sub> = V <sub>PPH1/2</sub>

**Commercial Temperature DC Characteristics for  
4-, 8-, and 16-Mbit Smart 5 FlashFile™ Memories (Continued)**

Sym	Parameter	Notes	5.0V V <sub>CC</sub>		Unit	Test Conditions
			Min	Max		
V <sub>IL</sub>	Input Low Voltage	7	-0.5	0.8	V	
V <sub>IH</sub>	Input High Voltage	7	2.0	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage	3,7		0.45	V	V <sub>CC</sub> = V <sub>CC</sub> Min I <sub>OL</sub> = 5.8 mA
V <sub>OH1</sub>	Output High Voltage (TTL)	3,7	2.4		V	V <sub>CC</sub> = V <sub>CC</sub> Min I <sub>OH</sub> = -2.5 mA
V <sub>OH2</sub>	Output High Voltage (CMOS)	3,7	0.85 V <sub>CC</sub>		V	V <sub>CC</sub> = V <sub>CC</sub> Min I <sub>OH</sub> = -2.5 mA
			V <sub>CC</sub> - 0.4		V	V <sub>CC</sub> = V <sub>CC</sub> Min I <sub>OH</sub> = -100 µA
V <sub>PPLK</sub>	V <sub>PP</sub> Lockout Voltage	4,7		1.5	V	
V <sub>PPH1</sub>	V <sub>PP</sub> Voltage		4.5	5.5	V	
V <sub>PPH2</sub>	V <sub>PP</sub> Voltage		11.4	12.6	V	
V <sub>LKO</sub>	V <sub>CC</sub> Lockout Voltage		2.0		V	
V <sub>HH</sub>	RP# Unlock Voltage	8,9	11.4	12.6	V	Set Master Lock-Bit Override Lock-Bit

**NOTES:**

1. All currents are in RMS unless otherwise noted. Typical values at nominal V<sub>CC</sub> voltage and T<sub>A</sub> = +25°C. These currents are valid for all product versions (packages and speeds).
2. I<sub>CCWS</sub> and I<sub>CCES</sub> are specified with the device de-selected. If read or written while in erase suspend mode, the device's current is the sum of I<sub>CCWS</sub> or I<sub>CCES</sub> and I<sub>CCR</sub> or I<sub>CCW</sub>.
3. Includes RY/BY#.
4. Block erases, programs, and lock-bit configurations are inhibited when V<sub>PP</sub> ≤ V<sub>PPLK</sub>, and not guaranteed in the range between V<sub>PPLK</sub> (max) and V<sub>PPH1</sub> (min), between V<sub>PPH1</sub> (max) and V<sub>PPH2</sub> (min), and above V<sub>PPH2</sub> (max).
5. Automatic Power Savings (APS) reduces typical I<sub>CCR</sub> to 1 mA in static operation.
6. CMOS inputs are either V<sub>CC</sub> ± 0.2V or GND ± 0.2V. TTL inputs are either V<sub>IL</sub> or V<sub>IH</sub>.
7. Sampled, not 100% tested.
8. Master lock-bit set operations are inhibited when RP# = V<sub>IH</sub>. Block lock-bit configuration operations are inhibited when the master lock-bit is set and RP# = V<sub>IH</sub>. Block erases and programs are inhibited when the corresponding block-lock bit is set and RP# = V<sub>IH</sub>. Block erase, program, and lock-bit configuration operations are not guaranteed and should not be attempted with V<sub>IH</sub> < RP# < V<sub>HH</sub>.
9. RP# connection to a V<sub>HH</sub> supply is allowed for a maximum cumulative period of 80 hours.



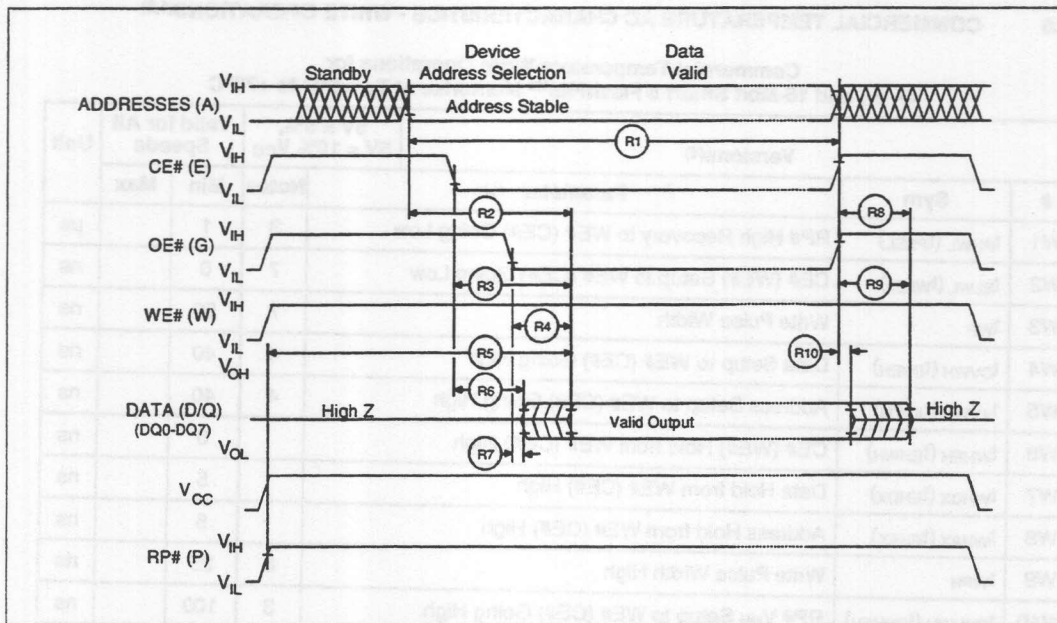
6.2.4 COMMERCIAL TEMPERATURE AC CHARACTERISTICS - READ-ONLY OPERATIONS<sup>(1)</sup>

Commercial Temperature Read-Only Operations for  
4-, 8-, and 16-Mbit Smart 5 FlashFile™ Memories at T<sub>A</sub> = 0°C to +70°C

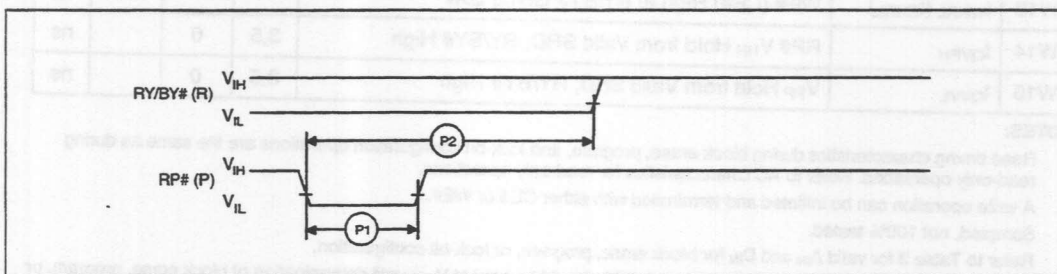
Versions(4)				5V ± 5% V <sub>CC</sub>		-85/-95(5)		—		—		Unit
				5V ± 10% V <sub>CC</sub>		—		-90/-100(6)		-120(6)		
#	Sym	Parameter		Notes	Min	Max	Min	Max	Min	Max		
R1	t <sub>AVAV</sub>	Read Cycle Time	4, 8 Mbit		85		90		120		ns	
			16 Mbit		95		100		120		ns	
R2	t <sub>AVQV</sub>	Address to Output	4, 8 Mbit		85		90		120		ns	
		Delay	16 Mbit		95		100		120		ns	
R3	t <sub>ELQV</sub>	CE# to Output Delay	4, 8 Mbit	2	85		90		120		ns	
			16 Mbit	2	95		100		120		ns	
R4	t <sub>GLQV</sub>	OE# to Output Delay		2		40		45		50	ns	
R5	t <sub>PHQV</sub>	RP# High to Output Delay				400		400		400	ns	
R6	t <sub>ELQX</sub>	CE# to Output in Low Z		3	0		0		0		ns	
R7	t <sub>GLQX</sub>	OE# to Output in Low Z		3	0		0		0		ns	
R8	t <sub>EHQZ</sub>	CE# High to Output in High Z		3		55		55		55	ns	
R9	t <sub>GHQZ</sub>	OE# High to Output in High Z		3		10		10		15	ns	
R10	t <sub>OH</sub>	Output Hold from Address, CE# or OE# Change, Whichever Occurs First		3	0		0		0		ns	

NOTES:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to t<sub>ELQV</sub>-t<sub>GLQV</sub> after the falling edge of CE# without impact on t<sub>ELQV</sub>.
3. Sampled, not 100% tested.
4. See Ordering Information for device speeds (valid operational combinations).
5. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Speed Configuration) for testing characteristics.
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.


**Figure 15. AC Waveform for Read Operations**

### 6.2.5 COMMERCIAL TEMPERATURE RESET OPERATIONS


**Figure 16. AC Waveform for Reset Operation**

#	Sym	Parameter	Notes	Min	Max	Unit
P1	$t_{PLPH}$	RP# Pulse Low Time (If RP# is tied to $V_{CC}$ , this specification is not applicable)		100		ns
P2	$t_{PLRH}$	RP# Low to Reset during Block Erase, Program, or Lock-Bit Configuration	2,3		12	$\mu$ s

**NOTES:**

1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted when the WSM is not busy (RY/BY# = '1'), the reset will complete within 100 ns.
3. A reset time,  $t_{HQR}$ , is required from the latter of RY/BY# or RP# going high until outputs are valid.

## PRODUCT PREVIEW

6.2.6 COMMERCIAL TEMPERATURE AC CHARACTERISTICS - WRITE OPERATIONS<sup>(1,2)</sup>

Commercial Temperature Write Operations for  
4-, 8-, and 16-Mbit Smart 5 FlashFile™ Memories at  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$

		Versions <sup>(4)</sup>	5V ± 5%, 5V ± 10% V <sub>CC</sub>	Valid for All Speeds		Unit
#	Sym	Parameter	Notes	Min	Max	
W1	t <sub>PHWL</sub> (t <sub>PHL</sub> )	RP# High Recovery to WE# (CE#) Going Low	3	1		μs
W2	t <sub>ELWL</sub> (t <sub>WLEL</sub> )	CE# (WE#) Setup to WE# (CE#) Going Low	7	0		ns
W3	t <sub>WP</sub>	Write Pulse Width	7	50		ns
W4	t <sub>DVWH</sub> (t <sub>DVEH</sub> )	Data Setup to WE# (CE#) Going High	4	40		ns
W5	t <sub>AWWH</sub> (t <sub>AVEH</sub> )	Address Setup to WE# (CE#) Going High	4	40		ns
W6	t <sub>WHEH</sub> (t <sub>EHWH</sub> )	CE# (WE#) Hold from WE# (CE#) High		0		ns
W7	t <sub>WHDH</sub> (t <sub>EHDX</sub> )	Data Hold from WE# (CE#) High		5		ns
W8	t <sub>WHAX</sub> (t <sub>EHAX</sub> )	Address Hold from WE# (CE#) High		5		ns
W9	t <sub>WPH</sub>	Write Pulse Width High	8	25		ns
W10	t <sub>PHHWH</sub> (t <sub>PHHEH</sub> )	RP# V <sub>HH</sub> Setup to WE# (CE#) Going High	3	100		ns
W11	t <sub>VPWH</sub> (t <sub>VPEH</sub> )	V <sub>PP</sub> Setup to WE# (CE#) Going High	3	100		ns
W12	t <sub>WHGL</sub> (t <sub>EHGL</sub> )	Write Recovery before Read		0		ns
W13	t <sub>WHRL</sub> (t <sub>EHRL</sub> )	WE# (CE#) High to RY/BY# Going Low			90	ns
W14	t <sub>QVPH</sub>	RP# V <sub>HH</sub> Hold from Valid SRD, RY/BY# High	3,5	0		ns
W15	t <sub>QVVL</sub>	V <sub>PP</sub> Hold from Valid SRD, RY/BY# High	3,5	0		ns

NOTES:

- Read timing characteristics during block erase, program, and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
- A write operation can be initiated and terminated with either CE# or WE#.
- Sampled, not 100% tested.
- Refer to Table 3 for valid A<sub>IN</sub> and D<sub>IN</sub> for block erase, program, or lock-bit configuration.
- V<sub>PP</sub> should be held at V<sub>PPH1/2</sub> (and if necessary RP# should be held at V<sub>HH</sub>) until determination of block erase, program, or lock-bit configuration success (SR.1/3/4/5 = 0).
- See Ordering Information for device speeds (valid operational combinations).
- Write pulse width (t<sub>WP</sub>) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). Hence, t<sub>WP</sub> = t<sub>WLWH</sub> = t<sub>LEH</sub> = t<sub>WLEH</sub> = t<sub>ELWH</sub>. If CE# is driven low 10 ns before WE# going low, WE# pulse width requirement decreases to t<sub>WP</sub> - 20 ns.
- Write pulse width high (t<sub>WPH</sub>) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low last). Hence, t<sub>WPH</sub> = t<sub>WHWL</sub> = t<sub>EHL</sub> = t<sub>WHEL</sub> = t<sub>EHWL</sub>.



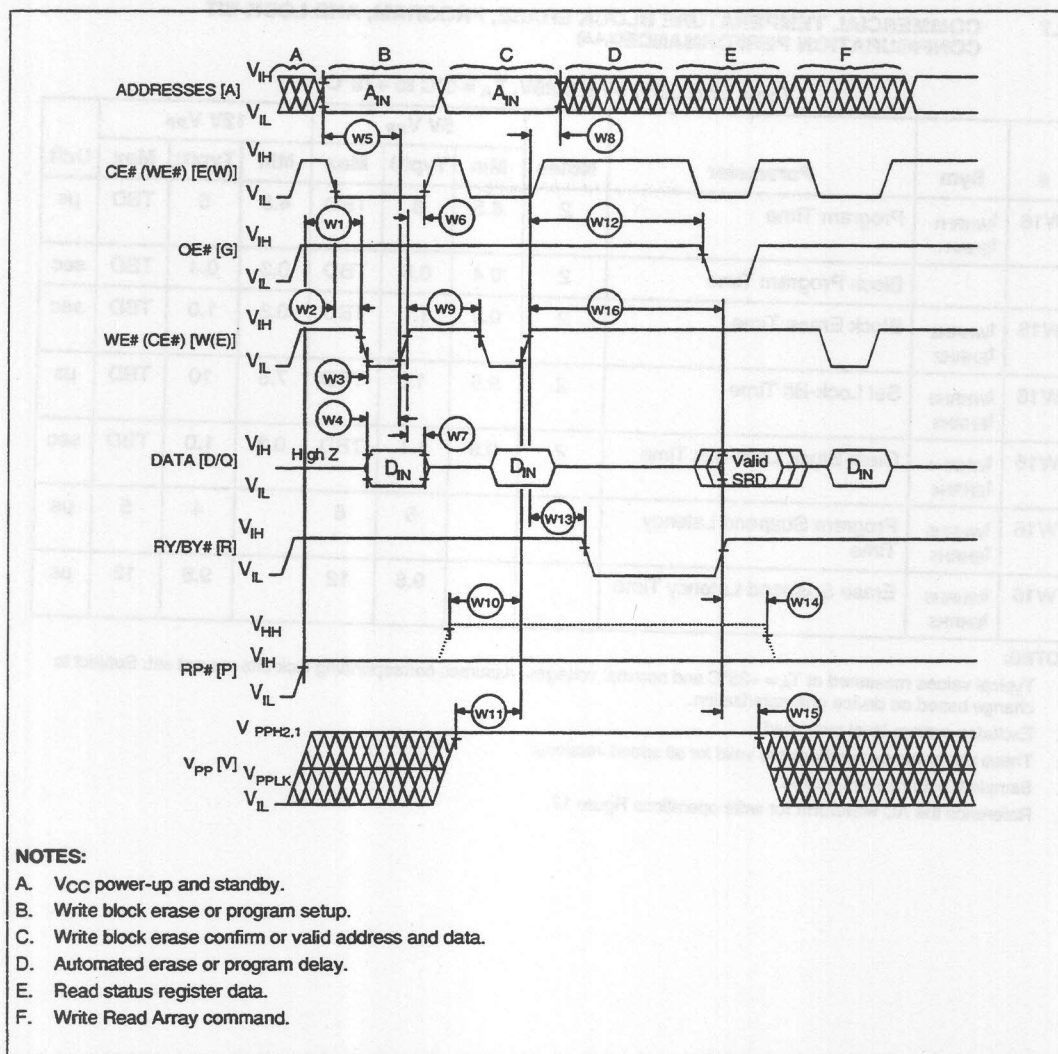


Figure 17. AC Waveform for Write Operations

6.2.7 COMMERCIAL TEMPERATURE BLOCK ERASE, PROGRAM, AND LOCK-BIT CONFIGURATION PERFORMANCE<sup>(3,4,5)</sup>

$V_{CC} = 5V \pm 0.5V$ ,  $5V \pm 0.25V$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$

#	Sym	Parameter	Notes	5V $V_{PP}$			12V $V_{PP}$			Unit
				Min	Typ <sup>(1)</sup>	Max	Min	Typ <sup>(1)</sup>	Max	
W16	$t_{WHRH1}$ $t_{EHRH1}$	Program Time	2	6.5	8	TBD	4.8	6	TBD	$\mu s$
		Block Program Time	2	0.4	0.5	TBD	0.3	0.4	TBD	sec
W16	$t_{WHRH2}$ $t_{EHRH2}$	Block Erase Time	2	0.9	1.1	TBD	0.3	1.0	TBD	sec
W16	$t_{WHRH3}$ $t_{EHRH3}$	Set Lock-Bit Time	2	9.5	12	TBD	7.8	10	TBD	$\mu s$
W16	$t_{WHRH4}$ $t_{EHRH4}$	Clear Block Lock-Bits Time	2	0.9	1.1	TBD	0.3	1.0	TBD	sec
W16	$t_{WHRH5}$ $t_{EHRH5}$	Program Suspend Latency Time			5	6		4	5	$\mu s$
W16	$t_{WHRH5}$ $t_{EHRH5}$	Erase Suspend Latency Time			9.6	12		9.6	12	$\mu s$

NOTES:

1. Typical values measured at  $T_A = +25^{\circ}C$  and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled, but not 100% tested.
5. Reference the AC waveform for write operations Figure 17.

### 6.3 Extended Temperature Operating Conditions

Except for the specifications given in this section, all DC and AC characteristics are identical to those give in commercial temperature specifications. See the Section 6.2 for commercial temperature specifications.

**Extended Temperature and V<sub>CC</sub> Operating Conditions**

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
T <sub>A</sub>	Operating Temperature		-40	+85	°C	Ambient Temperature

#### 6.3.1 EXTENDED TEMPERATURE DC CHARACTERISTICS

**Extended Temperature DC Characteristics for  
4-, 8-, and 16-Mbit Smart 5 FlashFile™ Memories**

Sym	Parameter	Notes	5.0V V <sub>CC</sub>		Unit	Test Conditions
			Typ	Max		
I <sub>CCD</sub>	V <sub>CC</sub> Deep Power-Down Current	1		20	μA	RP# = GND ± 0.2V I <sub>OUT</sub> (RY/BY#) = 0 mA

**NOTE:**

1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds). Contact Intel's Application Support Hotline or your local sales office for information about typical specifications.

#### 6.3.2 EXTENDED TEMPERATURE AC CHARACTERISTICS - READ-ONLY OPERATIONS<sup>(1)</sup>

**Extended Temperature Read-Only Operations for  
4-, 8-, and 16-Mbit Smart 5 FlashFile™ Memories at T<sub>A</sub> = -40°C to +85°C**

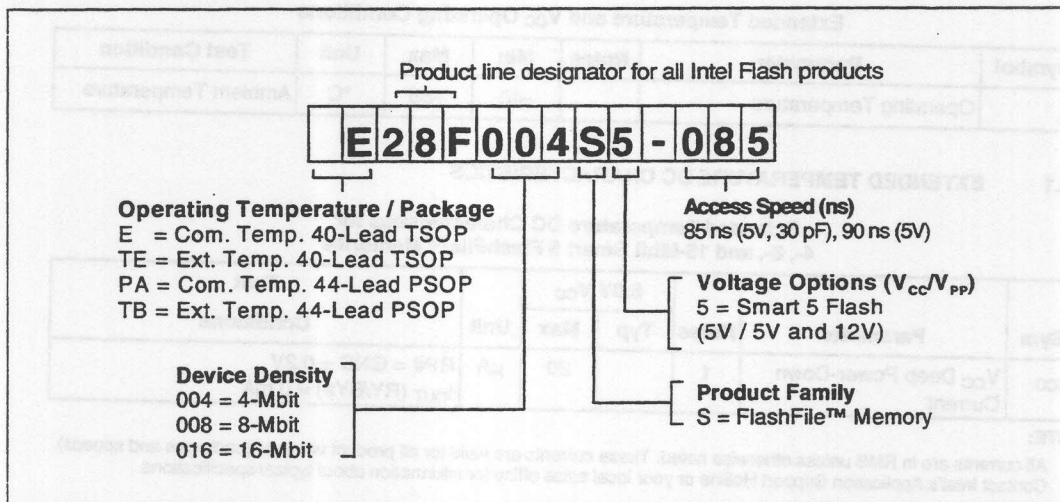
		Versions <sup>(3)</sup>	5V ± 10% V <sub>CC</sub>		-100/-110		Unit
#	Sym	Parameter	Notes		Min	Max	
R1	t <sub>AVAV</sub>	Read Cycle Time	4, 8 Mbit		100		ns
			16 Mbit		110		ns
R2	t <sub>AVQV</sub>	Address to Output Delay	4, 8 Mbit			100	ns
			16 Mbit			110	ns
R3	t <sub>ELQV</sub>	CE# to Output Delay	4, 8 Mbit	2		100	ns
			16 Mbit	2		110	ns

**NOTES:**

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to t<sub>ELQV</sub>-t<sub>GLQV</sub> after the falling edge of CE# without impact on t<sub>ELQV</sub>.
3. See Ordering Information for device speeds (valid operational combinations).



## APPENDIX A ORDERING INFORMATION



Order Code by Density			Valid Operational Combinations	
			5V $V_{CC}$	
4 Mbit	8 Mbit	16 Mbit	10% $V_{CC}$ 100 pF load	5% $V_{CC}$ 30 pF load
<b>Commercial Temperature</b>				
E28F004S5-85	E28F008S5-85	E28F016S5-95	-90/-100 <sup>(1)</sup>	-85/-95 <sup>(1)</sup>
E28F004S5-120	E28F008S5-120	E28F016S5-120	-120	
PA28F004S5-85	PA28F008S5-85	PA28F016S5-95	-90/-100 <sup>(1)</sup>	-85/-95 <sup>(1)</sup>
PA28F004S5-120	PA28F008S5-120	PA28F016S5-120	-120	
<b>Extended Temperature</b>				
TE28F004S5-100	TE28F008S5-100	TE28F016S5-110	-100/-110 <sup>(1)</sup>	
TB28F004S5-100	TB28F008S5-100	TB28F016S5-110	-100/-110 <sup>(1)</sup>	

**NOTE:**

- Valid access time for 16-Mbit byte-wide FlashFile memory.

## APPENDIX B ADDITIONAL INFORMATION(1,2)

Order Number	Document/Tool
290598	<i>Byte-Wide Smart 3 FlashFile™ Memory Family Datasheet</i>
290600	<i>Byte-Wide SmartVoltage FlashFile™ Memory Family Datasheet</i>
292183	<i>AB-64 4-, 8-, 16-Mbit Byte-Wide FlashFile™ Memory Family Overview</i>
292094	<i>AP-359 28F008SA Hardware Interfacing</i>
292099	<i>AP-364 28F008SA Automation and Algorithms</i>
292123	<i>AP-374 Flash Memory Write Protection Techniques</i>
292180	<i>AP-625 28F008SC Compatibility with 28F008SA</i>
292182	<i>AP-627 Byte-Wide FlashFile™ Memory Family Software Drivers</i>
Contact Intel/Distribution Sales Office	4-, 8-, and 16-Mbit Schematic Symbols
Contact Intel/Distribution Sales Office	4-, 8-, and 16-Mbit TimingDesigner* Files
Contact Intel/Distribution Sales Office	4-, 8-, and 16-Mbit VHDL and Verilog Models
Contact Intel/Distribution Sales Office	4-, 8-, and 16-Mbit iBIS Models

**NOTE:**

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at <http://www.Intel.com> for technical documentation and tools.

# APPENDIX B ADDITIONAL INFORMATION (2)

Order Number	Documentation
280000	Byte-Wide Smart & Protect™ Memory Family Datasheet
280005	Byte-Wide Smart & Protect™ Memory Family Datasheet
280100	4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384, 32768, 65536, 131072, 262144, 524288, 1048576, 2097152, 4194304, 8388608, 16777216, 33554432, 67108864, 134217728, 268435456, 536870912, 1073741824, 2147483648, 4294967296, 8589934592, 17179869184, 34359738368, 68719476736, 137438953472, 274877906944, 549755813888, 1099511627776, 2199023255552, 4398046511104, 8796093022208, 17592186044416, 35184372088832, 70368744177664, 140737488355328, 281474976710656, 562949953421312, 1125899906842624, 2251799813685248, 4503599627370496, 9007199254740992, 18014398509481984, 36028797018963968, 72057594037927936, 144115188075855872, 288230376151711744, 576460752303423488, 1152921504606846976, 2305843009213693952, 4611686018427387904, 9223372036854775808, 18446744073709551616, 36893488147419103232, 73786976294838206464, 147573952589676412928, 295147905179352825856, 590295810358705651712, 1180591620717411303424, 2361183241434822606848, 4722366482869645213696, 9444732965739290427392, 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